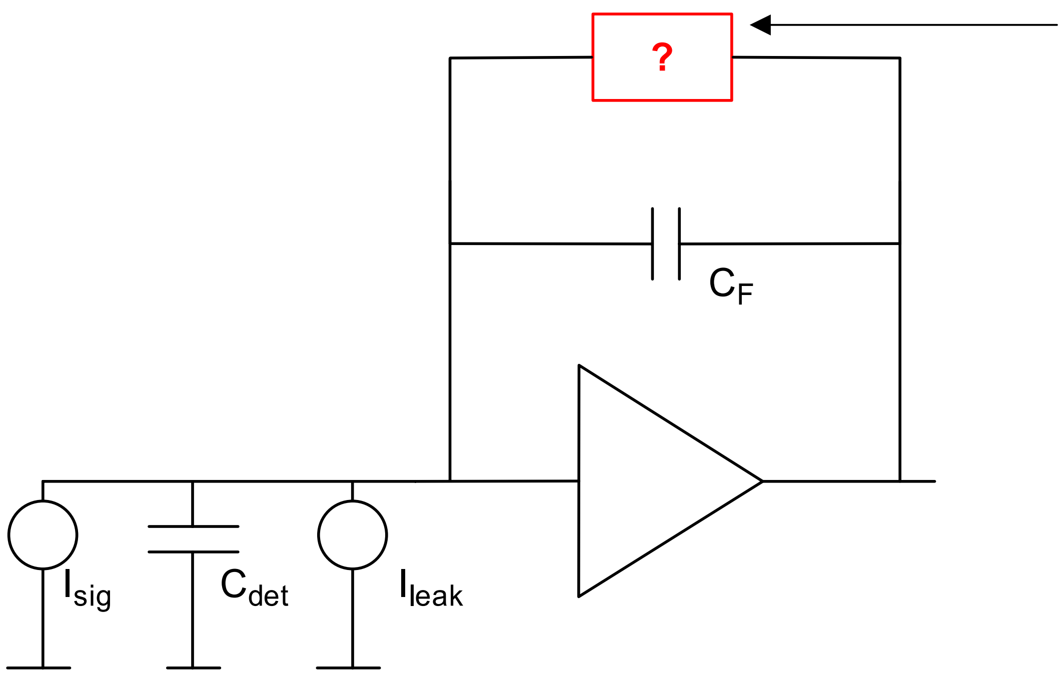
Charge-Sensitive Preamplifier
Continuous Reset

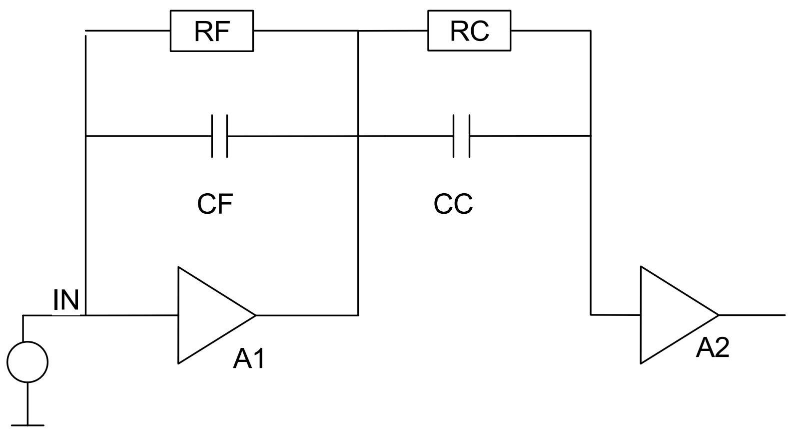


Requirements:

- discharge C_F
- source I_{leak} (variable)
- minimum noise
- linear
- insensitive to process, temperature, and supply variation
- low capacitance

Simplest: FET
Drawback:
Nonlinear
Needs biasing

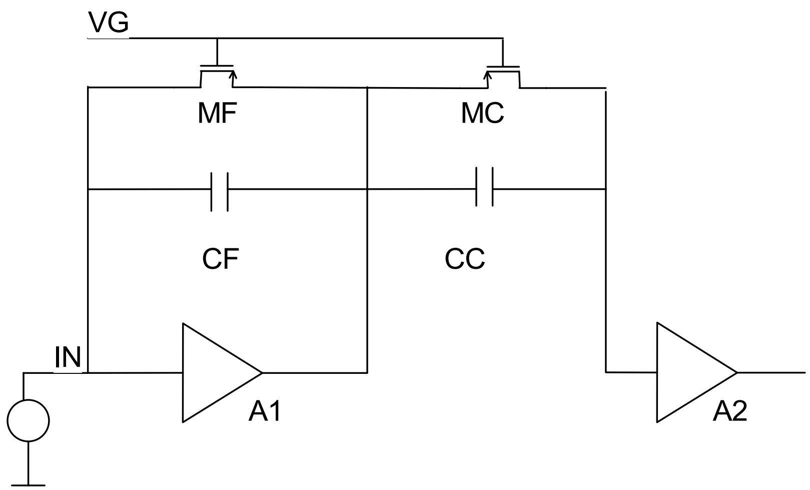
Nonlinear Pole-Zero Compensation



<u>Classical</u>

RF · CF = RC ·CC

Zero created by RC,CC cancels pole formed by RF, CF



<u>IC version</u>

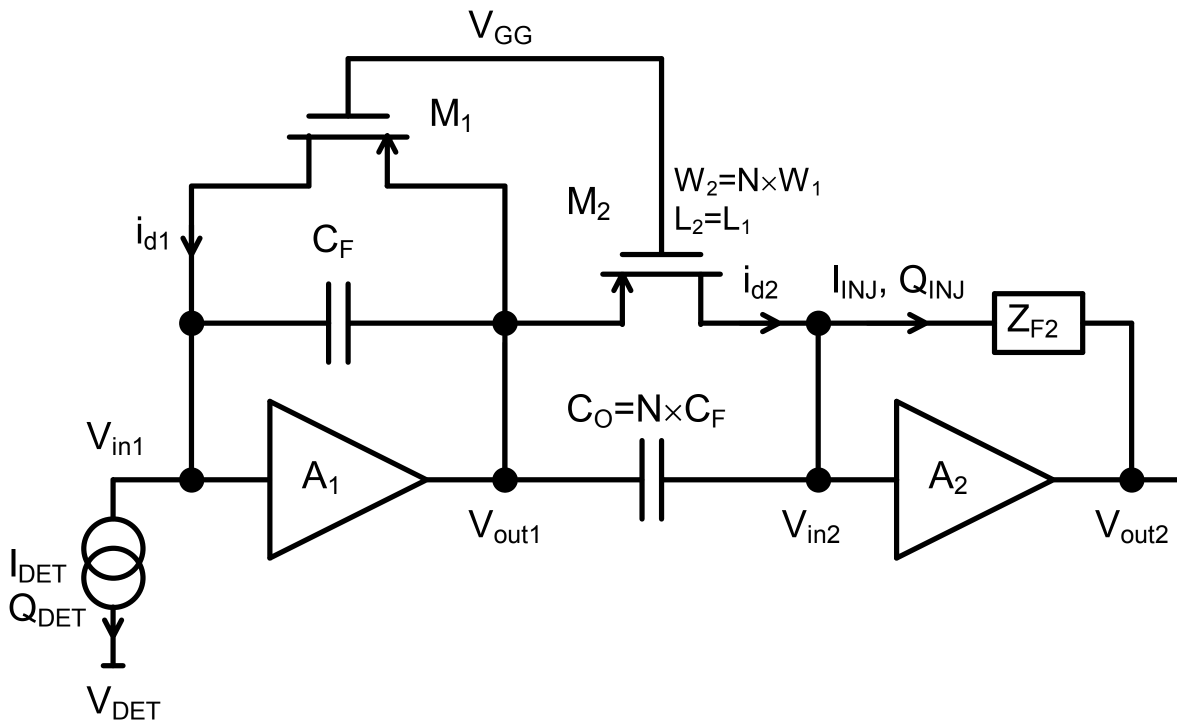
CC = N · CF

$(W/L)_{MC} = N \cdot (W/L)_{MF}$

Zero created by MC, CC cancels pole formed by MF, CF

Rely on good matching characteristics of CMOS FETs and capacitors

In more detail…



$V_{gs1} = V_{gs2}$
$V_{in1} = V_{in2}$
$V_{T1} = V_{T2}$

$I_{d1} = I_{DET}$
$I_{d2} = N \cdot I_{DET}$
$Q_{inj} = N \cdot Q_{DET}$

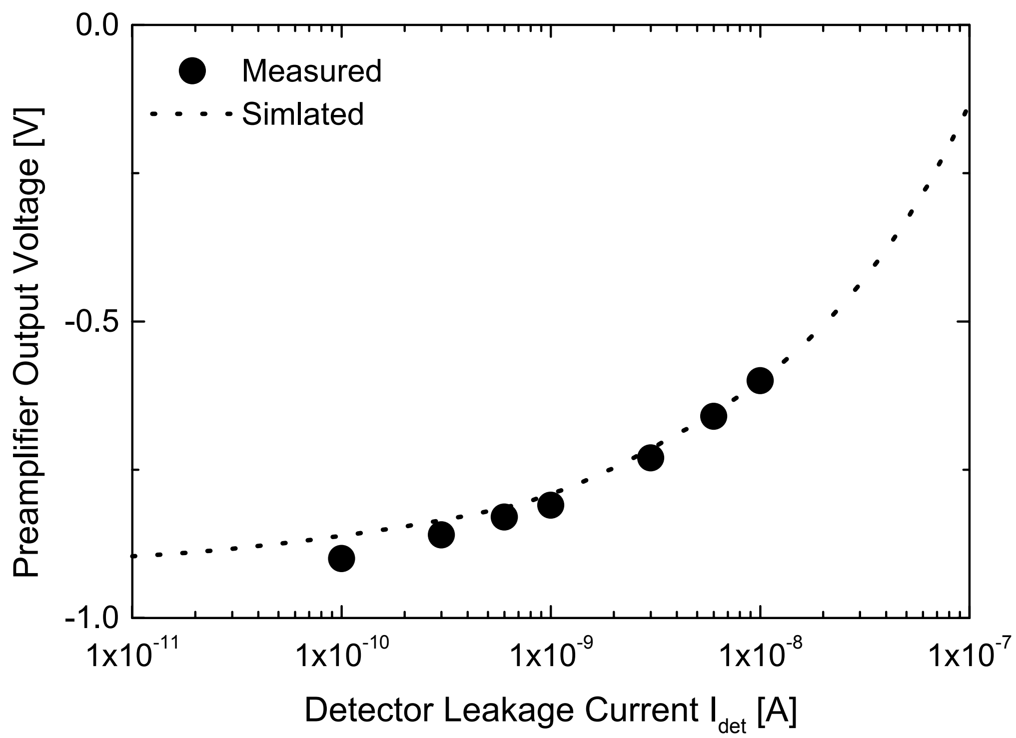
Composite amplifier is a charge (current) amplifier with gain of N

DC Analysis

M1, M2 in saturation, strong inversion

$$V_{OUT} \approx V_{GG} - V_{T1} + \sqrt{\frac{2}{k'}\frac{L_1}{W_1}\left(I_{DET} + I_B\right)}$$

- Leakage current up to 100 nA can be sourced with modest increase in output voltage

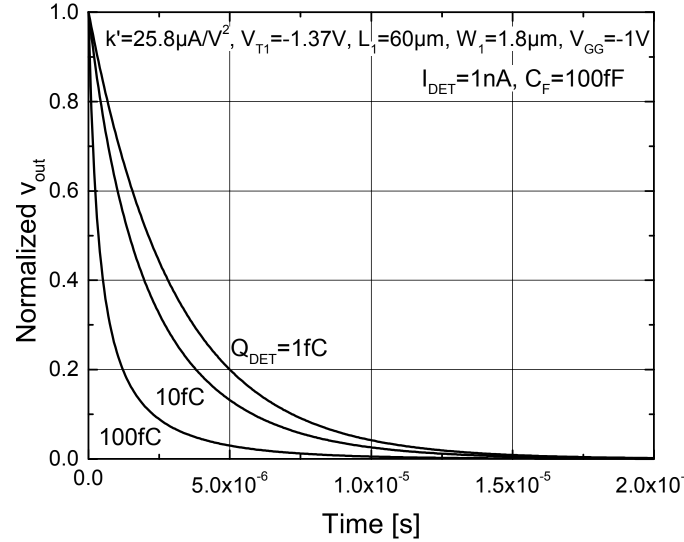


Dynamic Analysis

First stage alone

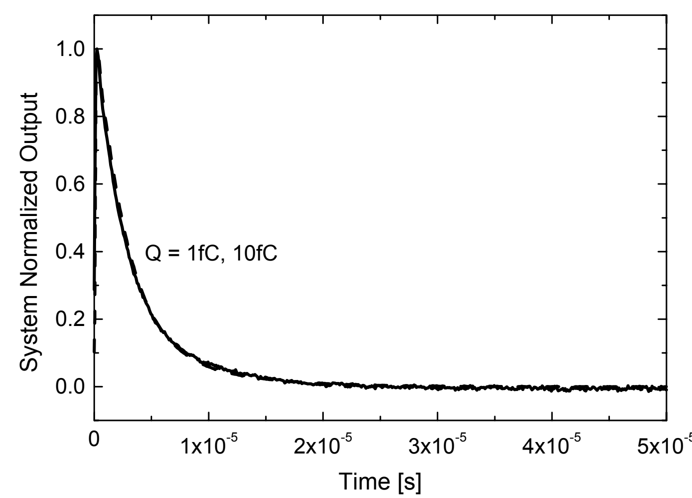
$$v_{out}(t) = \frac{2\left(V_{GS1} - V_{T1}\right)}{\frac{K}{V_{GS1} - V_{T1}} \frac{C_F}{k'} \frac{L_1}{W_1} \exp\left[\frac{-t}{C_F} k' \frac{W_1}{L_1}\left(V_{GS1} - V_{T1}\right)\right] + 1}$$

- Decay time constant ~ C_F/g_{m1}
- Effective feedback resistance of M1: $R_{F,eff} = 1/g_{m1}$
- Strong variation with Q_{DET}



With compensation

- Linearity is recovered
- Time constant no longer depends on injected charge



Noise Analysis

Parallel noise:

M1, M2 bias condition at minimum I_{DET}:

VDS > VGS – VT Saturation

(VGS – VT) >> kT/q Strong Inversion

M1 conbutes thermal noise < shot noise of detector leakage

$$ENC^2 = 2kTA_3t_m\,[\gamma g_{m1}\cdot(1 + g_{m1}/g_{mA}) + (\gamma g_{m2} + 1/R_{F2}) / N^2] + \text{series} + 1/f$$

Non-stationary noise:

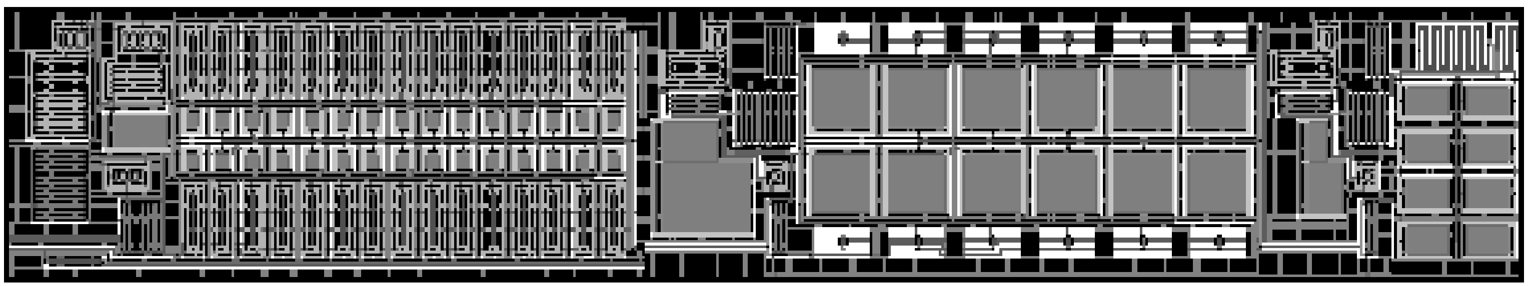
Due to increase in M1's drain current during the reset.

Signal-dependent $ENC_{NS} \sim \sqrt{Q_{DET}}$

Responsible for minor (< 2%) degradation of S/N.

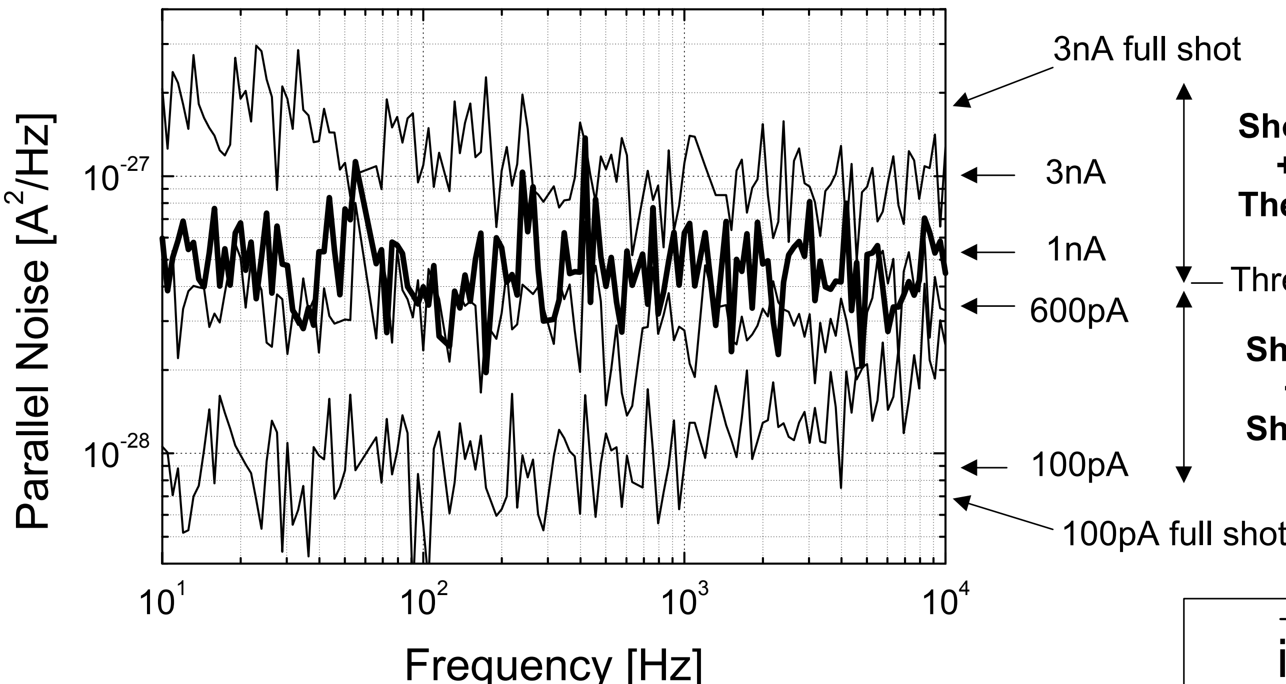
Layout

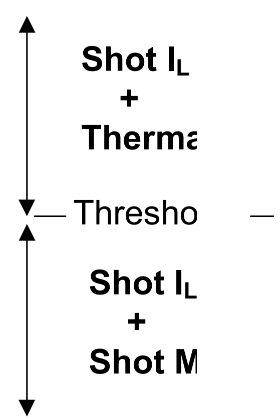
Two-stage compensation circuit
N_1 = 24 (PMOS), N_2 = 6 (NMOS)
N_{tot} = 144



0.14 x 0.78 mm

Parallel Noise

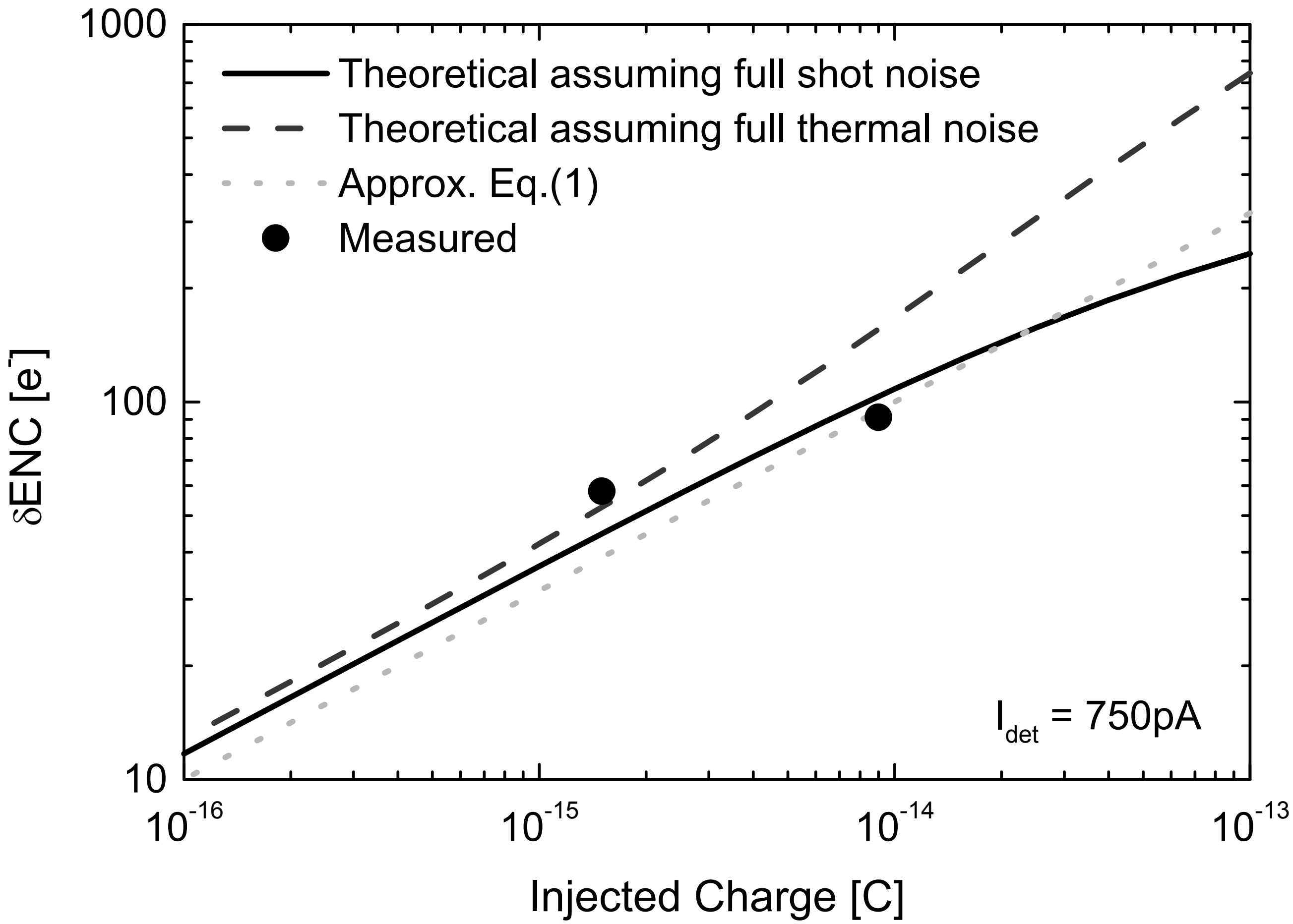




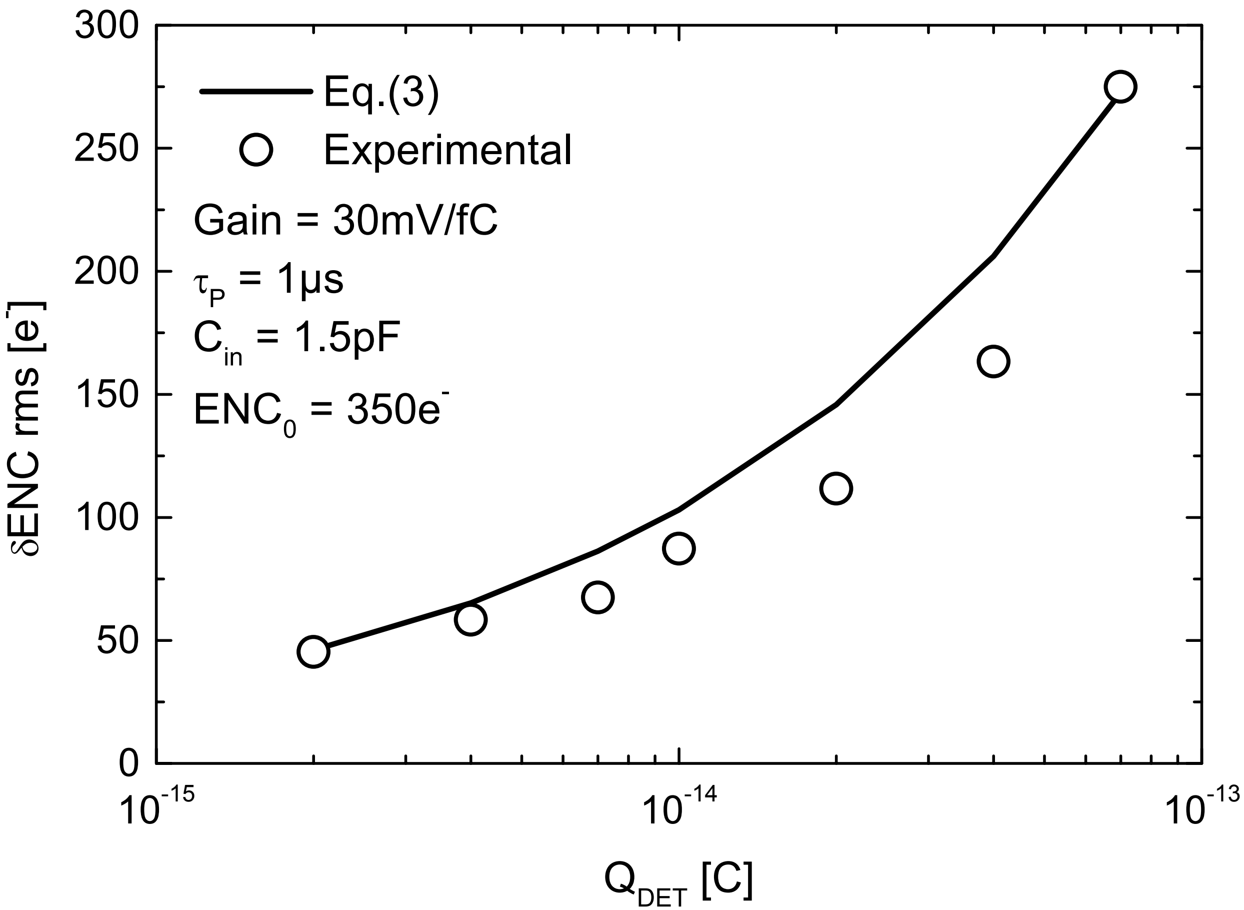
$\overline{i_n^2} \div$

$\overline{i_n^2}$

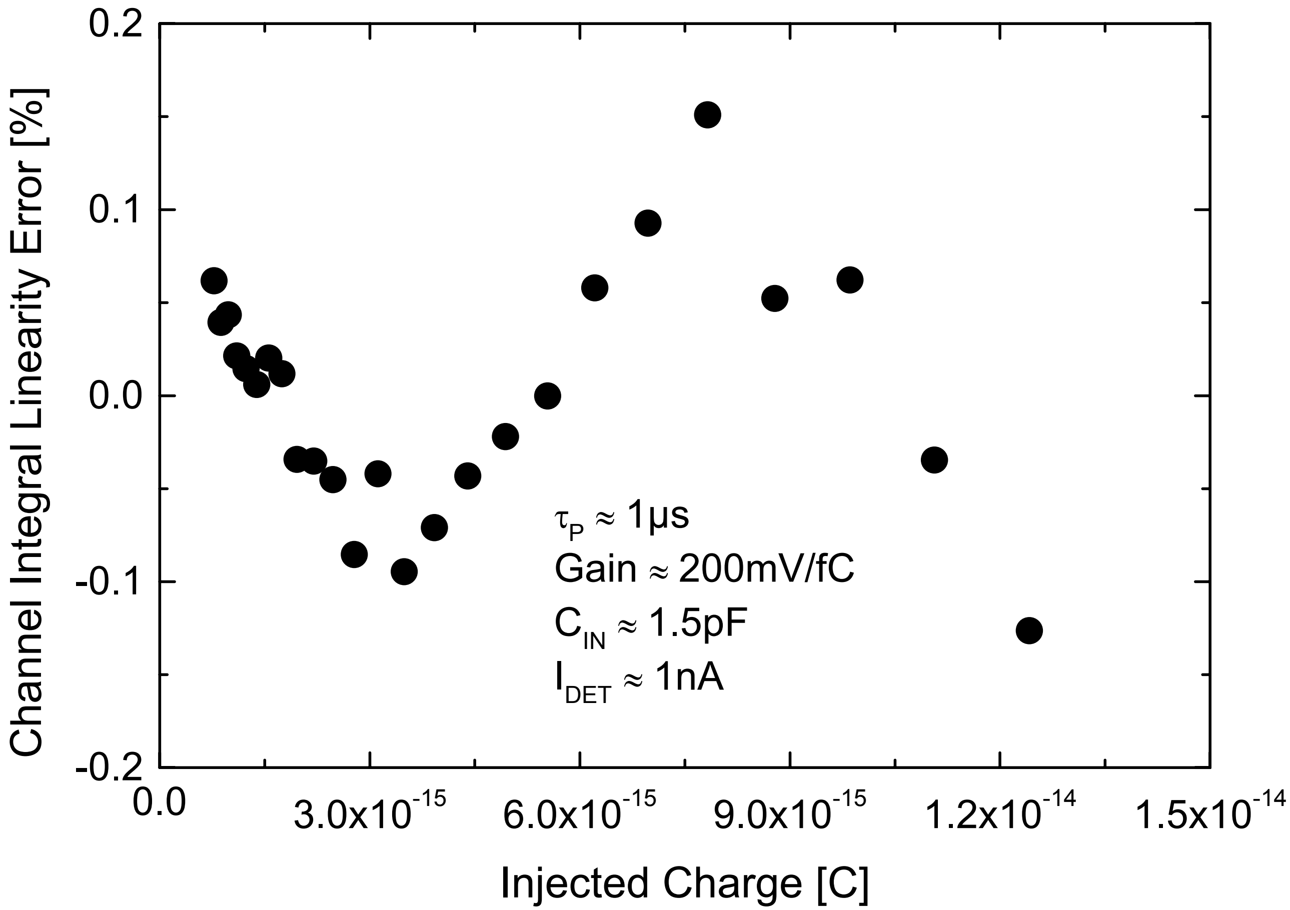
Nonstationary Noise



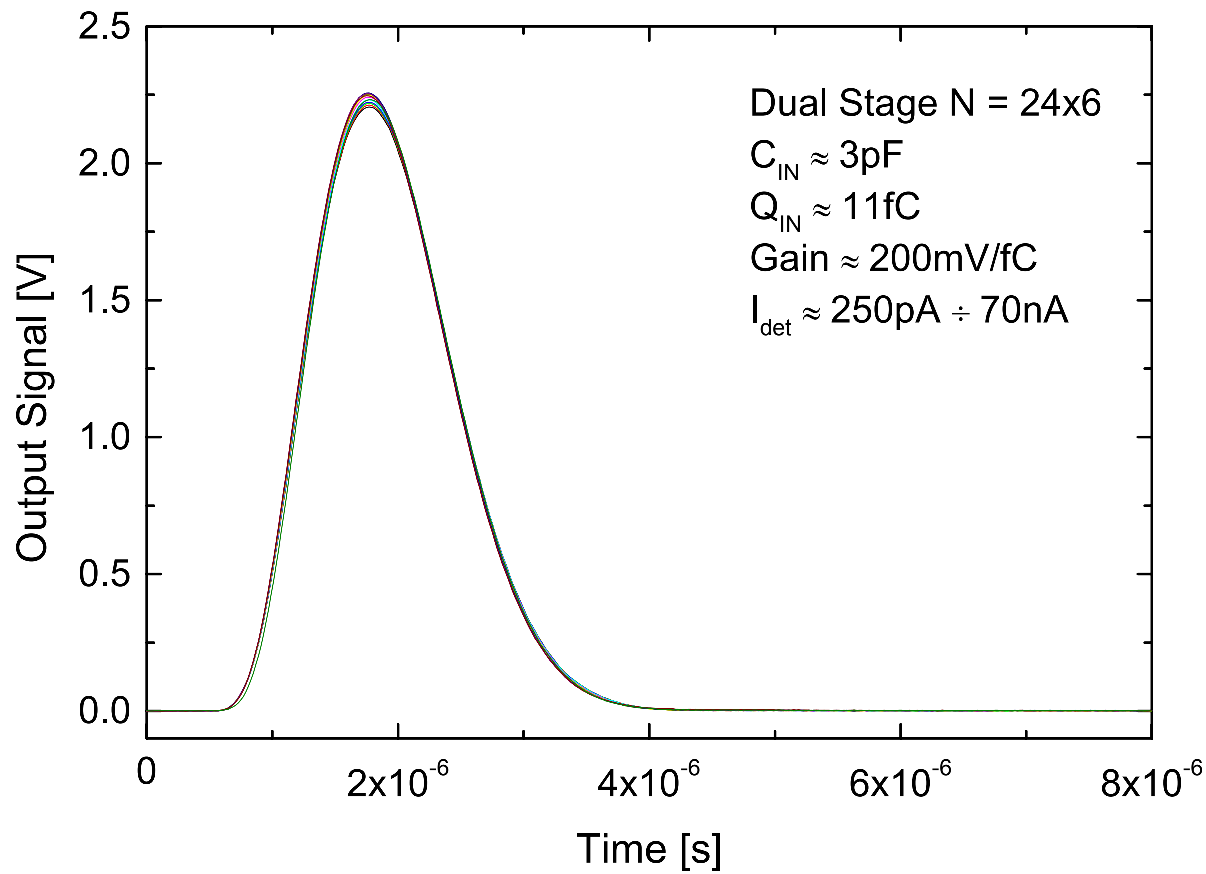
Nonstationary Noise



Nonlinearity



Leakage Current Handling



Summary

- New reset system for DC-coupled detectors
- Self-adaptive to wide range of leakage current
- No tweaking or switching
- Excellent noise and linearity
- Versatile

Shaping	5th order compl. unip.
Gain	≈ 200mV/fC
Peaking time	≈ 400ns
ENC	≈ 30+37/pF+0.4√(Q/q)
Integral linearity error	< 0.2% @ 13fC