BROOKHAVEN NATIONAL LABORATORY
Instrumentation Division

NSLS
NATIONAL SYNCHROTRON LIGHT SOURCE

Silicon Sensor with Readout ASICs for EXAFS Spectroscopy

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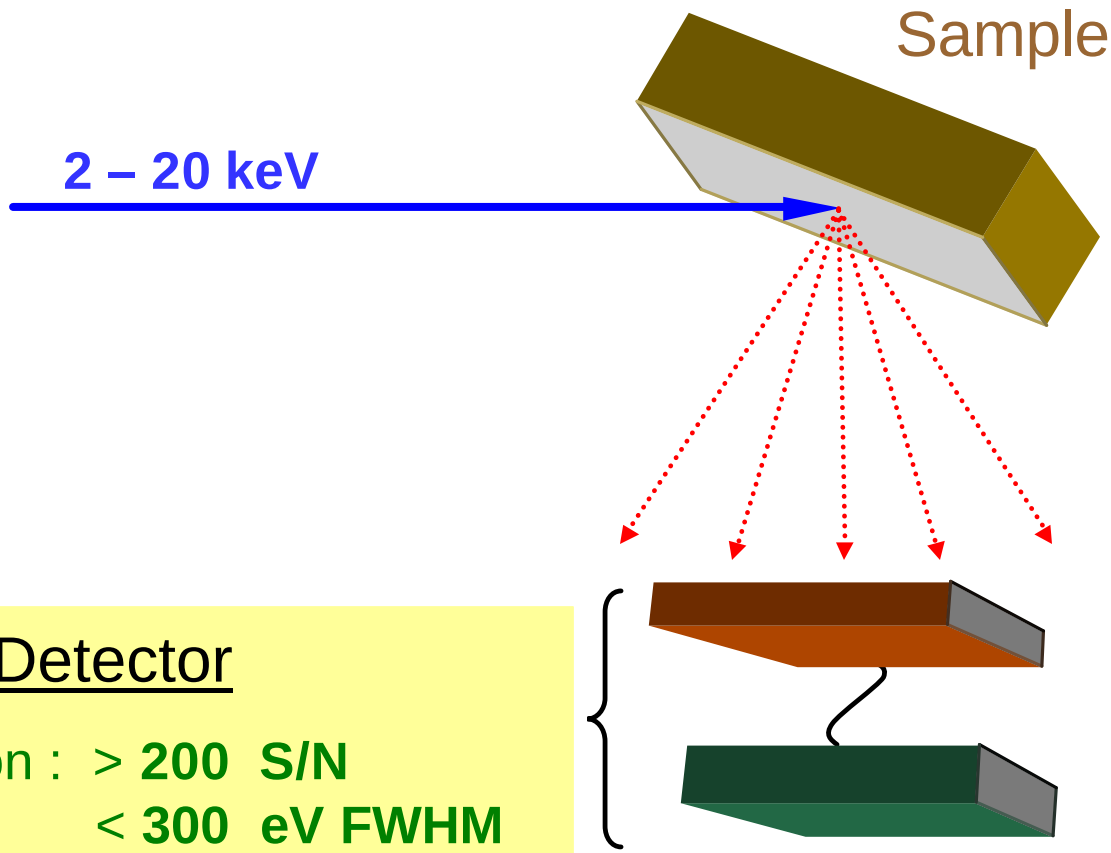
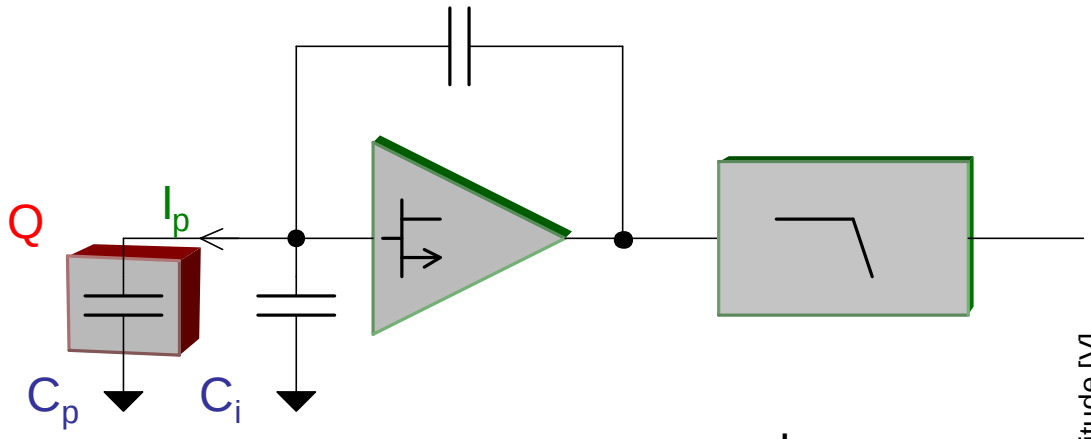
Typical fluorescence EXAFS spectroscopy geometry



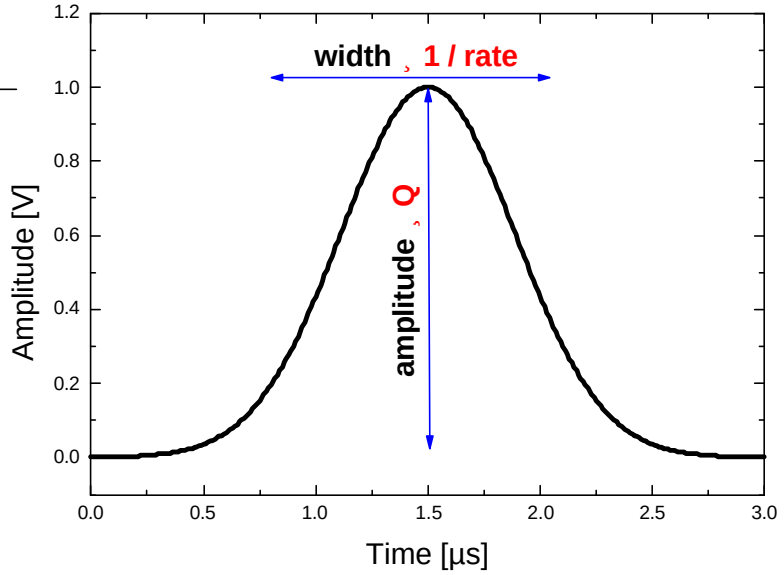
Detector

- Resolution : > **200 S/N**
  < **300 eV FWHM**
- Rate : > **10 MHz/cm²**
  > **100 kHz/pixel**
- Spectroscopy (energy windows)

Resolution vs Rate

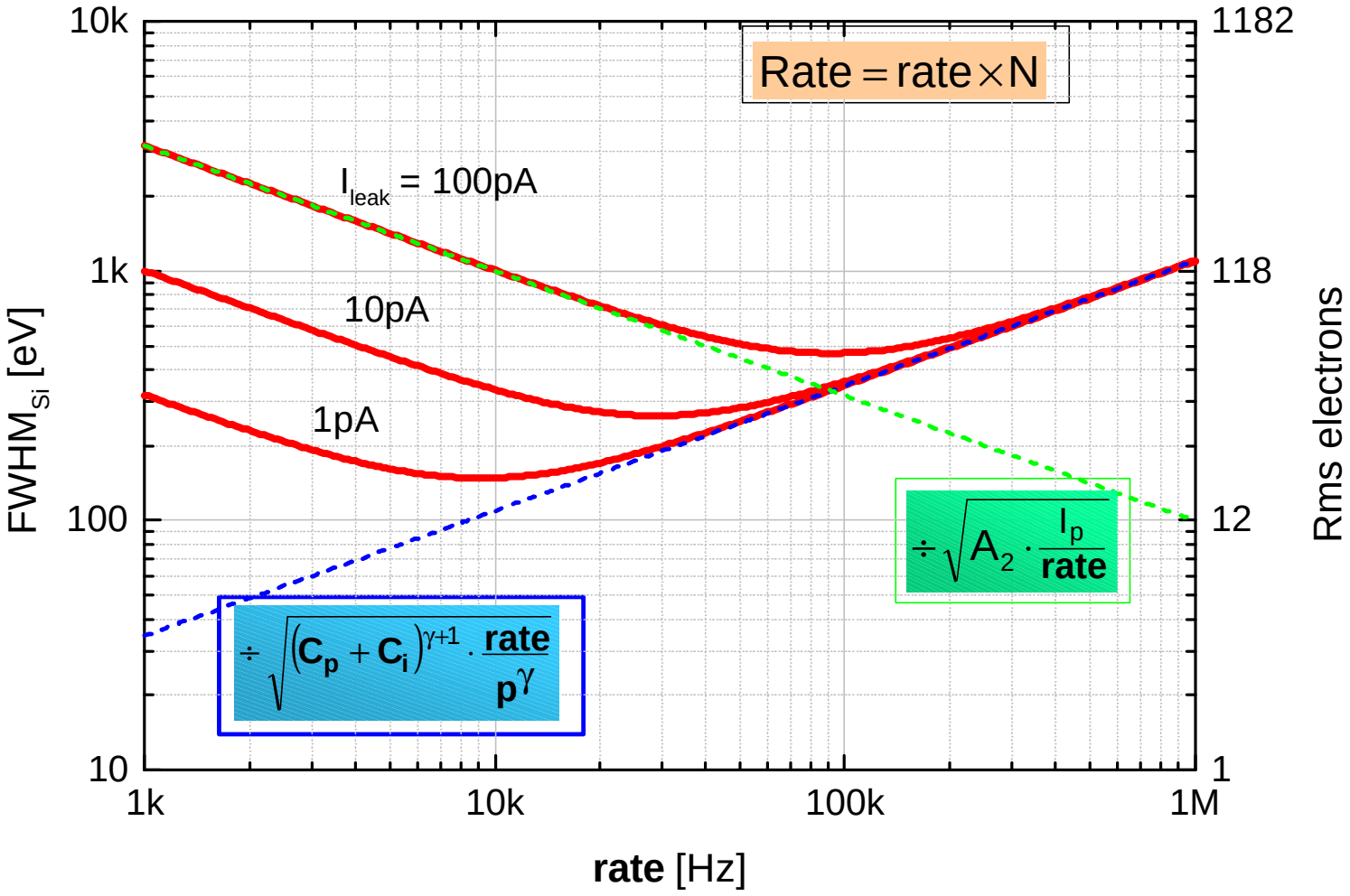


$$\text{rate} = \frac{\text{Rate}}{N} \quad (N = \text{number of pixels})$$

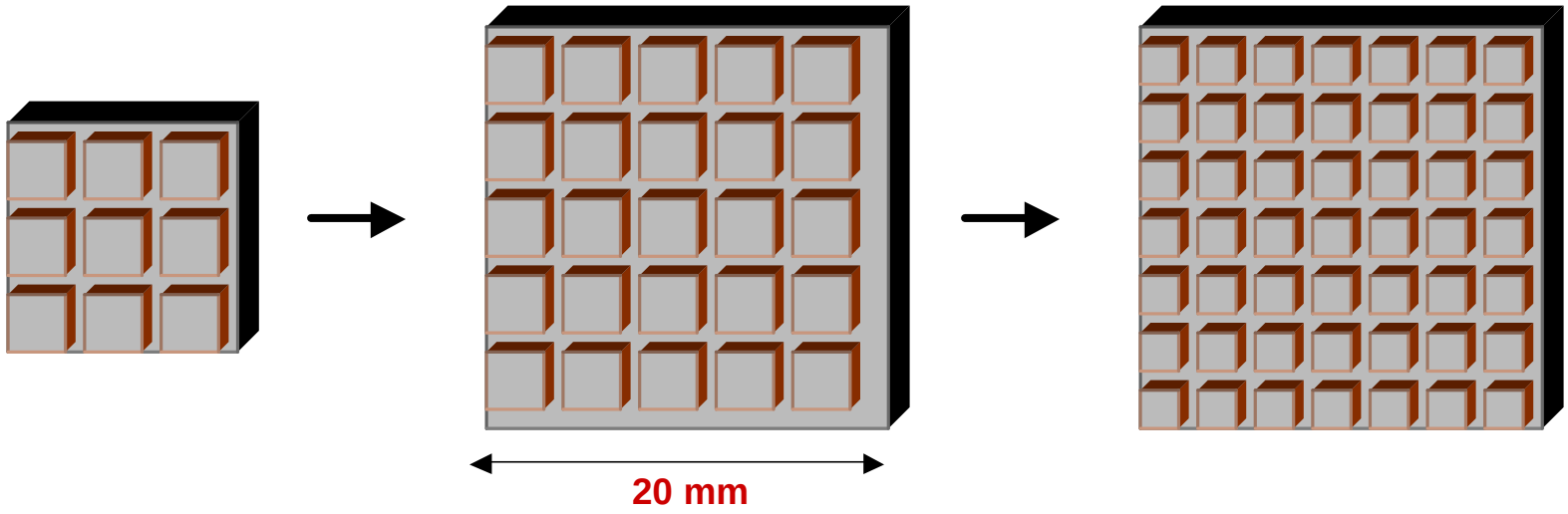


$$ENC^2 = A_1(\gamma)\left(C_p + C_i\right)^{\gamma+1}\frac{\text{rate}}{p^{\gamma}} + A_2\frac{I_p}{\text{rate}} \qquad 0 < \gamma < 1$$

Resolution vs Rate



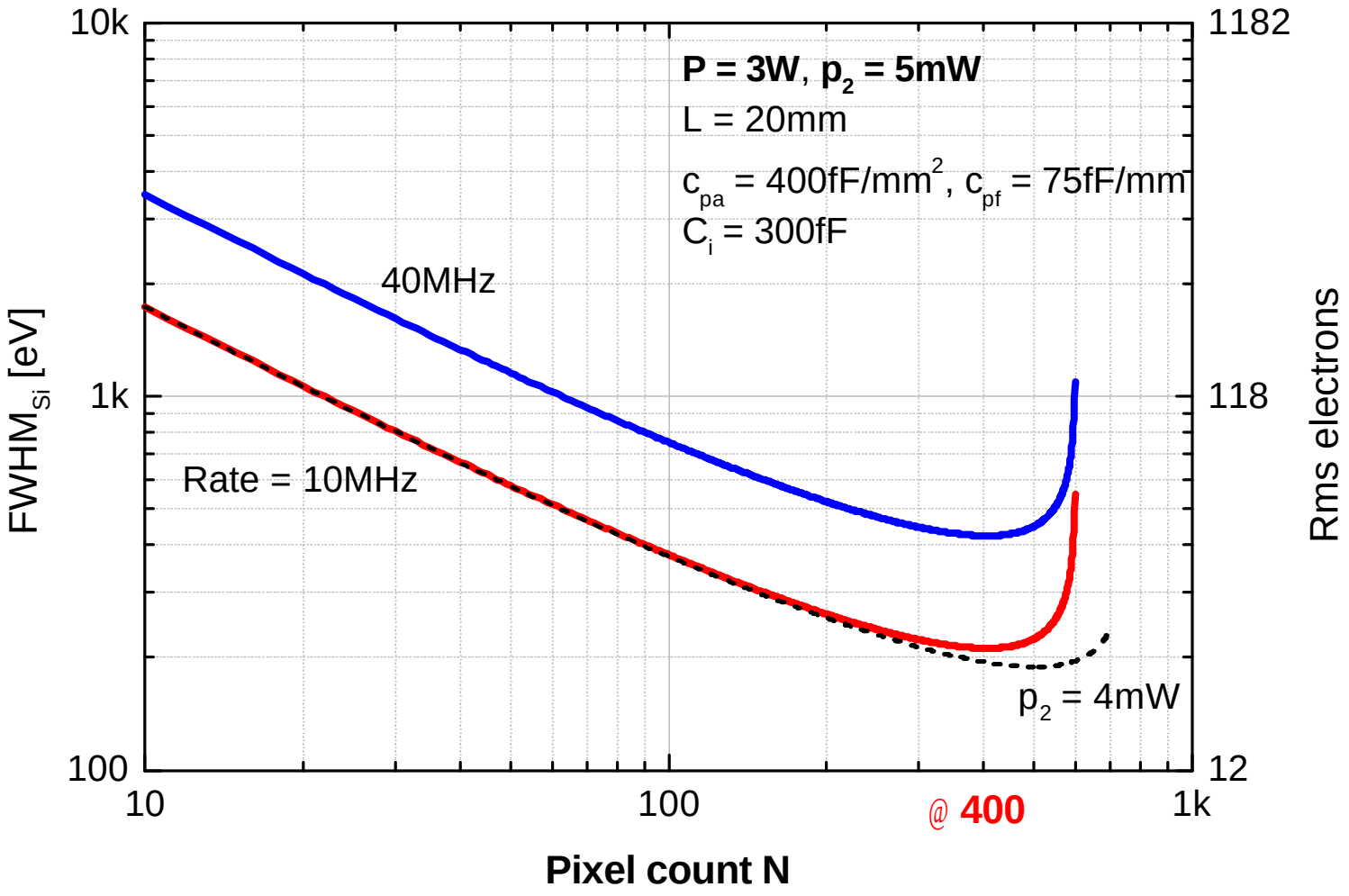
Optimum pixellation

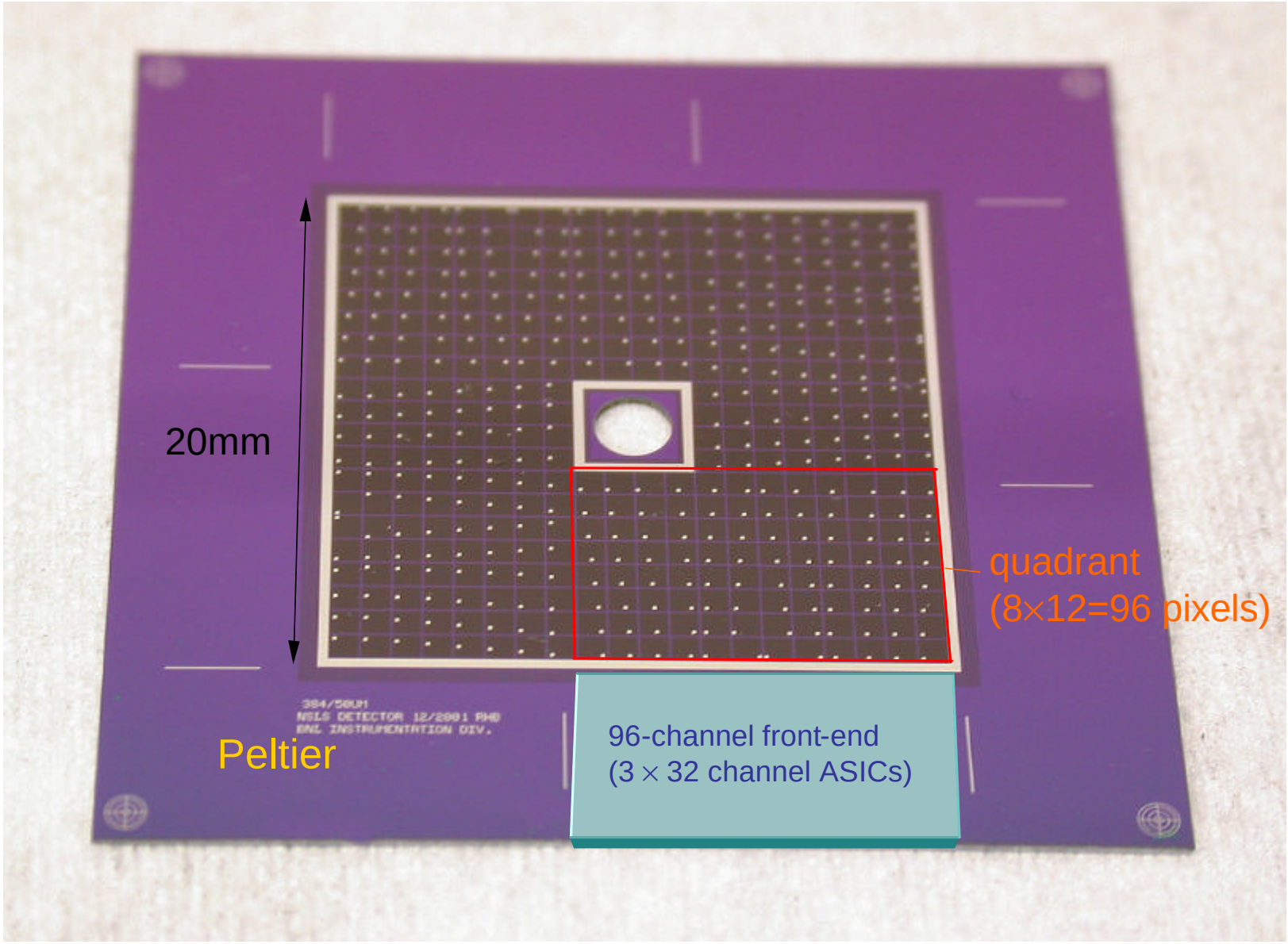


$$ENC^2 \div \left(C_p(N) + C_i\right)^{\gamma+1} \frac{\frac{\text{Rate}}{N}}{\left(\frac{P}{N} - p_2\right)^{\gamma}}$$

- charge sharing (≈20µm/side) and trapping (gap/side) : empirical

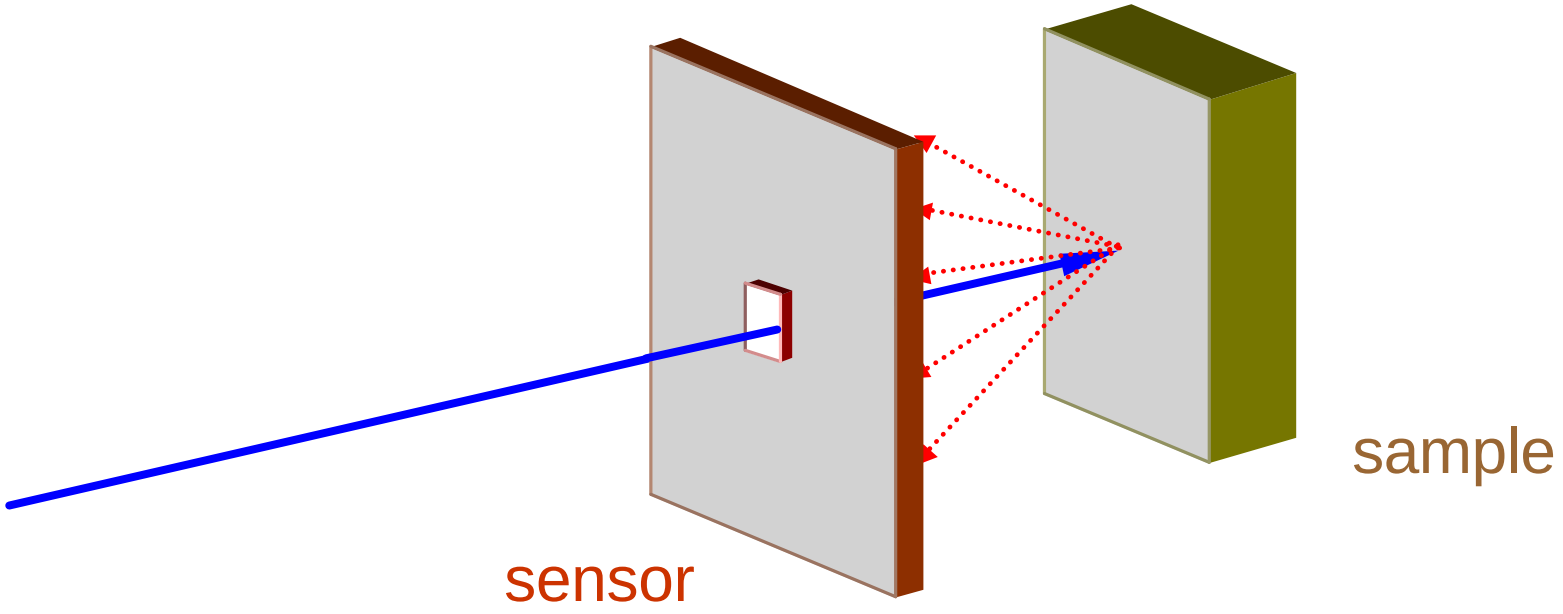
Optimum pixellation



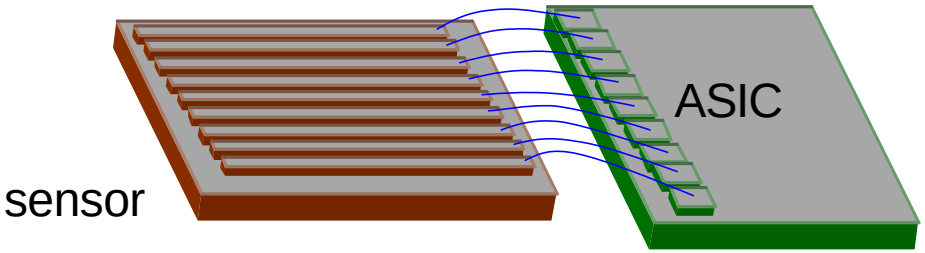


Si n-type high resistivity wafer 250µm thick,
N = 384 p^+ ≈1mm×1mm pixels, C_p ≈ 700-1000fF
gaps 10µm, 30µm, 50µm

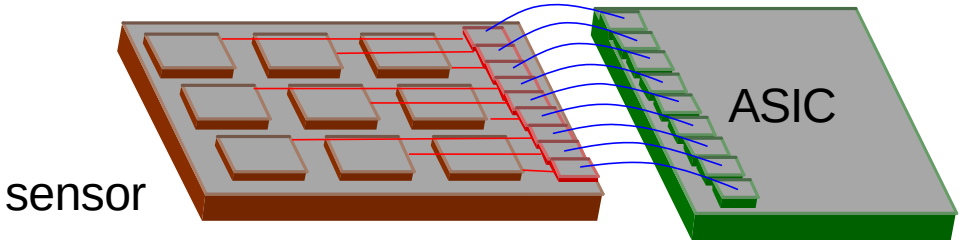
Beam through



Interconnecting pixel to front-end electronics

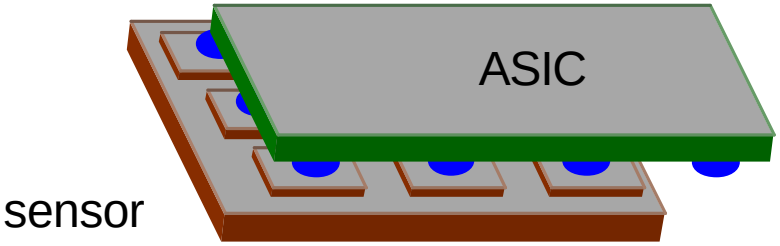


+ interconnect parasitic
+ bond length
- fringe capacitance
- charge sharing and trapping

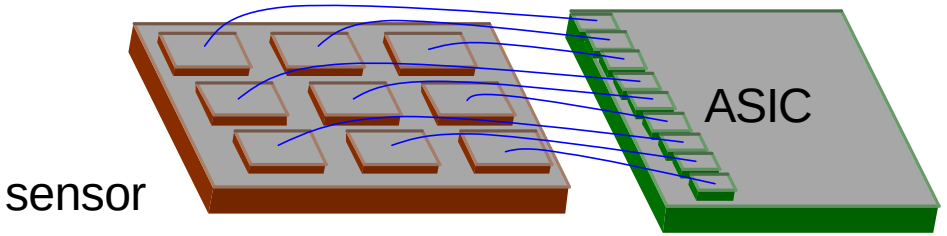


+ bond length
- interconnect parasitic
- dielectric losses

6mm×10µm, Si_3N_4 (ε_r=6.5,*tan(d)* ≈ 1m), 3µm, d**C_i**»**1.2pF**
d**$FWHM_{loss}$** = 8.5/q·√(2kTC_i*tan(d)*) » **180eV**

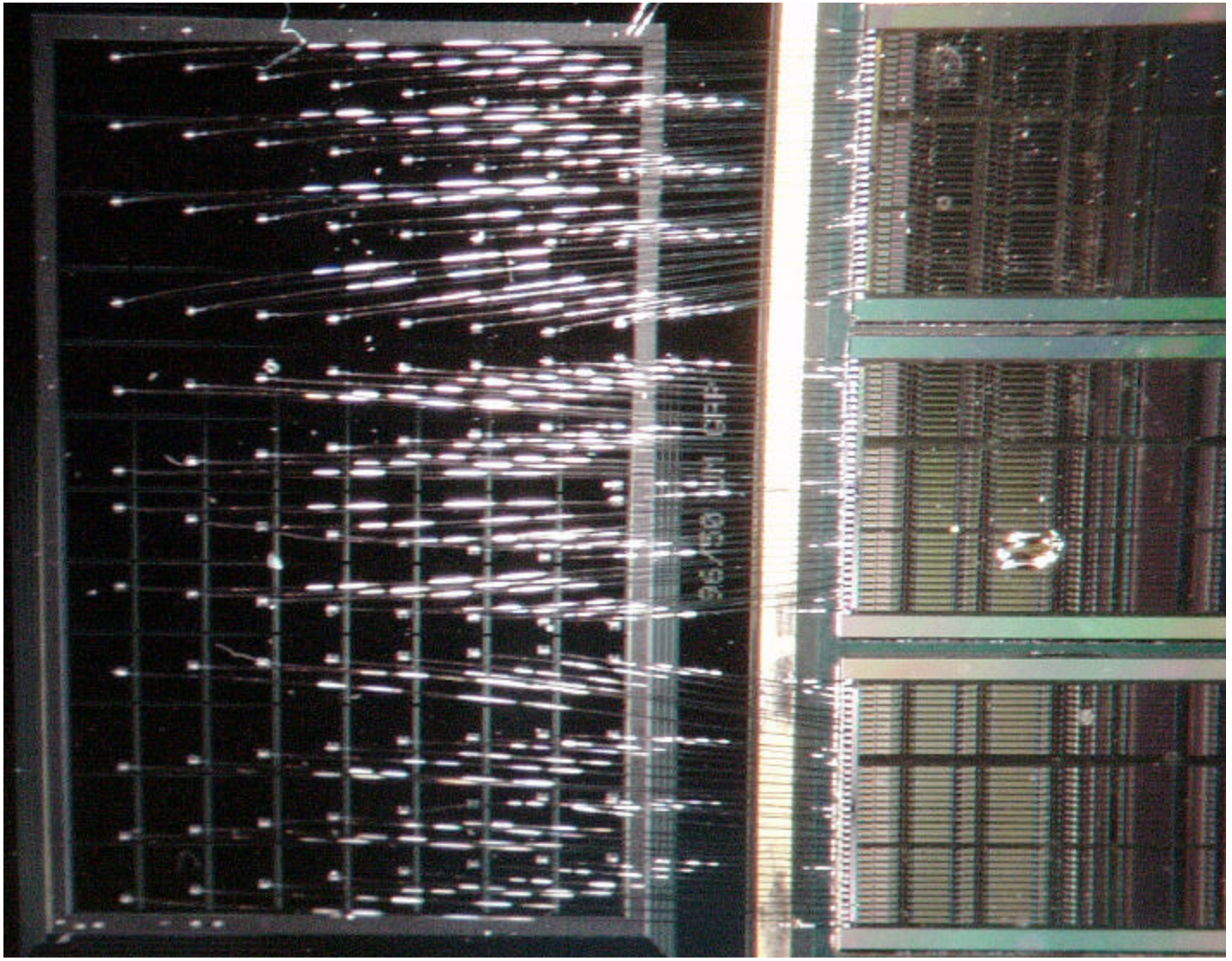


+ interconnect parasitic
- constraint on ASIC area and layout
- fluorescence from Pb (Sn/Pb/Ag)
- illumination from segmented side



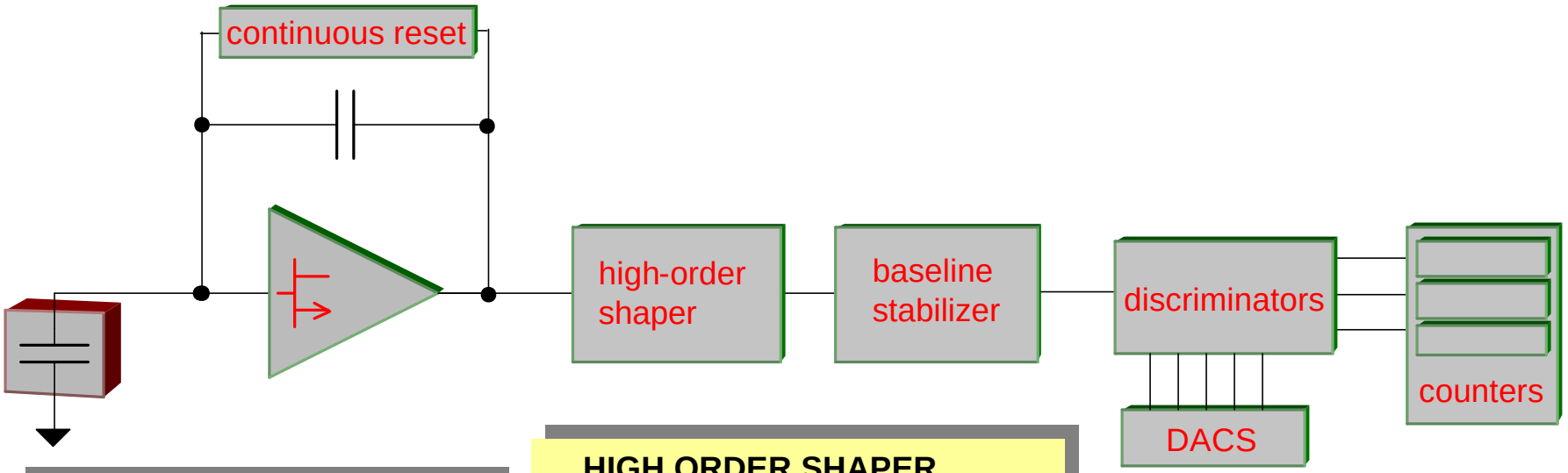
+ dielectric losses
± interconnect parasitic
- bond length

Sensor – ASIC photo



one quadrant

ASIC channel overview



INPUT p-MOSFET
- optimized for operating region
- NIM A480, p.713

CONTINUOUS RESET
- feedback MOSFET
- self adaptive 1pA - 100pA
- low noise < 3.5e$^-$ rms @ 1µs
- highly linear < 0.2% FS
- US patent 5,793,254
- NIM A421, p.322
- TNS 47, p.1458

HIGH ORDER SHAPER
- amplifier with passive feedback
- 5th order complex semigaussian
- 2.6x better resolution vs 2nd order
- TNS 47, p.1857

BASELINE STABILIZER (BLH)
- low-frequency feedback, BGR
- slew-rate limited follower
- DC and high-rate stabilization
- dispersion < 3mV rms
- stability <2mV rms @ rt×tp<0.1
- TNS 47, p.818

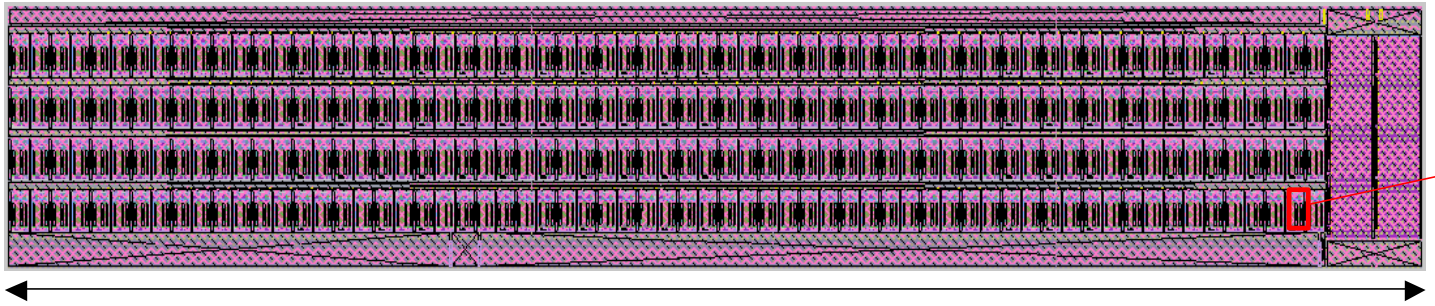
DISCRIMINATORS
- five comparators
- 1 threshold + 2 windows
- four 6-bit DACs (1.6mV step)
- dispersion (adj) < 2.5e$^-$ rms

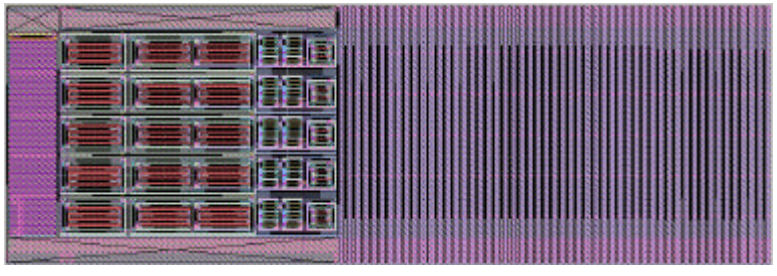
COUNTERS
- three (one per discriminator)
- 24-bit each

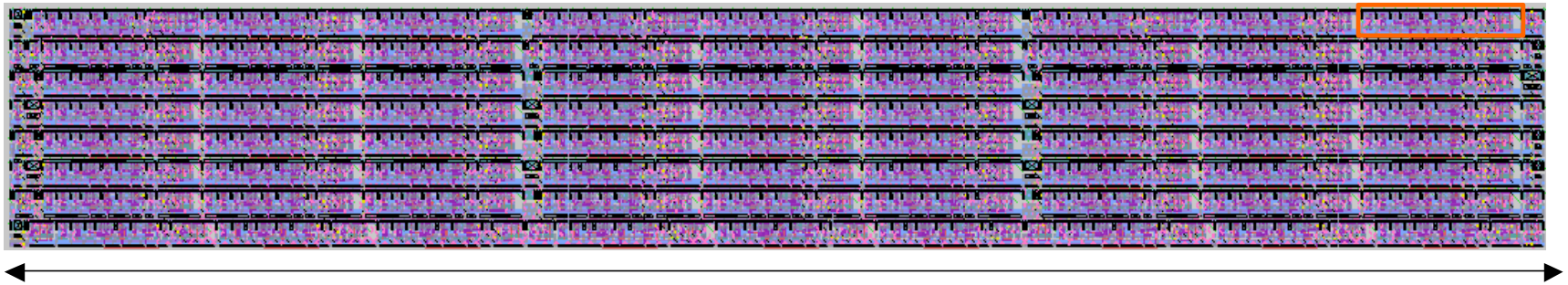
≈ 3 mW

≈ 5 mW

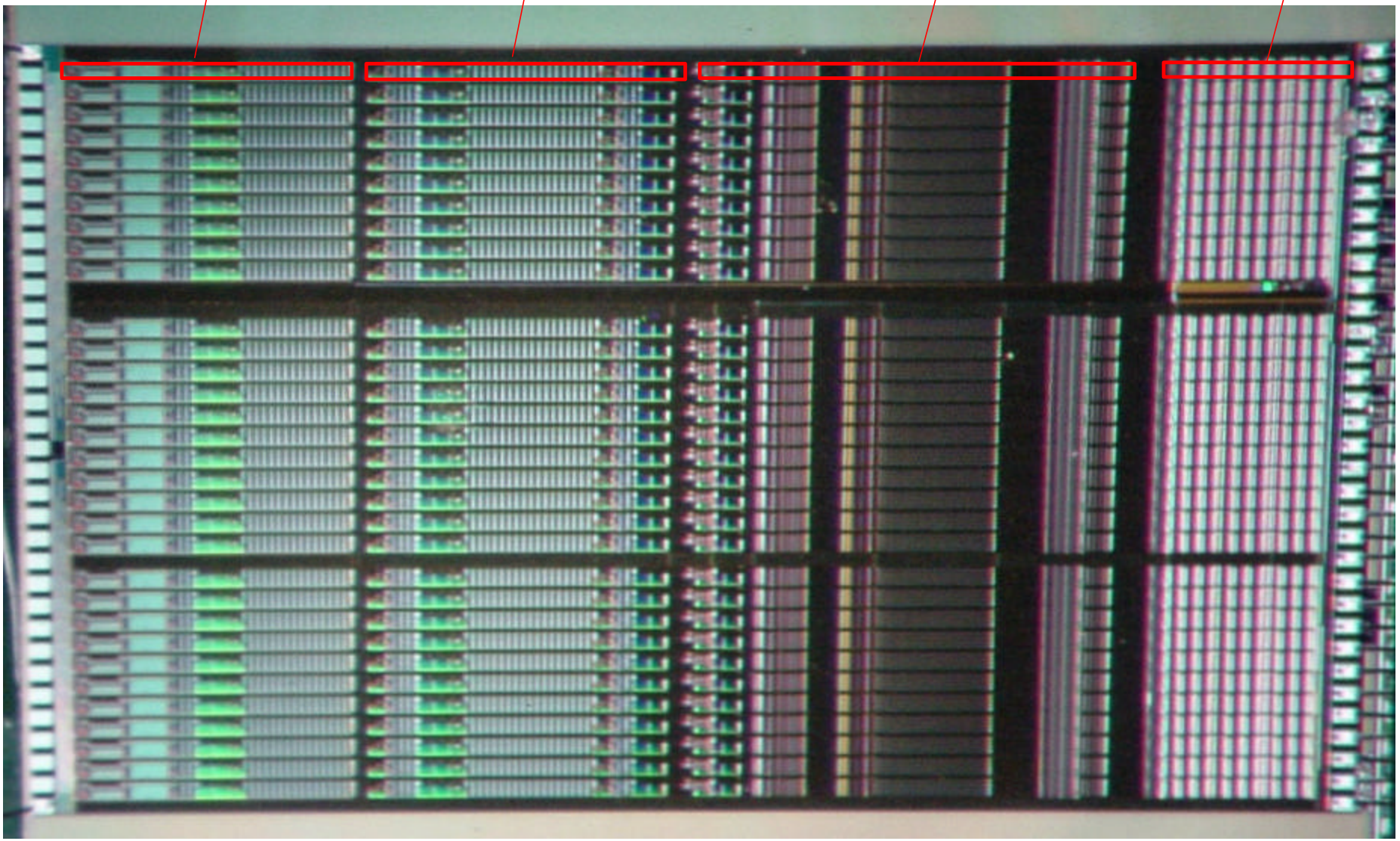
ASIC layout cells





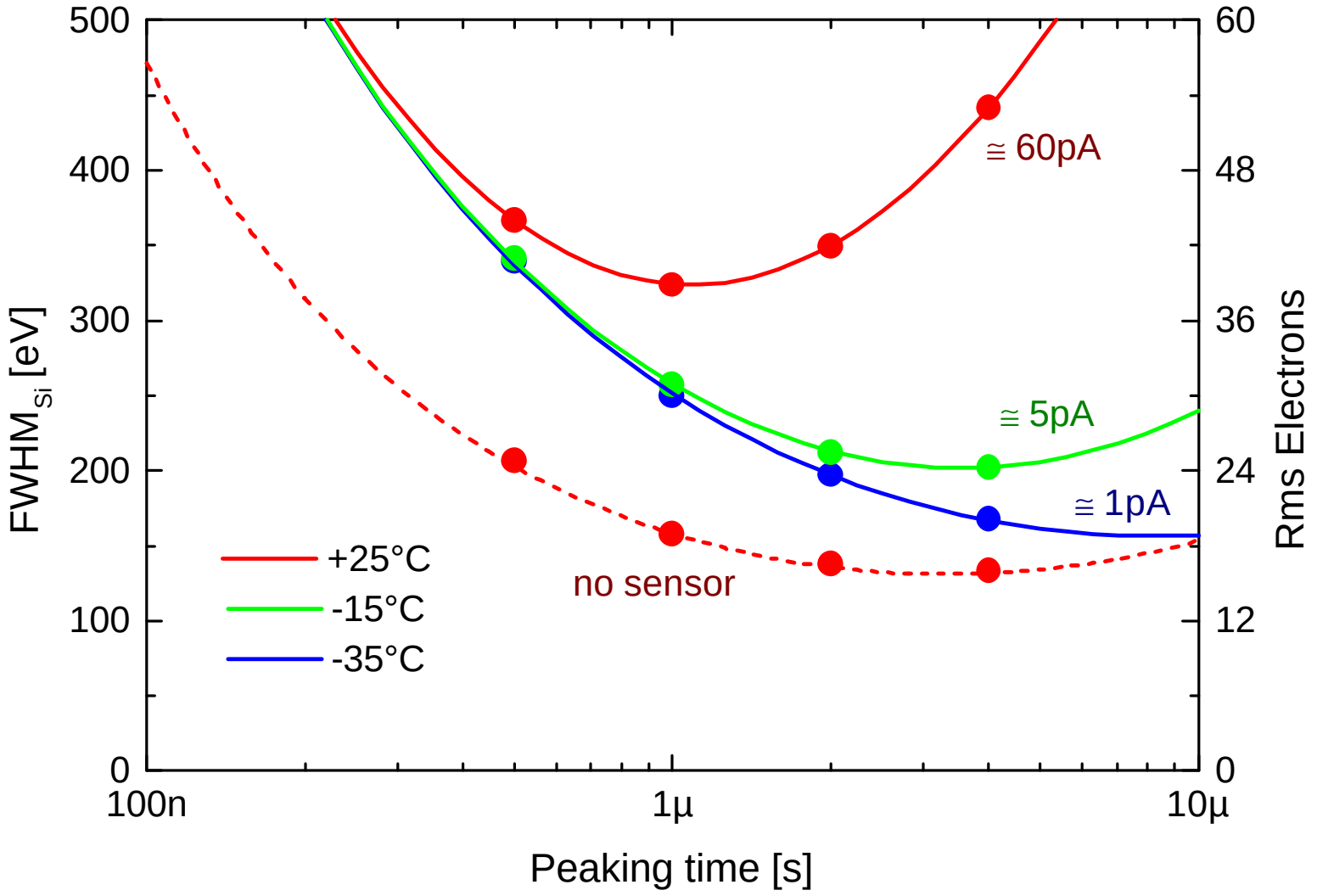


ASIC photo



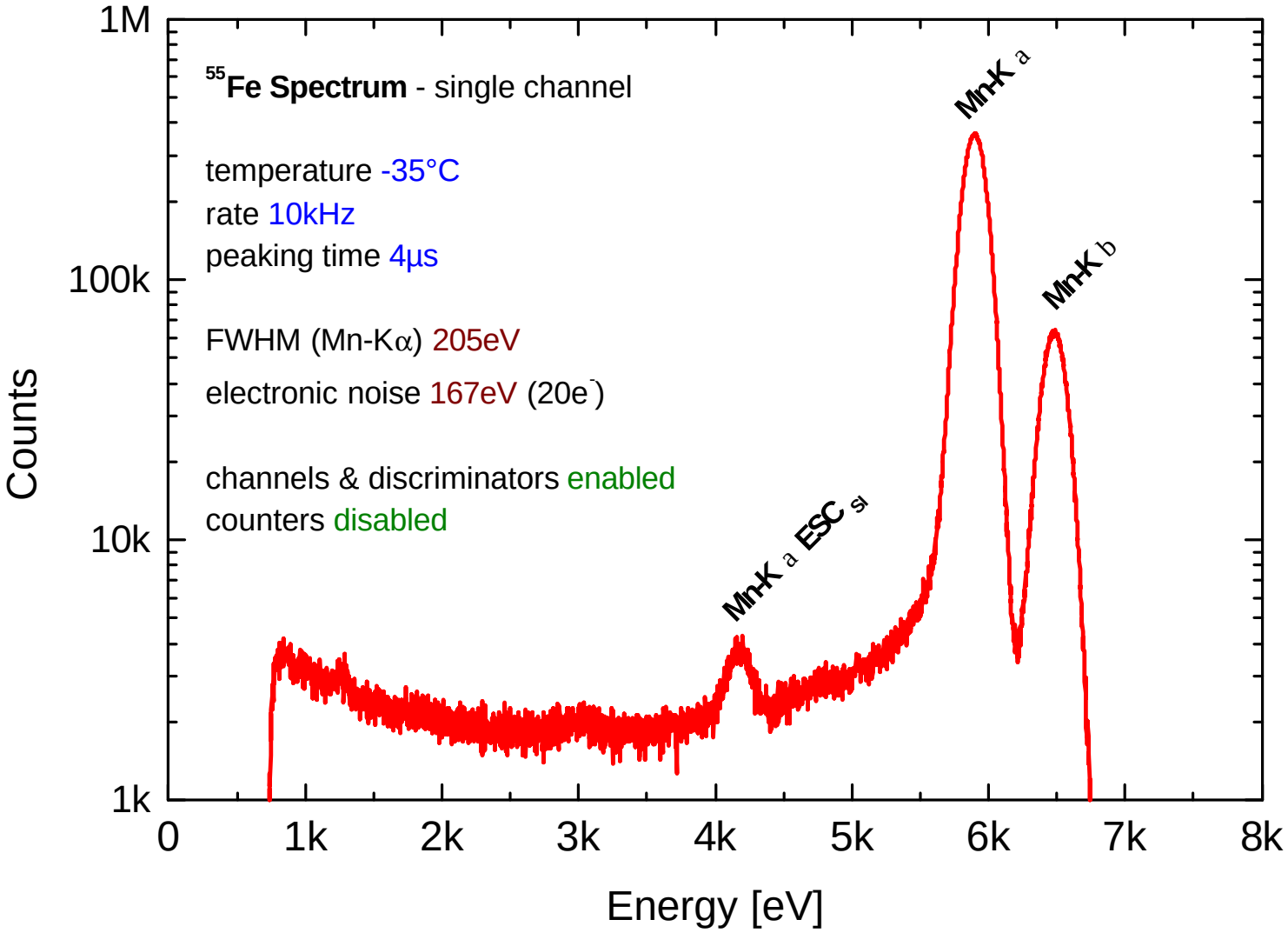
32 channels, 3.6 ´ 6.3 mm²

Measured resolution



50µm-gap, $C_p \approx 700fF$, $C_{i\text{-}bond} \approx 50\text{-}200fF$, $C_{i\text{-}pad} \approx 220fF$

^{55}Fe spectrum



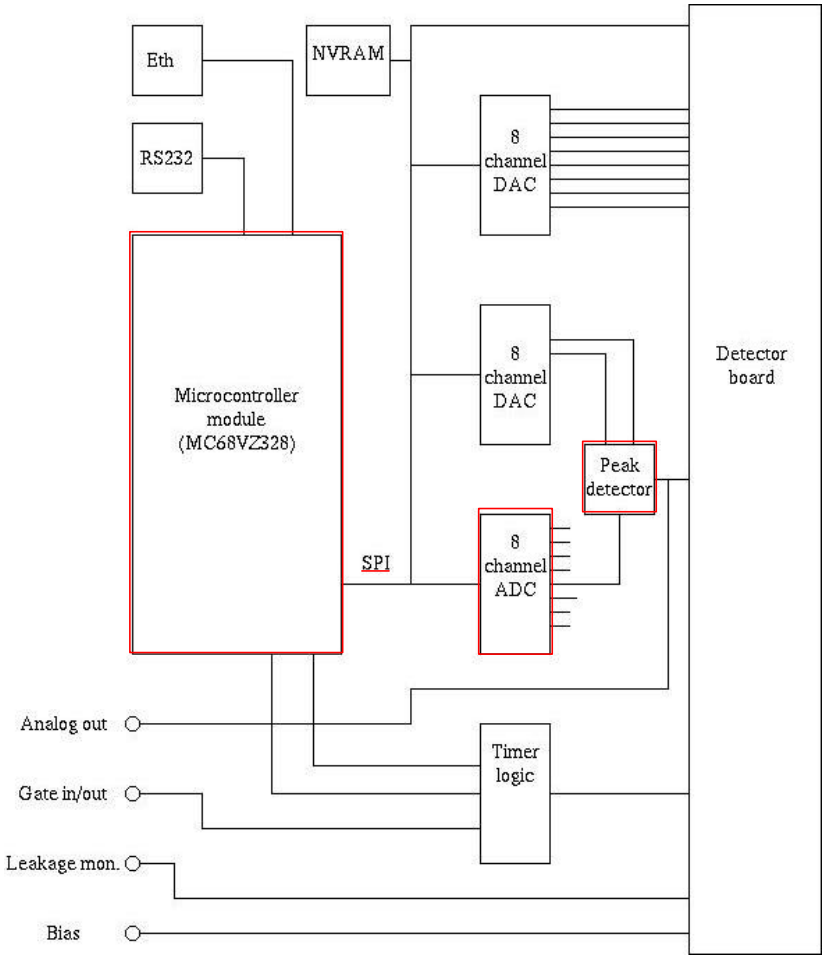
50µm-gap, $C_p \approx 700fF$, $C_{i\text{-}bond} \approx 50\text{-}200fF$, $C_{i\text{-}pad} \approx 220fF$

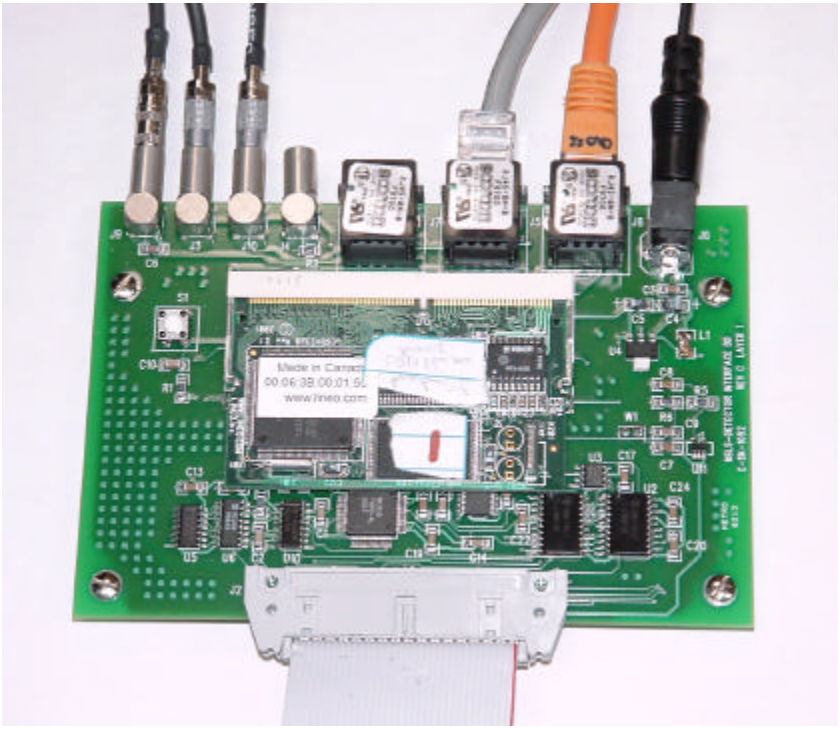
ASIC overview

Technology	CMOS 0.35µm 3.3V 2P4M
Size	≈ 3.6 × 6.3 mm^2
# MOSFETs	≈ 180,000
# Channels	32
power / channel	≈ 8 mW
# Discriminators	three / channel (1 thr., 2 win.)
threshold adjustment	four 6-bit DACs (1.6mV step)
threshold dispersion (adj)	≈ 2.5 electrons rms
# Counters	three / channel
bits per counter	24
Gain (settable)	750, 1500 mV/fC
Peaking time (settable)	0.5, 1, 2, 4 µs
ENC @ 1µs	≈ 14 + 12/pF electrons rms
ENC @ 4µs	≈ 11 + 6/pF electrons rms

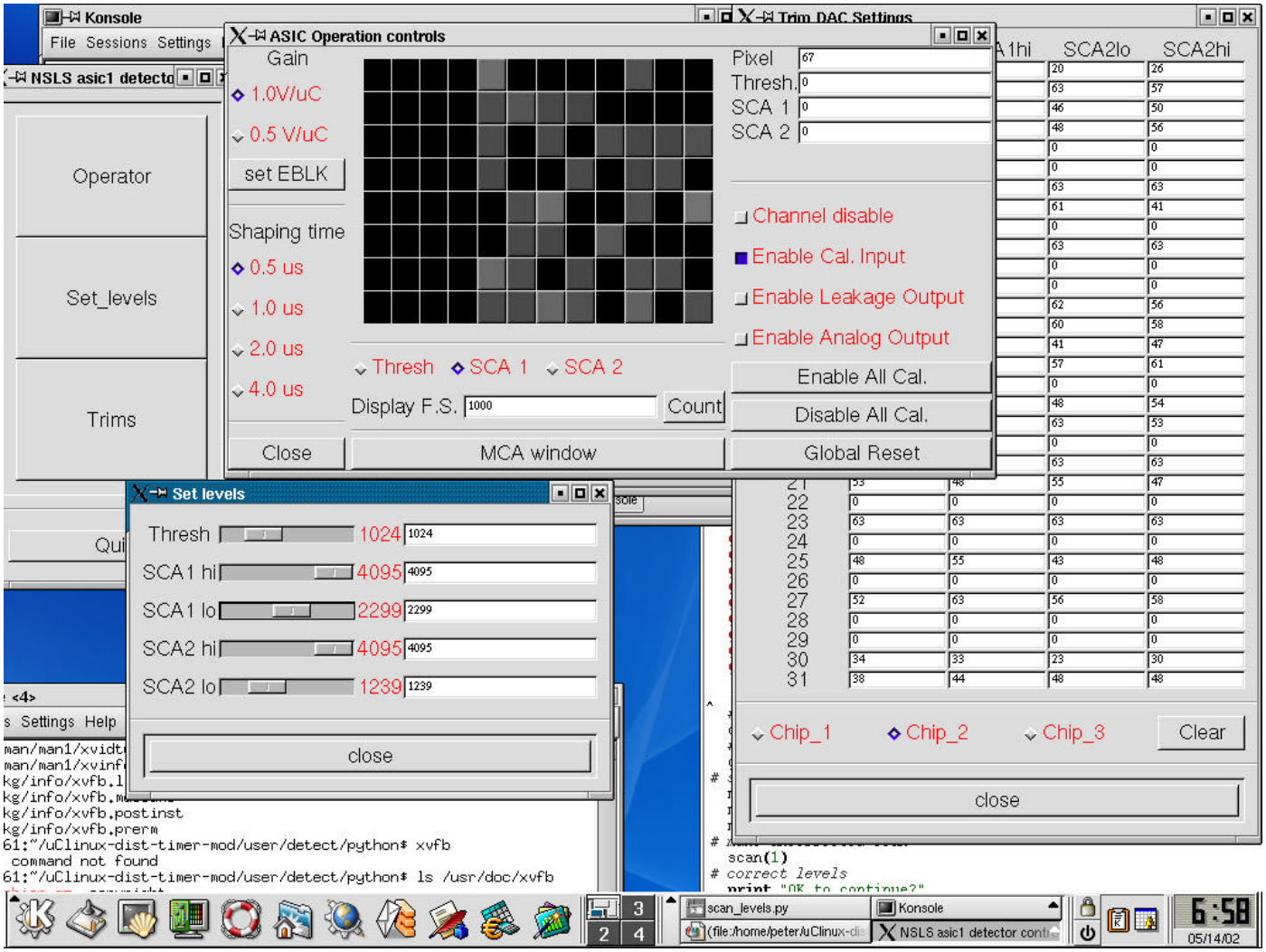
- self adaptive continuous reset
- high order shaper
- band-gap referenced output baseline
- output baseline stabilizer (BLH)
- test capacitors
- analog and pixel leakage monitors
- plug & play (fully self biasing)
- serial interface
    - counters readout
    - gain / peaking-time setting
    - monitors & test enable
    - channel masking
    - DACs setting
- token or chip-select mode

Readout

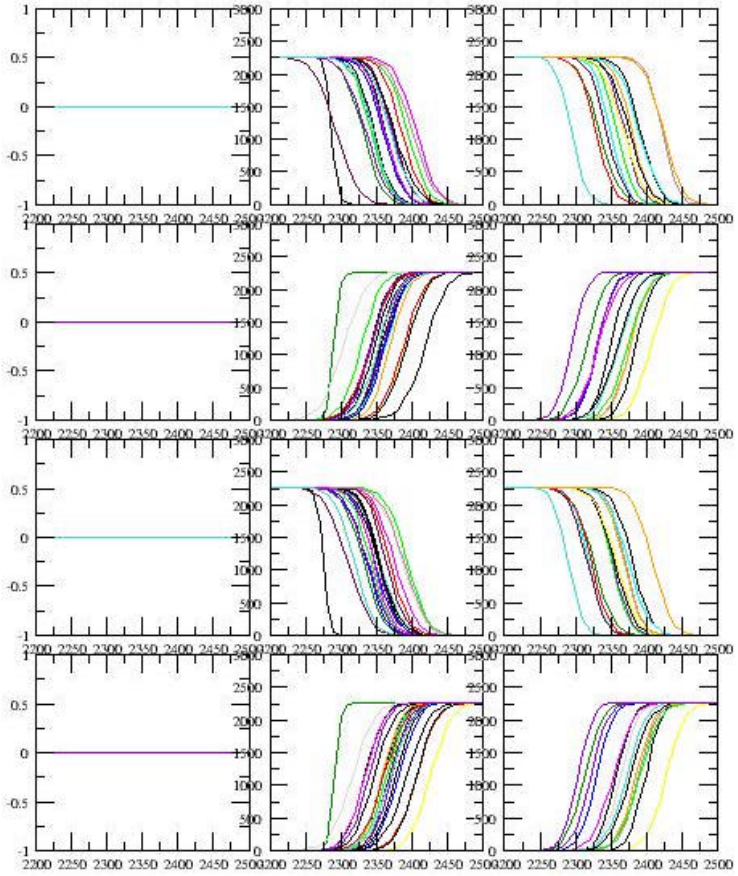

Eth
NVRAM
RS232
8 channel DAC
8 channel DAC
Microcontroller module (MC68VZ328)
Peak detector
SPI
8 channel ADC
Detector board
Analog out
Timer logic
Gate in/out
Leakage mon.
Bias



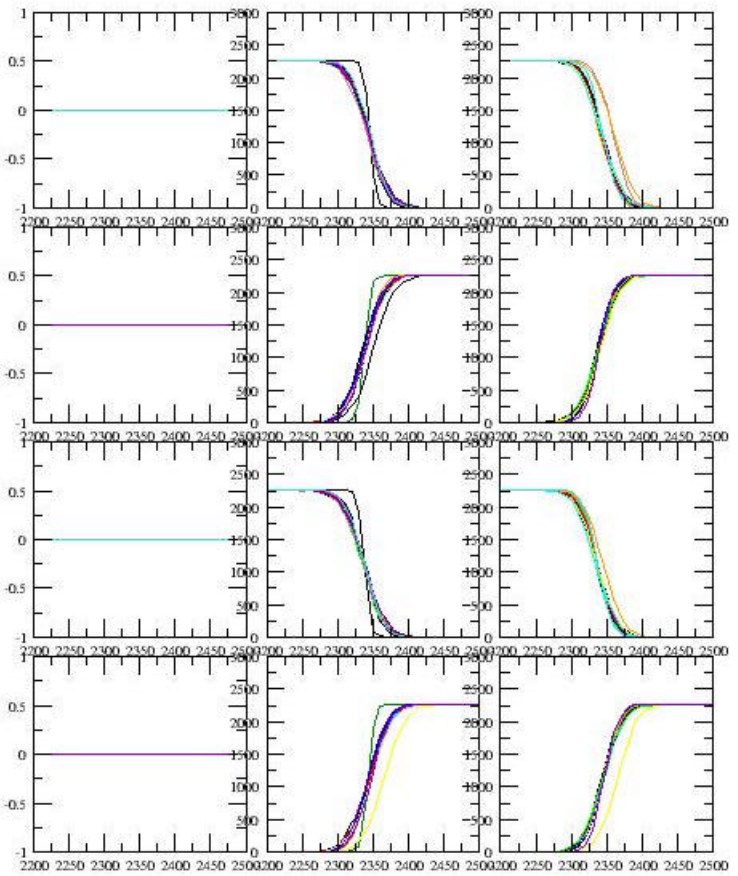
Readout interface



Automatic threshold equalization

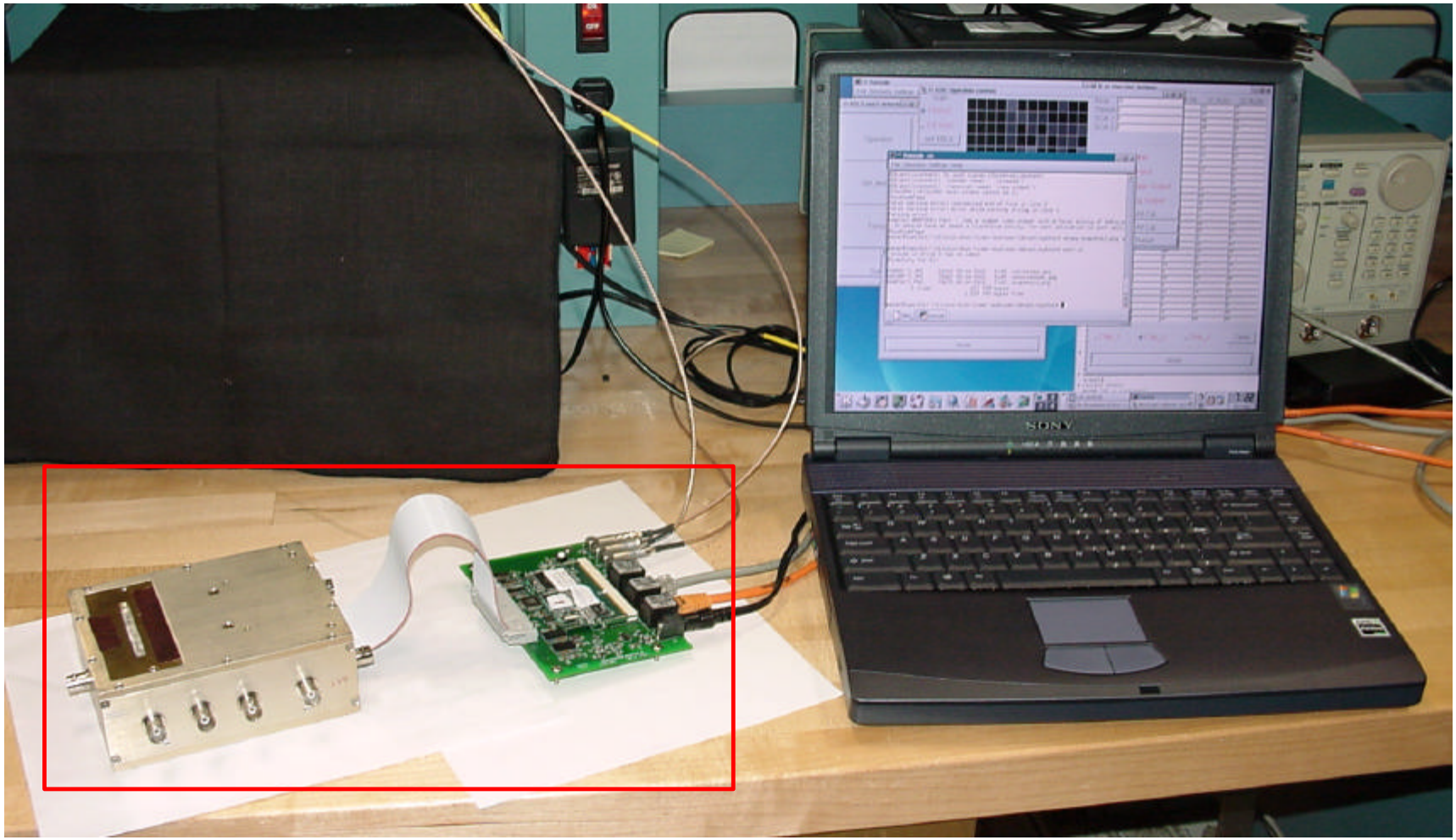


before correction $\sigma \approx 170e^-$ *rms*



after correction $\sigma \approx 2.5e^-$ *rms*

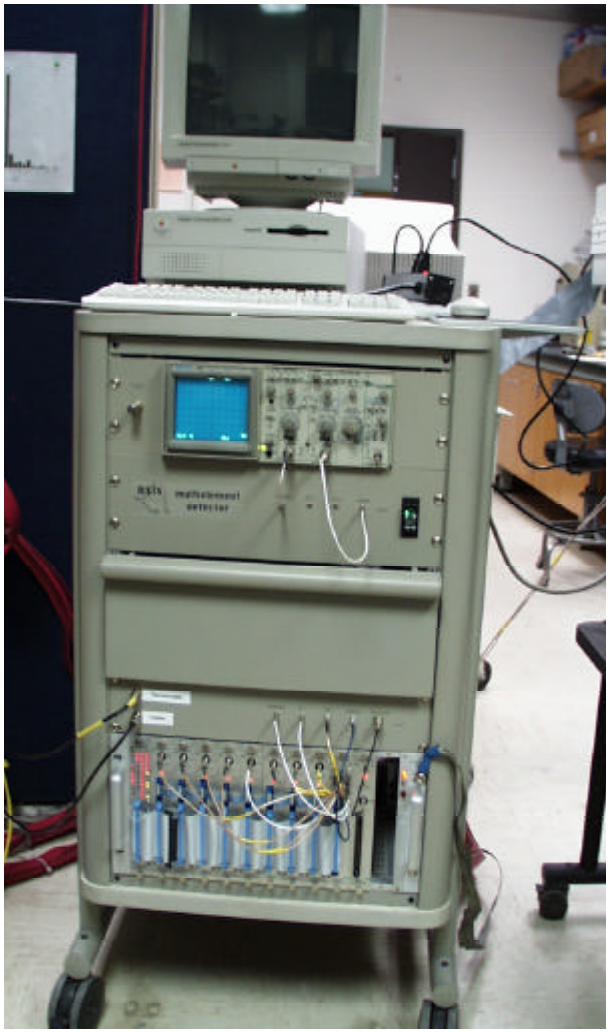
New EXAFS detector



» ***400 channels, < 300 eV, > 10MHz***

Current EXAFS detector

head - preamplifiers



rack – shapers …

» ***100 channels, > 350 eV, < 1 MHz***

Summary

New detector for EXAFS

- monolithic Si sensor, 400-mm^2 active area
- ≈ 400 1-mm^2 pixels
- 32-channel ASICs

First results (single quadrant)

- ENC ≈ 11 + 6/pF e^- rms @ 4μs
- FWHM < 300eV @ rate < 100 kHz/pixel
- threshold dispersion < 2.5 e^- rms

Future work

- one ASIC iteration
- pixel gap selection (10, 30, 50 μm)
- Peltier cooler assembly / test
- four quadrant (12 ASICs) assembly / test
- on-field test at NSLS (BNL)