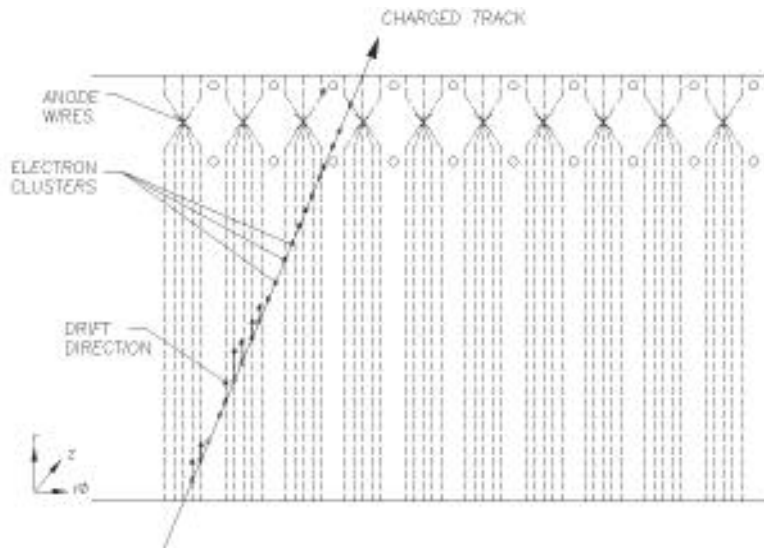


PHENIX TEC

LOCATION:

- between RICH and EMCAL ($4.05\text{m} < R < 4.85\text{ m}$)



GOAL:

- Electron/pion separation by fine sampling energy loss (dE/dx)
- Upgradable to TRD

ELECTRONICS CHAIN:

Anode wires -- PS -- FADC -- DMU

(octal)-(single)-(quad)

30,000 3750 30000 7500

- TRD capability already designed in to electronics.



TEC Preamp Shaper ASIC (TEC PS)

Design and Test:

P. O'Connor, A. Kandasamy, BNL

Function:

Preamplify and shape charge on anode wires

Provide separate outputs for dE/dx and TR signals

Core Circuit:

Transimpedance Preamplifier (75K)

Unipolar, 70 nsec, CR-RC⁴ shaper with Ion Tail Cancellation

Active Baseline Restoration

Split gain stage: 1X, 5X

System Interface Features:

Digitally Selectable Gain, Peaking Time, Tail Cancellation

Individual Channel Injection Capacitor & Switch

Individual Channel Disable

Chainable, 3-Wire Serial Interface

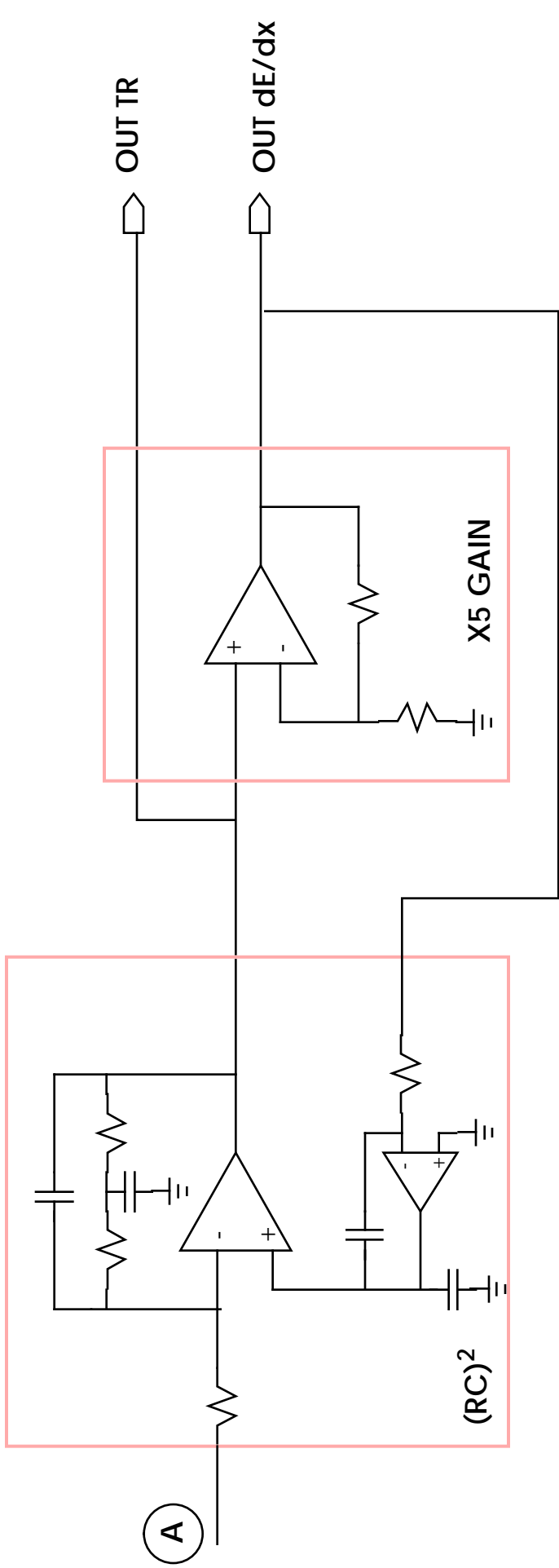
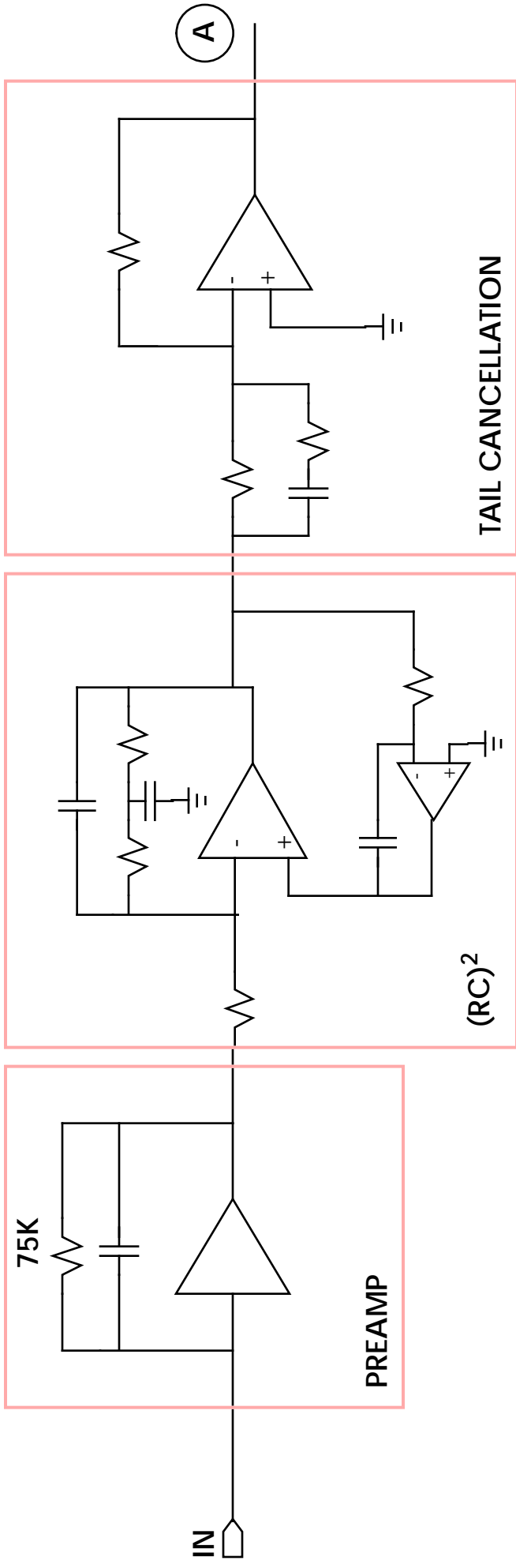
Other:

Die Size: 3.5x5mm

Power Dissipation: 350 mW

Package: 64 PQFP (proposed)





TEC PS Development Plan

1st Prototype:

- Delivered 4Q '95
- Verify preamp and shaper stage design only

2nd Prototype:

- Delivered 4Q '95
- 8 channel chip with full system interface
- Extensive bench testing (162 channels)
- Beam test April '96 (32 channels)

3rd Prototype:

- Delivered Nov. '96
- Minor design modifications to Prototype 2
- PQFP package trial
- To be used in chain tests Dec. '96 - Feb. '97
- 400 channels available
- Option to purchase 400 additional channels for 1/4 price

Development complete

- (pending results of Spring '97 chain test)



TEC PS Performance Results

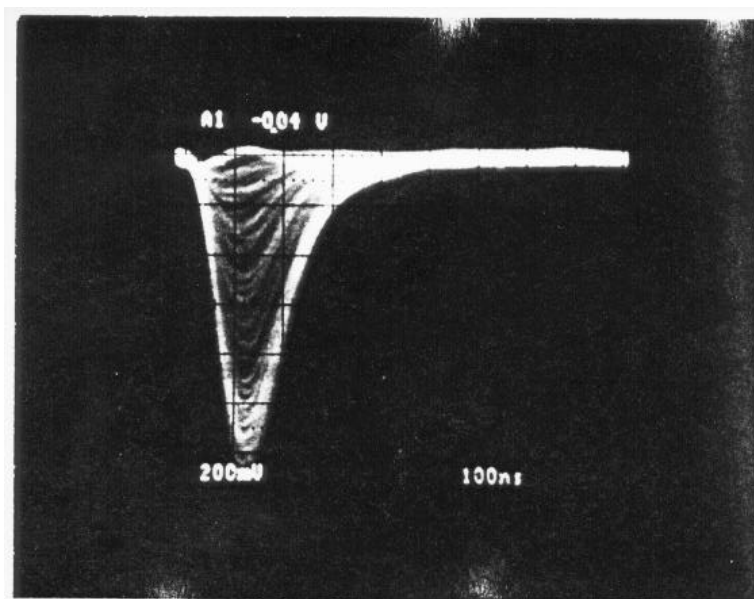
1st Lot ChipTest Results:

18/25 chips tested.

Each is 9-channel preamp/shaper with 2 outputs (X1, X5 gain.)

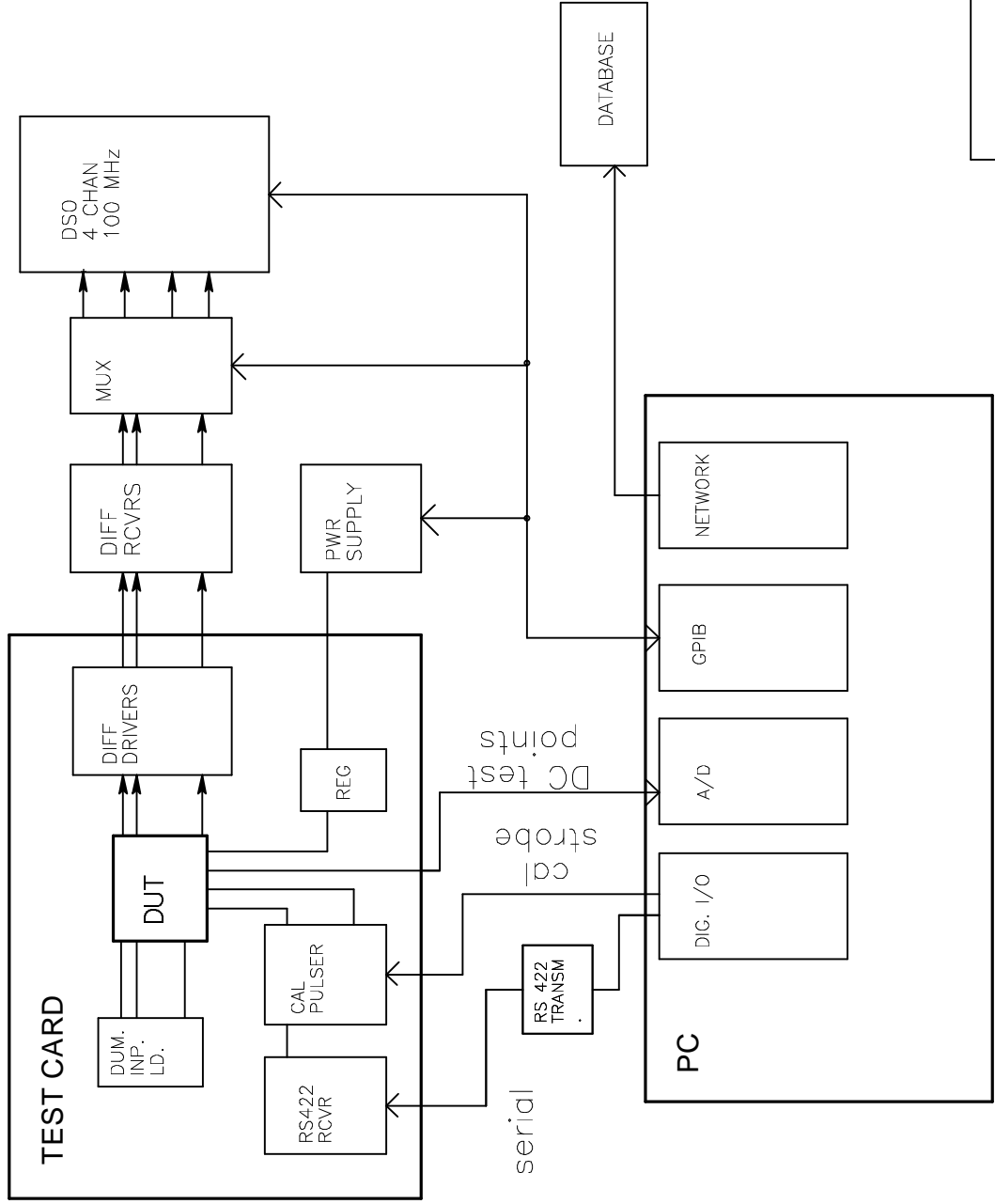
- 321/324 outputs OK
- Bad outputs attributed to wirebond failures
- All other channels completely functional and in spec:

	MEAN	ST. DEV.
Gain	21.3 mV/fC	2.2%
Peaking Time	74.3 nsec	2.2%
Offset	-66 μ V	1.4 mV
Noise @ 18 pF	1260 e ⁻	--



⁵⁵Fe Source
1m chamber





BROOKHAVEN NATIONAL LABORATORY

TEST SET FOR TECP S ASIC

B 1 / 1

DRAWN 11/19/1996

POC

TEC PS Test Strategy

- classify failures in prototype runs
- look for DC signatures which correlate

Plan for manufacturing test:

- | | |
|-----------------------|---------------------|
| • Wafer probe DC only | FOUNDRY |
| • Package | FOUNDRY OR PACKAGER |
| • Chip test AC + DC | COLLAB. |
| • Burn-in (?) | |
| • Assemble PCB | CONTRACT ASSEMBLER |
| • Board Test | COLLAB. |

Test Sequence:

1. Apply power, monitor DC currents, DC bias voltages, output + input DC levels
2. Test serial interface
3. Functional test all channels
4. Loop over channels

 Loop over configurations (gain, pk. time, tail cancellation)

 Download configuration

 Pulse 100X

 Measure gain, pk. time, noise (?)

 Next configuration

 Next channel

5. Write record to database

6. Barcode

Estimated total time: 2 - 3 minutes

Total time to test 3750 chips @ 70% yield + 10% spares: 25 8-hour days

Status:

- Wafer test vendor not yet selected; quotations requested
- Test hardware: 80% exists, some development needed
- Code fragments (VB) exist for multichannel gain, pk. time, noise measurement
- Manpower needed for software development



TEC PS Manufacturing Plan

FOUNDRY:

- HP (AMOSI, CMOS34) = 1.2 micron nwell CMOS, linear capacitor, double metal, single poly

"Preproduction" Order 5/97:

- for 11/97 sector test - approx. 500 chips needed

Logistics of preproduction:

MPW

\$420/mm²/lot of 25 chips

\$320/mm²/extra lot of 25

$(\$420 + \$320 \times 19 \text{ lots}) \times 17.5\text{mm}^2 = \114K

PRODUCTION

Chips/6" wafer ~ 500

Min. order 3 wafers (\$64K)

- Retain tooling, spares for full production starting 11/97 (pending successful sector test)
- Full production requires 12 wafers (18 wafers for 6-plane) assuming 70% yield and 10% spares

NOTE: Process to be phased out 3/98 TEC PS

Remaining effort:

- * Verify final design in chain and beam tests
- * PQFP package
- * Complete test H/W, S/W
- * Finalize procurement



TEC FLASH ADC ASIC (TEC FADC)

Design and Test:

Joe Harder, BNL

Function:

Digitize pulse height from dE/dx and TR channels of TEC PS

Encode into 5-bit word at 40 MSa/s

TEC FADC Development Plan

- Prototype History:
 - 3 Prototypes delivered in '94 (2.0 micron CMOS)
 - First 1.2 micron prototype early '95
 - Second '95 prototype added TR channel, has linear dE/dx range
- Final design produced Summer '96 with nonlinear dE/dx
- Bench tested
- Final package chosen and prototyped
- Crude preamp/shaper - driver - receiver - FADC demonstration
- 8 devices available now + 40 older devices (linear dE/dx levels)
- Chain test/beam test Jan. '96 with TEC PS
- 150-300 nonlinear devices will be ordered for April '97 Chain Test. (\$100/chip)

DNL < 0.1 LSB



TEC FADC Test Strategy

- - **No wafer test** -
- Package
- Chip test AC + DC
 - First 1000 to be tested in-house
 - Remainder to be contract tested
- Cheap plastic pkg, small die => minimal impact of omitting wafer test

Status:

- Test hardware exists
- Labview software in development
- Contract test vendor not yet identified



TEC FADC Manufacturing Plan

FOUNDRY:

- Orbit 1.2 micron nwell CMOS, double poly, double metal

PACKAGE:

- 24 SSOP, Azimuth (Taiwan) or Emmanuel (Calif.)

"Preproduction" Order 5/97:

- for 11/97 sector test
- approx. 4000 chips needed
- Logistics of preproduction:
 - 25 wafers/boat; Min. order 10 wafers (5 good guaranteed)
 - 1800 die sites/wafer, assume 60% yield => Need 4 wafers for sector test
 - Retain tooling, spares for full production starting 11/97 (pending successful sector test)

Full production

- Need additional 50 wafers (fixed lot size)
- Expect 40 good
- 84K die produced from 40 wafers
- Should satisfy all PHENIX needs if yield > 50%
- Total fab cost: \$84K
- Assume \$0.75 to package and test a die => \$63K for 84K packaged chips
- Total cost: \$181K, cost per channel \$3.59



TEC Digital Memory Unit ASIC (TEC DMU)

Design:

J. Gannon, Sy Rankowitz, BNL; R. Sundblad, SICON

Purpose:

Buffers data out of FADC for Level 1 latency

Contains 5 event FIFO memories

4 channels/chip

Programmable delay/event length

Test data input

Specs:

Minimum clock period	25 ns
Power Consumption	50mW (data collection) 0.75W (readout)
Memory Delay Length	1 to 190
Event Length	2 to 80



TEC DMU Development Plan

SiCon chips in PGA completed fabrication Summer '96

5 chips tested at SiCon and delivered to BNL

100 additional chips in PQFP awaiting test

To be bench tested in motherboard at BNL Dec. '96

Chain test April '97

TEC DMU Test Plan

All chip testing to be done by SiCon

TEC DMU Manufacturing Plan

Production Order: 5/97

Foundry: AMS

Need 8000 die + yield

Packaged die delivered 12 weeks after fabrication start

Total cost: \$350K including full production

\$200K from Swedish government

