Charge Preamplifiers in Scaled CMOS

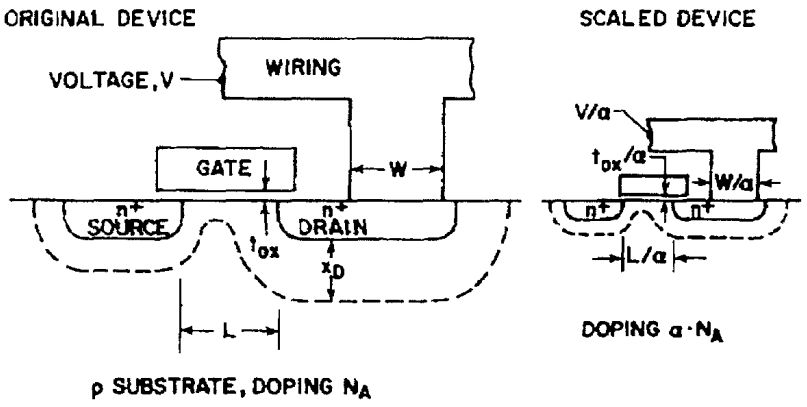
- **Digital CMOS Scaling**
- Charge Amplifiers
- MOS Noise Sources
  - series
  - parallel
- Analog-Digital coexistence
- Limits, Future Scenarios

CMOS Scaling

Driven by digital VLSI circuit needs

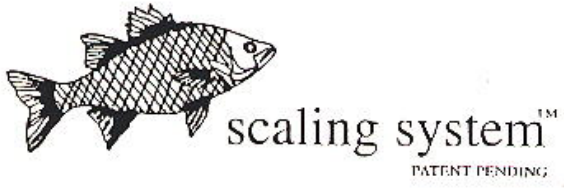
Goals: in each generation

- **2X increase in density**
- **1.5X increase in speed**
- **Control short-channel effects, threshold fluctuations**
- **< 1 failure in 10^7 chip-hours**

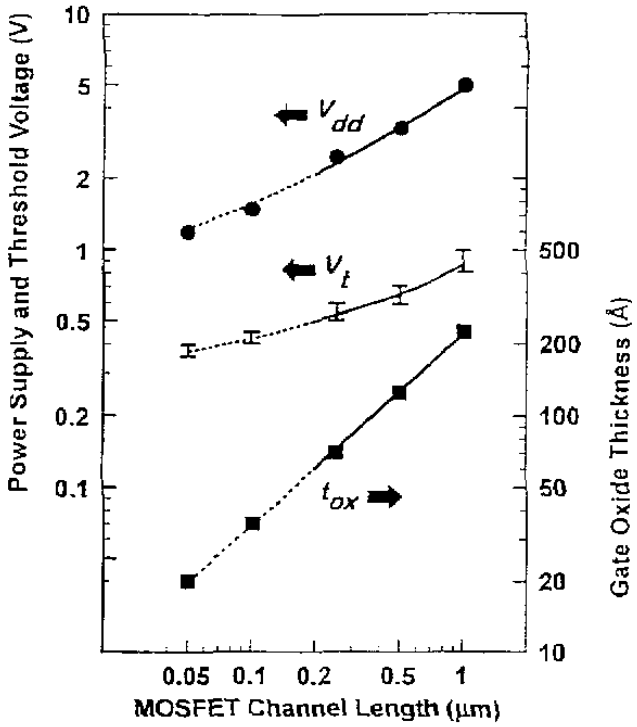


Rules:

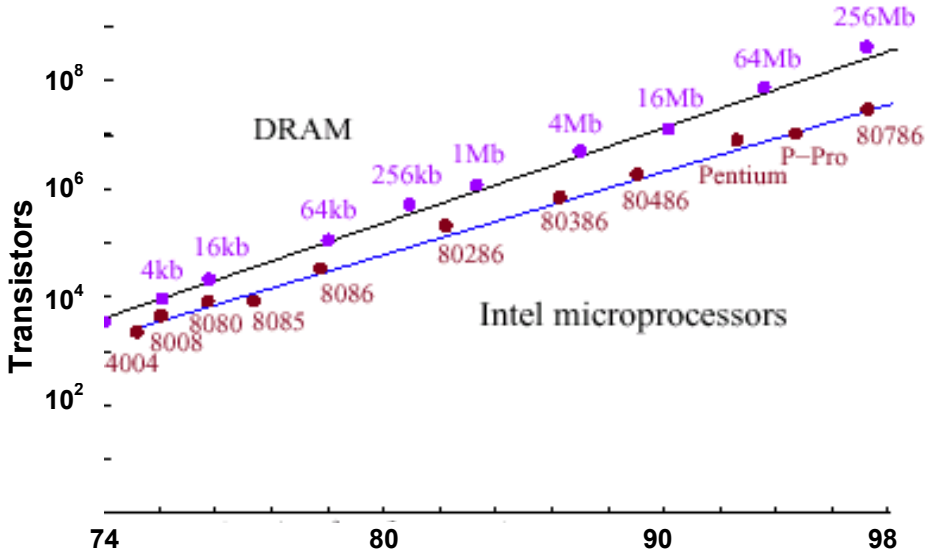
- all dimensions scaled by factor λ
- electric field kept constant by reducing voltages
- doping density increased



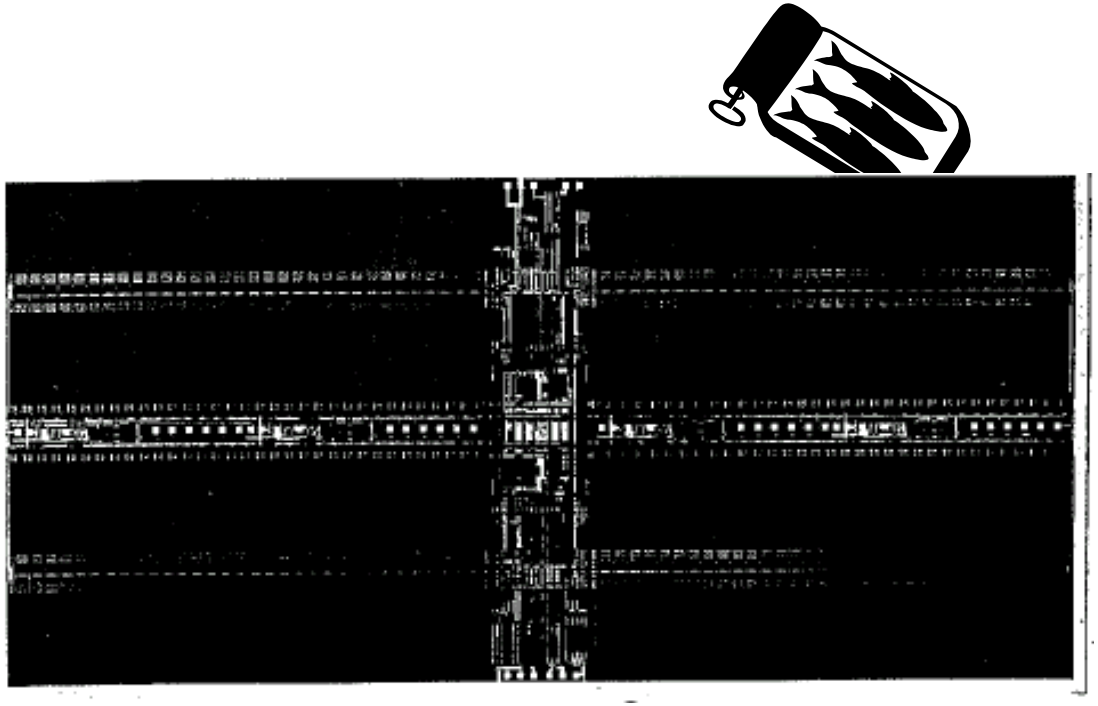
Technology Roadmap



Year	1997	1999	2001	2003	2006	2009
Feature size (μm)	0.25	0.18	0.15	0.13	0.10	0.07
Supply (V)	2.5	1.8	1.6	1.5	1.2	0.9
Tox (nm)	5.0	4.0	3.3	2.8	2.2	2.0
Vth (mV)	500	470	440	420	400	370
Nsub (10^{16}/cm^3)	3.4	5	6	7	10	20
Xj (μm)	0.1	0.07	0.05	< .05	<.05	<.05
10^6FETs/cm^2	8	14	16	24	40	64
Interconnect (meters/chip)	820	1500	2200	2800	5100	10000



Memory Scaling



2b
2.3 mm^2
1960s

64Kb
26 mm^2
1980s

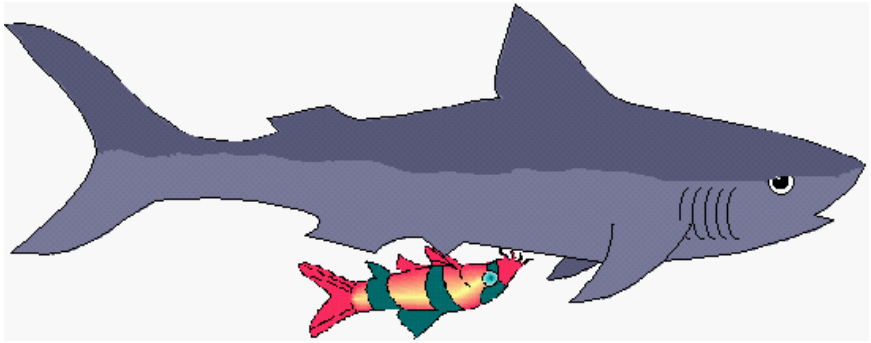
64Mb
198 mm^2
1990s

Analog Design in Digital CMOS Technology

- **Supply voltage is reduced with every generation**

  Reduced output dynamic range
  Restricted use of cascode structures

- **Reduced device gain g_m/g_d**
- **Poor quality passive components**
- **Poor models**
- **Digital crosstalk**



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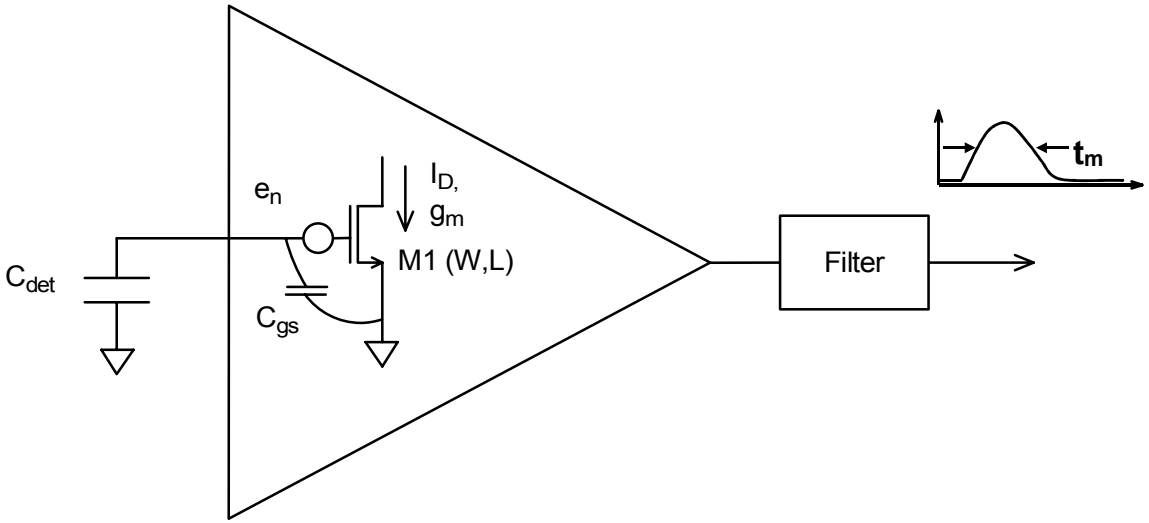
Charge Amplifiers - Review

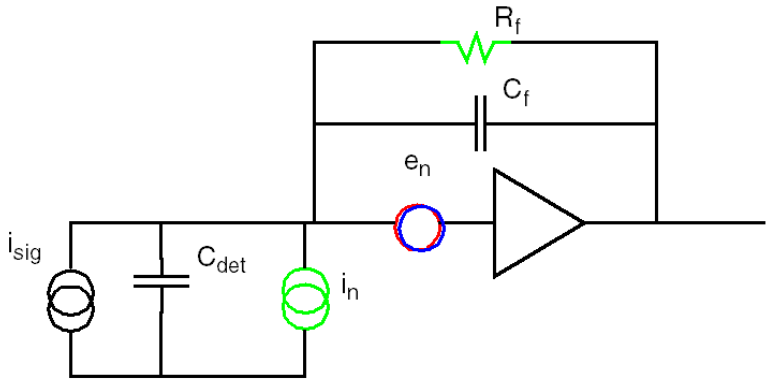


Input: charge pulse from capacitive source

Output: filtered voltage pulse

System noise is dominated by the input transistor

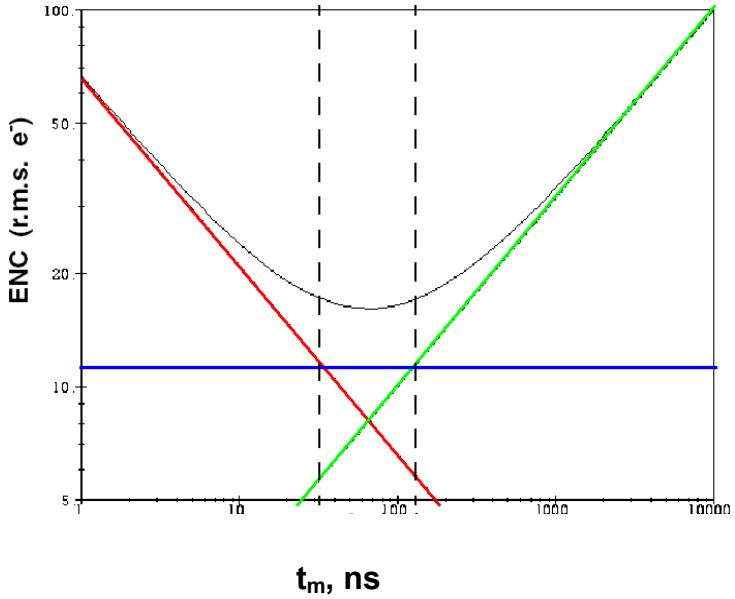
Equivalent Input Noise Charge (ENC)



$$C_{tot} = C_{\det} + C_{gs}$$

$$ENC^2 = \frac{a_1 e_{nw}^2 C_{tot}^2}{t_m} + a_2 \frac{K_F}{C_{gs}} C_{tot}^2 + a_3 i_n^2 t_m$$

$$e_{nw}^2 = 4kTR_s \qquad i_n^2 = \frac{4kT}{R_f} + 2qI_{leak}$$



Scaling and Charge Amplifiers

Technological trend	***Effects***	
increased f_T	series noise	+
shallow S/D junctions; LDD structure	series noise	-
excess thermal noise from hot carriers	series noise	-
velocity saturation	series noise	-
reduced supply voltage	dynamic range	-
	excess current source noise	-
	radiation tolerance	+
new gate dielectric	1/f noise	-
hot carrier stress	1/f noise	-
reduced oxide thickness	parallel noise	-
	radiation tolerance	+
reduced Vth	parallel noise	-

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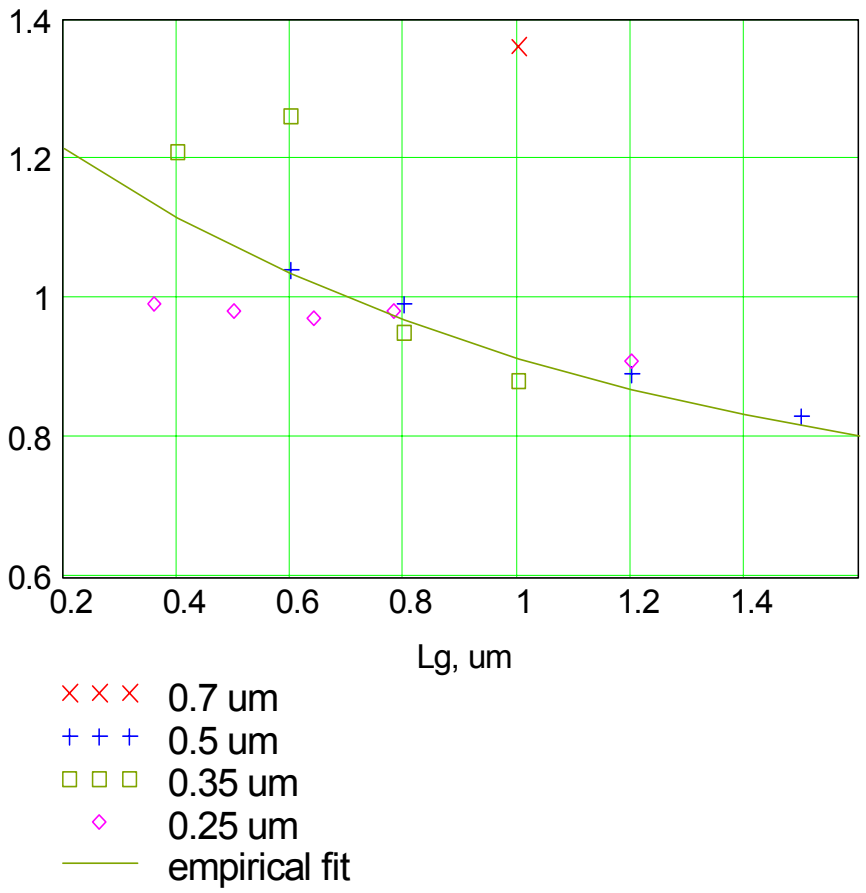
White series noise

- **Parameter $\gamma = g_m * R_n$**
- **Long channel** $\gamma =$ **1 linear**
  1/2 weak inversion
  2/3 strong inversion
- **Short channel γ: difficult to model**
- **High γ (γ = 2 – 4) reported in experimental submicron NMOS devices**
- **Strong increase in γ at high V_{DS}, high I_D/W**
- **Recent results on submicron CMOS at low V_{DS}, I_D/W:**

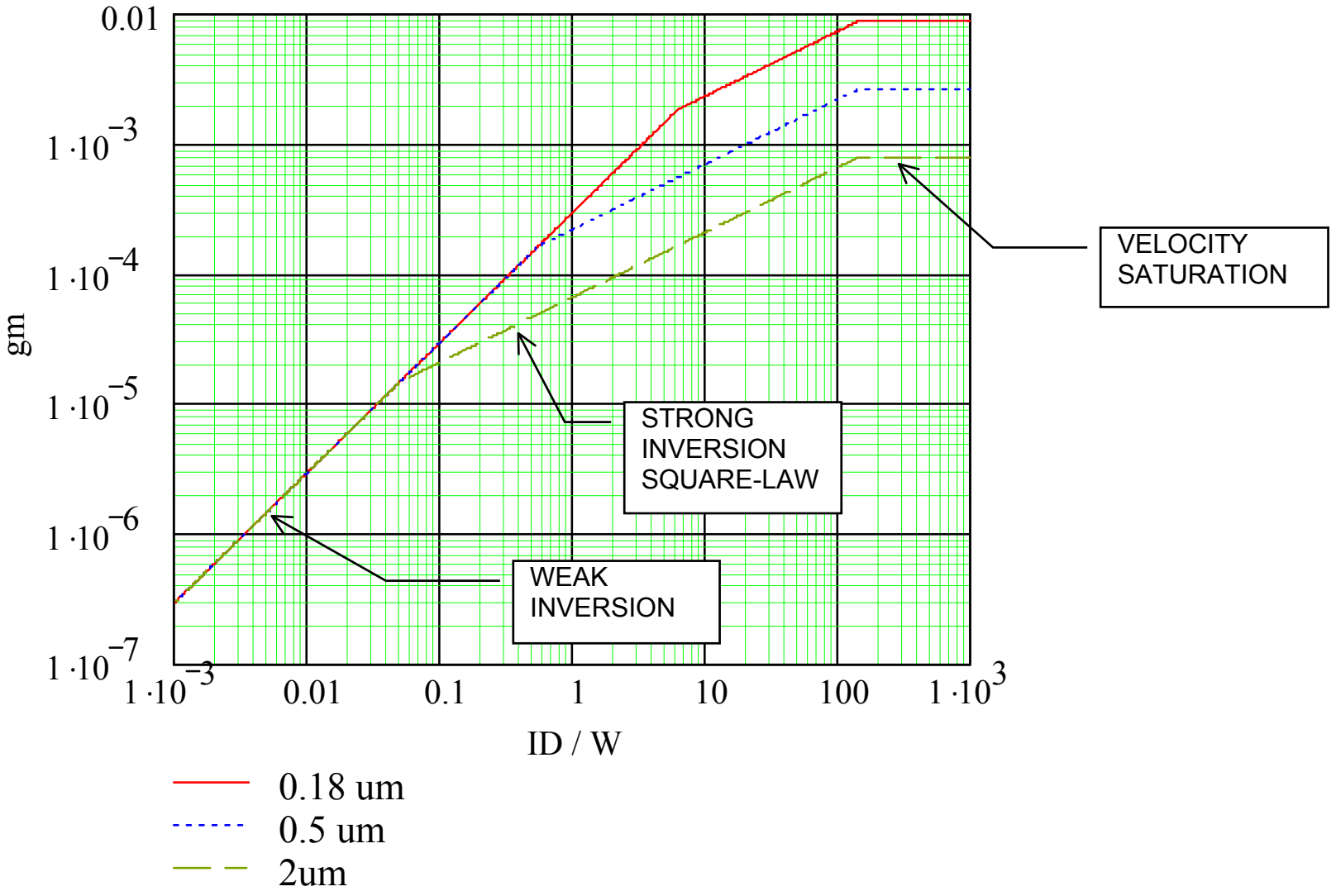
  $0.8 < \gamma < 1.35$

- **Shallow junctions increase S/D series resistance => noise**



Departure from square-law behavior

- **Submicron devices are less often operated in strong inversion, square-law region.**

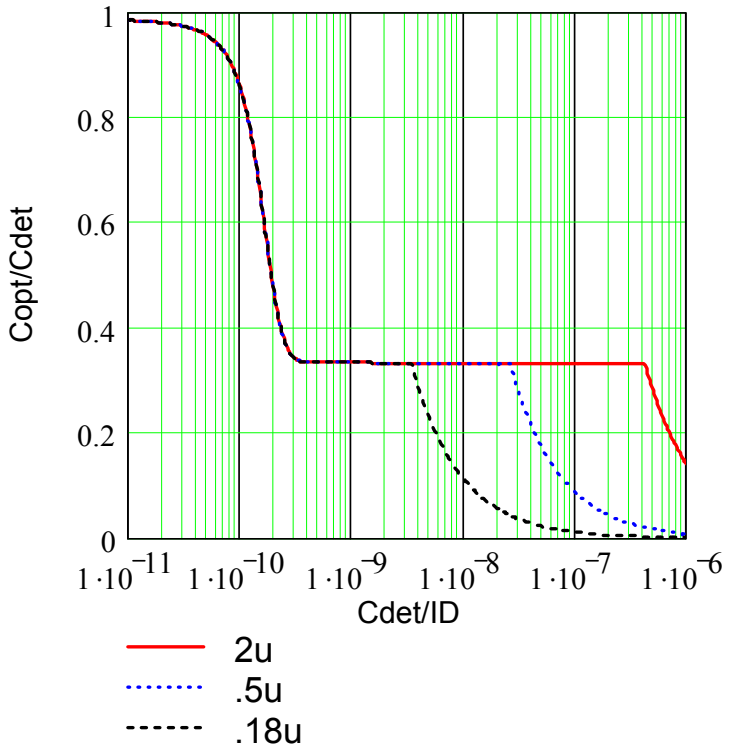


Dimensioning the input device

- **Drain current = constant**
- **Ratio of C_{gs} to C_{det} determined by C_{det}/I_D:**

C_{det} / I_D Ratio	Region of operation	Optimum capacitive match
$\frac{C_{\det}}{I_D} < \frac{6\mu}{v_{sat}^2}$	Velocity saturated	$C_{gs} = C_{det}$
$\frac{6L^2}{\mu(nkT/q)^2} < \frac{C_{\det}}{I_D} < \frac{6\mu}{v_{sat}^2}$	Strong-inversion square-law	$C_{gs} = C_{det} / 3$
$\frac{C_{\det}}{I_D} > \frac{6L^2}{\mu(nkT/q)^2}$	Weak inversion boundary	$C_{gs} = \frac{2L^2 I_D}{C_{\det}(nkT/q)^2}$

- **Weak inversion operation is never optimal for noise**



ENC scaling for white series noise

$$ENC_{w,\min}^2 = \frac{128}{27}\frac{a_1 kTC_{\det}^2 L}{\sqrt{2\mu C_{\det} P / 3V_{DD} t_m}}$$

L' -> λ L

VDD' -> λ VDD

$ENC_{w,min}$' -> $\lambda^{3/4}$ $ENC_{w,min}$

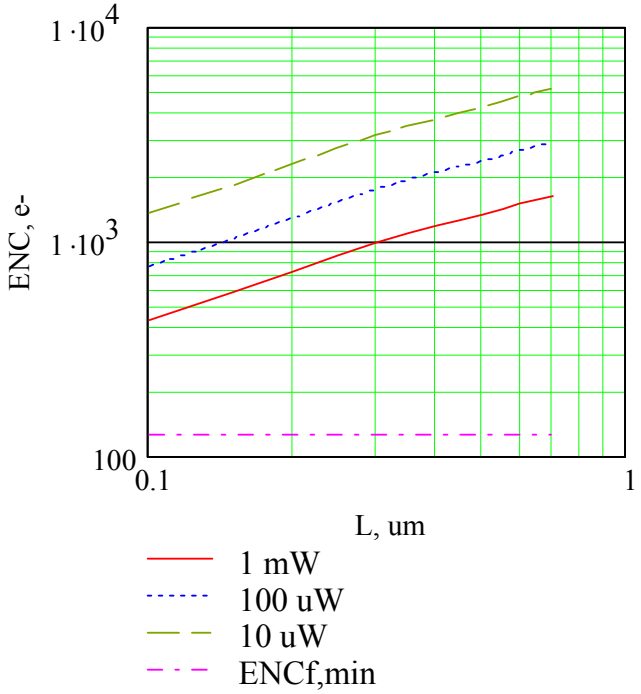
23% improvement per generation

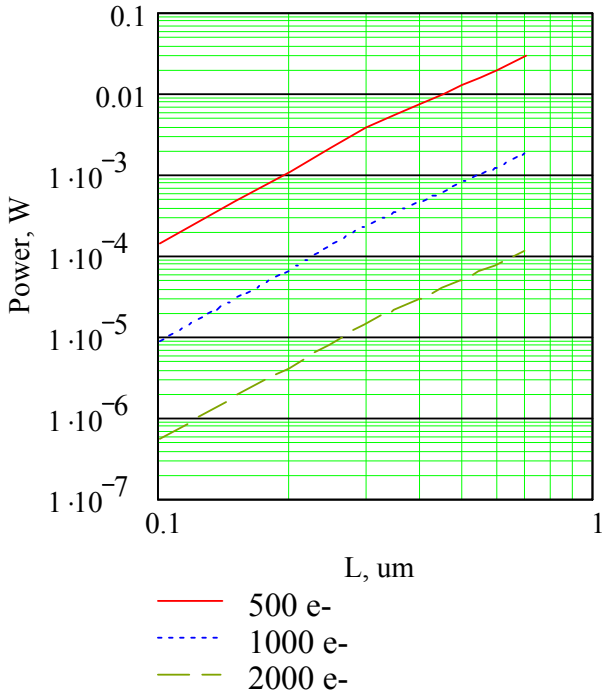
Power required to achieve ENC:

P' -> λ^3 P

66% decrease/generation

Conditions: C_{det} = 50 pF, t_m = 50 ns





Dynamic Range

Max output signal ~ V_{DD} => $Q_{in,max} = c\, C_{det}\, V_{DD}$

Where $c = C_F/C_{det} < 0.05$ in practical circuits.

SNR scaling:

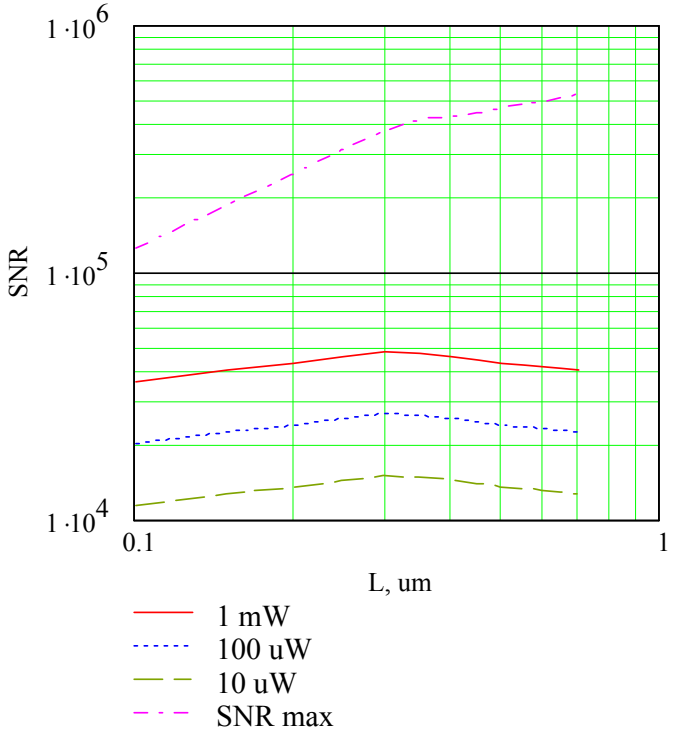
$$SNR = \frac{c\mu^{1/4} P^{1/4} C_{\det}^{1/4} V_{DD}^{1/4}}{\sqrt{10 a_1 kT / t_m} L^{1/2}}$$

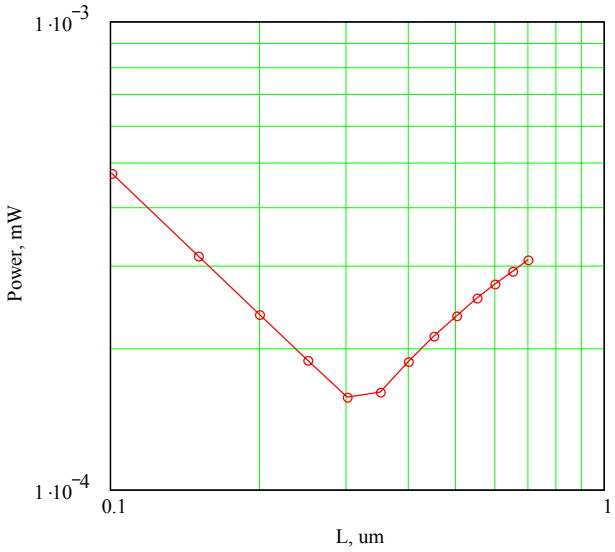
L' -> λ L
VDD' -> λ V_{DD}
SNR' -> $\lambda^{1/4}$ SNR
10% decrease per generation

P' -> λ^{-1} P
43% increase per generation

Conditions: C_{det} = 50 pF, t_m = 50 ns,

C_F/C_{det} = 0.05



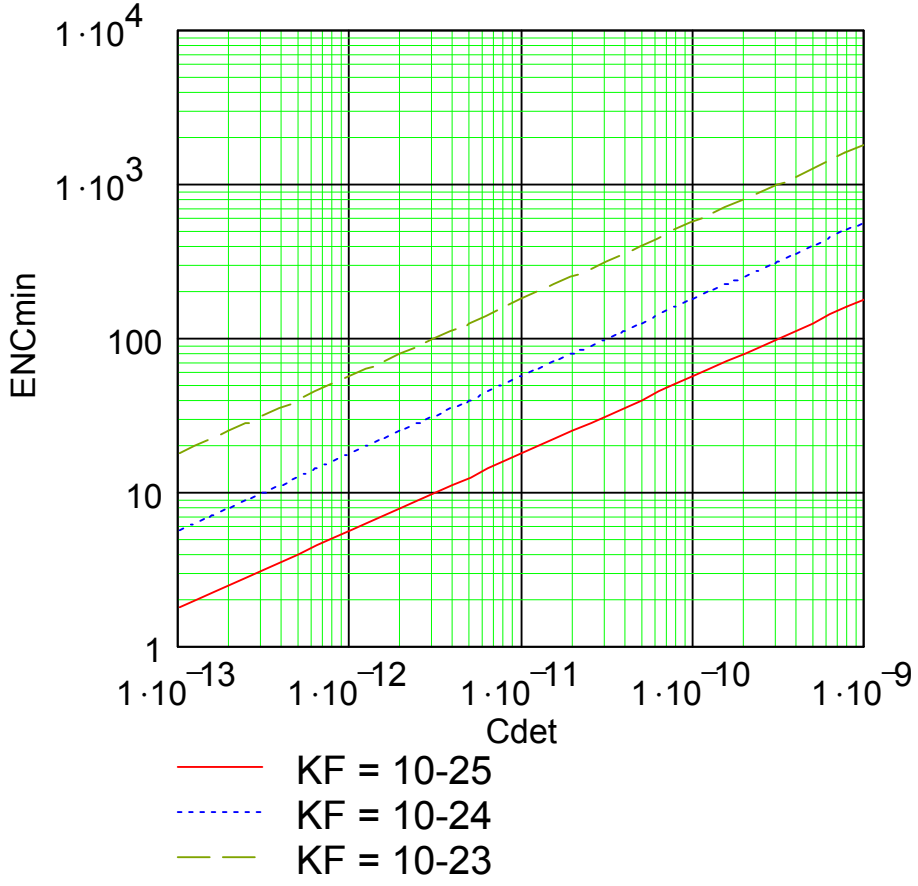


1/f noise

- **High and variable 1/f noise has always been characteristic of MOSFETs**
- **Strongly dependent on interface quality and gate process**
- **PMOS always found to be 3 - 30X better than NMOS (buried channel device)**
- **1/f sets the min. achievable ENC for the technology:**

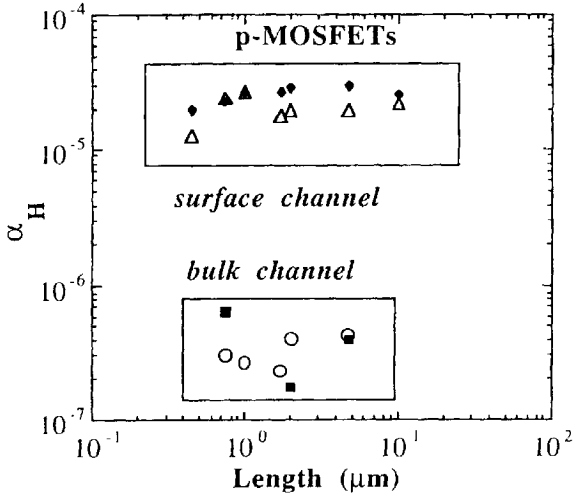
$$\mathrm{ENC}_{\mathrm{f,min}} = 2\sqrt{a_2 K_F C_{\mathrm{det}}} \qquad \text{where } \mathrm{e}^2_{\mathrm{n,f}} = \frac{K_F}{C_{ox} W L f}$$

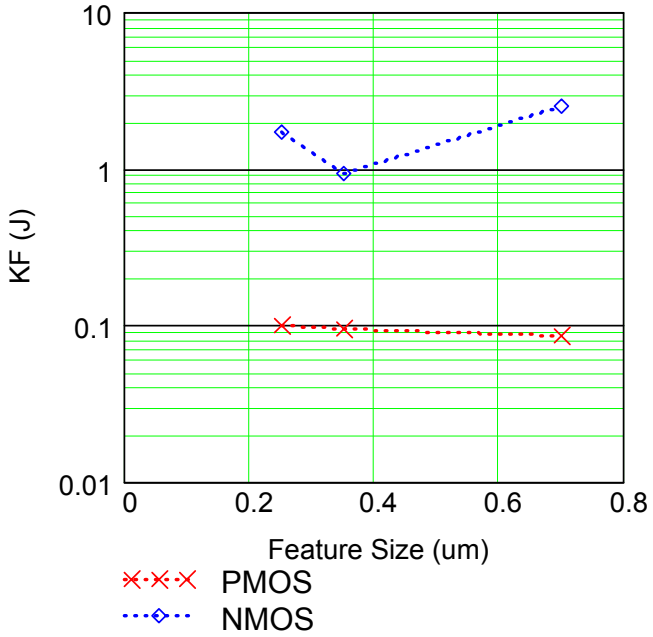
- **To reach $\mathrm{ENC}_{\mathrm{fmin}}$, series white noise must be suppressed by increasing I_D.**



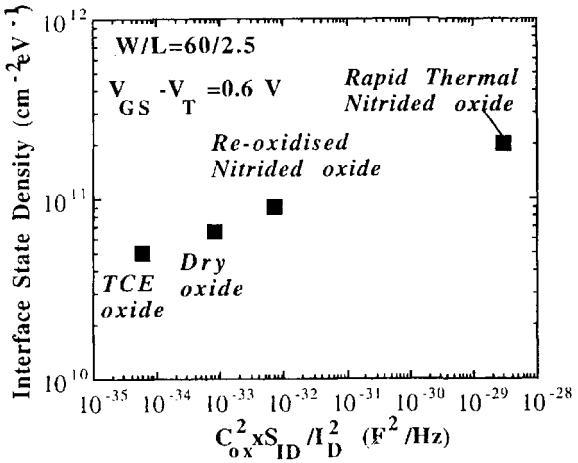
1/f scaling issues

1. **Prediction: In processes with n+/p+ poly gates and retrograde wells, PMOS will become a surface channel device and will lose its advantage over NMOS. Not confirmed by measurements on typical amplifier devices even down to 0.25 μm**





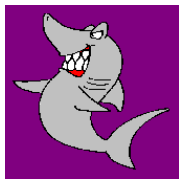
2. **The shallow junctions required for scaled devices can only be preserved by limiting the thermal budget -- hence gate process will have reduced post-oxidation anneal and higher trap density**

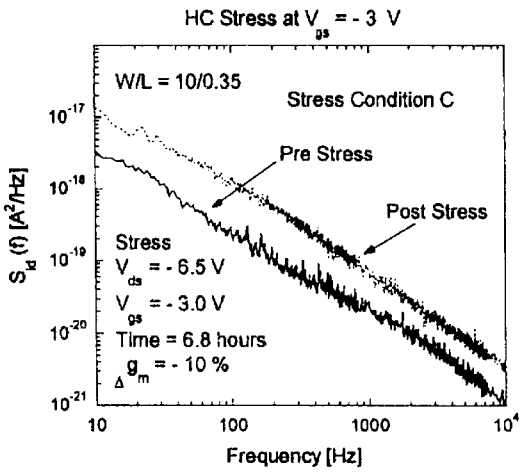


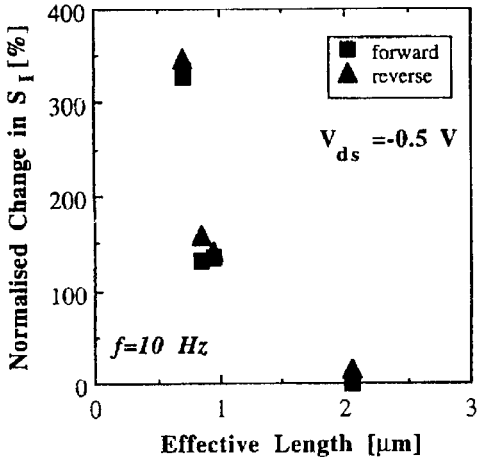
3. **For ultrathin gates new dielectrics with higher trap densities will be used (nitrided, halogenated, H_2 annealed)**

Hot carrier stress and 1/f noise

- **Hot carrier stress generates new oxide/interface traps.**
- **1/f noise more sensitive than change in static parameters:**
  - **Δgm -10%**
  - **Δ(1/f) +400%**
- **Worse for shorter channel lengths**
- **A device engineered for "acceptable" degradation of V_{th} and g_m may show unacceptable increase in 1/f noise over the same period.**
- **The operating point of the device will determine the stability of the long-term 1/f noise.**







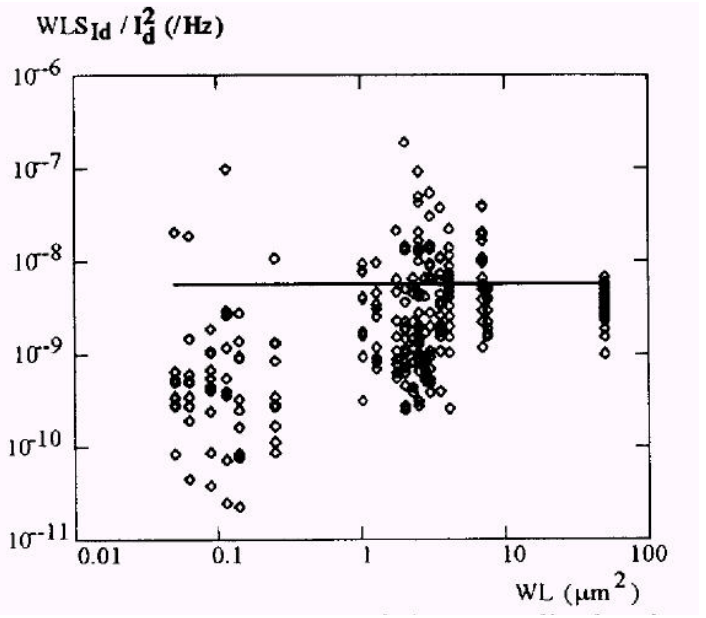
1/f noise in very small devices

1/f noise is a superposition of a large number of RTS fluctuations due to trapping-detrapping phenomena.

The 1/f spectrum is the sum of a series of Lorentzians for each trap.

For small devices (WL ~ 1 μm^2) there will be a departure from 1/f behavior and much greater dispersion in the noise from transistor to transistor, due to the finite number of active traps.

Usually, the CSA input device will be dimensioned much larger than this.



Low frequency noise dispersion measured over a wide range of device size.

ENC due to 1/f noise

- **Input device dimensioned to $C_{gs} = C_{det}$**

$$\mathrm{ENC}_{\mathrm{f,min}} = 2\sqrt{a_2 K_F C_{\mathrm{det}}}$$

Note: independent of bias, peaking time, device dimension.

- **ENC_{fmin} is the ultimate limit to ENC of any MOS amplifier.**

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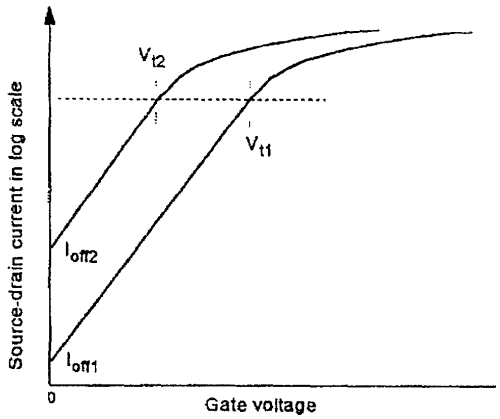
Increase in Off-state Leakage

- **Due to threshold voltage scaling**

$$I_{off} \sim e^{q(V_G - V_{th})/nkT}$$

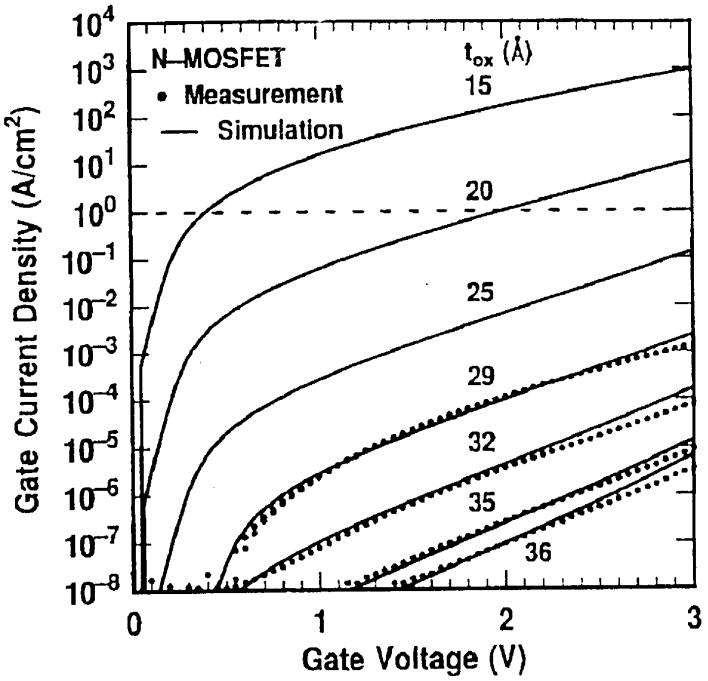


- **Other effects:**
  - **source-drain punchthrough**
  - **gate-induced drain leakage**

- **Source-drain leakage will effect parallel noise from the DC feedback (reset) system**

Gate Tunnelling current

- **At a bias of 1.5V, gate current density increases by 10 orders of magnitude as the oxide thickness decreases from 3.6 to 1.5 nm**
- **I_G = 1A/cm^2 considered tolerable for digital circuits (total gate area per chip ~ 0.1 cm^2)**
- **Typical input FET would have I_G ~ 10 - 100 nA; ENC_p ~ 200 - 700 rms e^- at 1 μsec**



ESD protection devices in scaled technology can develop 100 nA leakage after exposure to small stresses

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MOSFET Replacement of Resistors and Capacitors

- **Charge sensitive amplifier with linearized feedback**

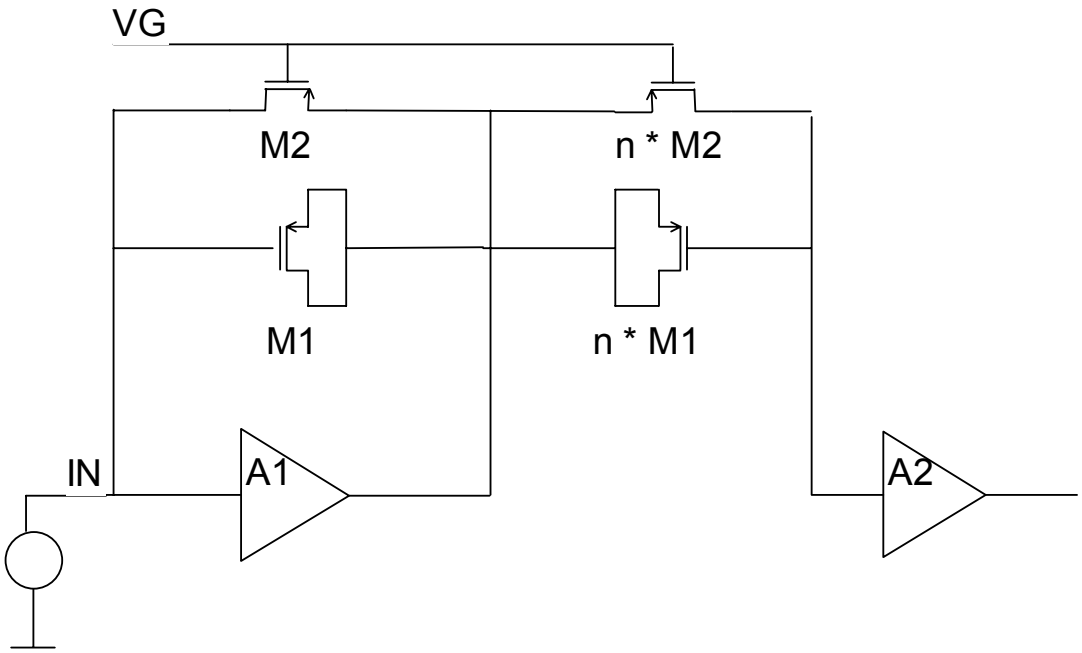
  Qout = n * Qin

- **MOSFET-C, gm-C filters**

  Dynamic range to 50 – 60 dB

- **ADCs based on MOS resistor ladders**

  12 bit, 1 MHz



Crosstalk

- **Wire bonds**
- **Substrate**
- **Power Supply**
- **Bias nodes**

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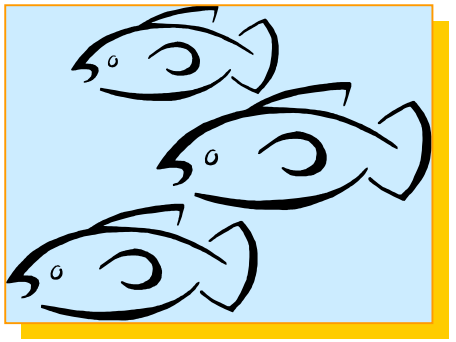
Performance limits

- **Device noise sources – gradual increase**
- **1/f will continue to set the ultimate limit of ENC performance**
- **To maintain SNR, power dissipation will need to increase**
- **Possibility of process-related catastrophic increase in 1/f noise (unlikely because of RF and PLL needs)**
- **Low-C preamplifiers will be most effected by 1/f and parallel noise increases**
- **Rail-to-rail and differential techniques will be needed to help the SNR**
- **Promising new technologies**
  - **Dual- Vth CMOS**
  - **SOI**
  - **Si-Ge CMOS**
  - **Double-gated CMOS**

Analog-digital "partnership"

- **Increasing integration of VLSI digital processing with the front end**
  - cost of on-chip connection << on-chip
  - digital more power-efficient for high-precision signal processing
  - digital cost per transistor
- **Analog will be relegated to the bare essentials:**
  - impedance conversion/amplification
  - filtering
  - A/D conversion
- **Digital control loops can compensate for analog imperfections, change of signal conditions –**
  - offset, gain trim
  - self-calibration
  - linearization
  - time constant control
  - radiation-induced changes
  - pole-zero cancellation
  - rate changes
  - non-random noise



Charge sensitive amplifiers in the ULSI environment

- **Mega-transistor design requires high manpower investment**
  - **Only justified for high-volume applications**
    - **collider detector**
    - **generic function chip, personalizable to serve many systems**

- **Growing use of CMOS VLSI to process signals from array sensors – pixel, CMOS imager**