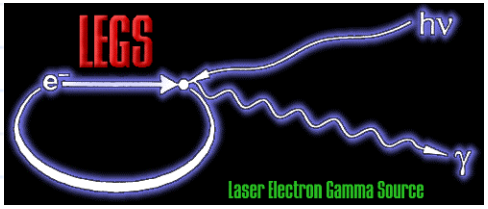


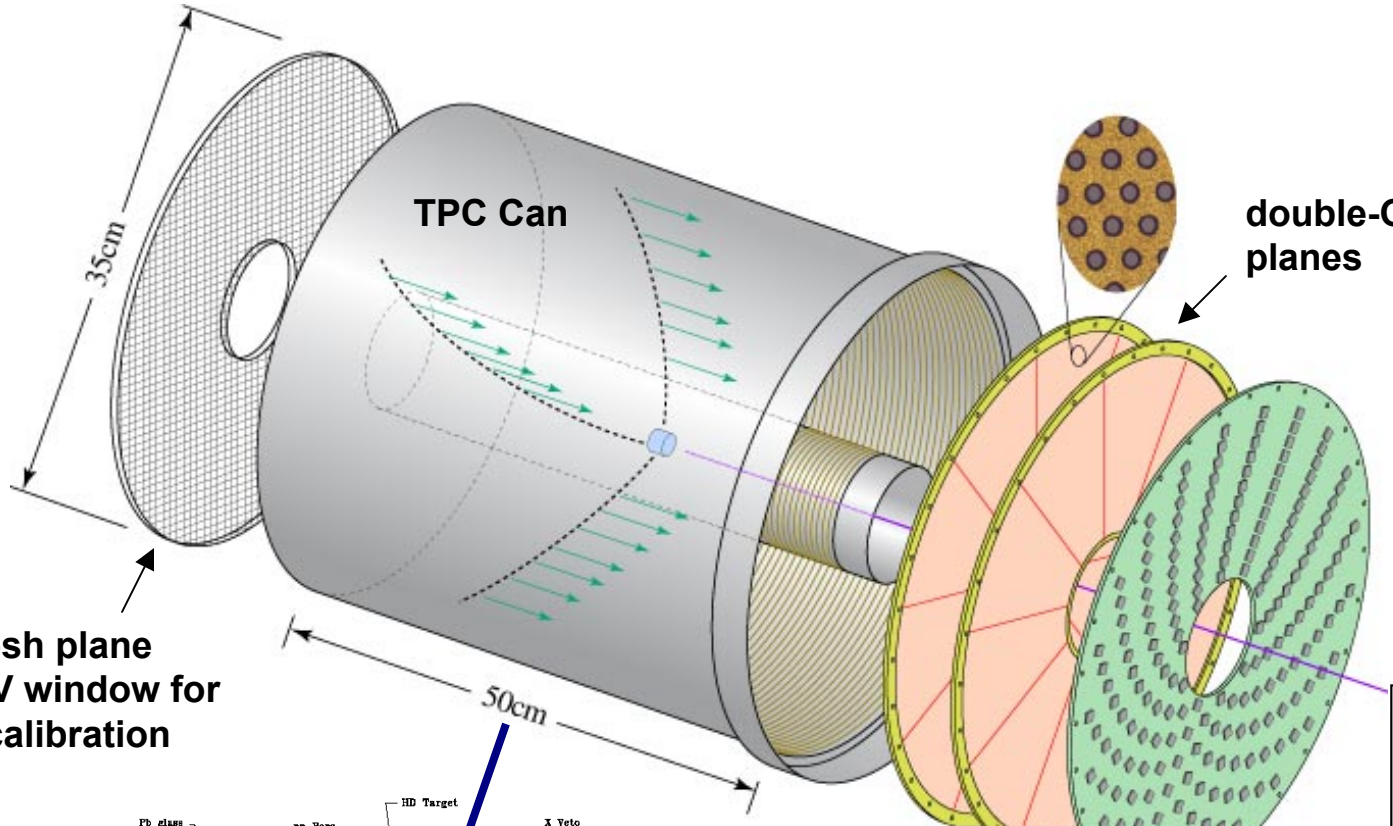
Front-End ASIC for a GEM Based Time Projection Chamber

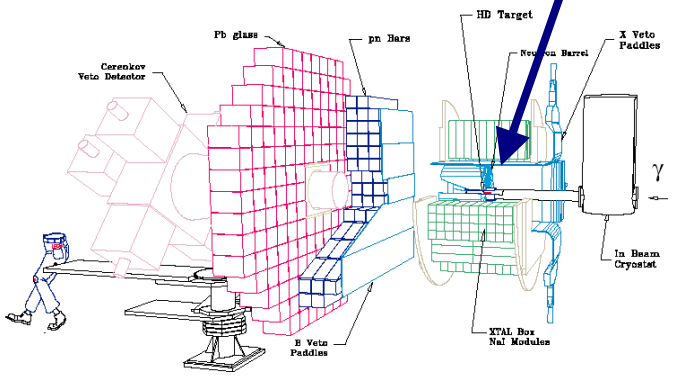
G. De Geronimo, J. Fried, P. O'Connor, G. Smith, V. Radeka, B. Yu
Instrumentation Division, Brookhaven National Laboratory, Upton, NY

C. Thorn
LEGS Group, Physics Department, Brookhaven National Laboratory, Upton, NY

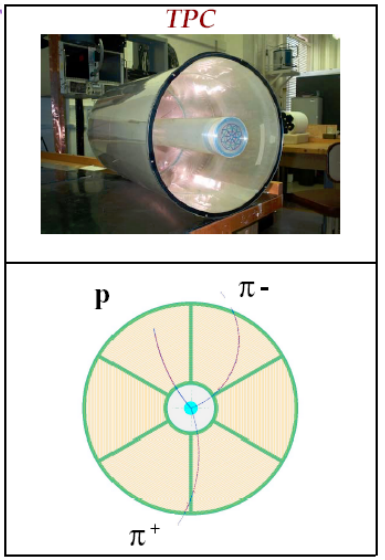
NSS / MIC 2003

Laser Electron Gamma Source : Time Projection Chamber (TPC)



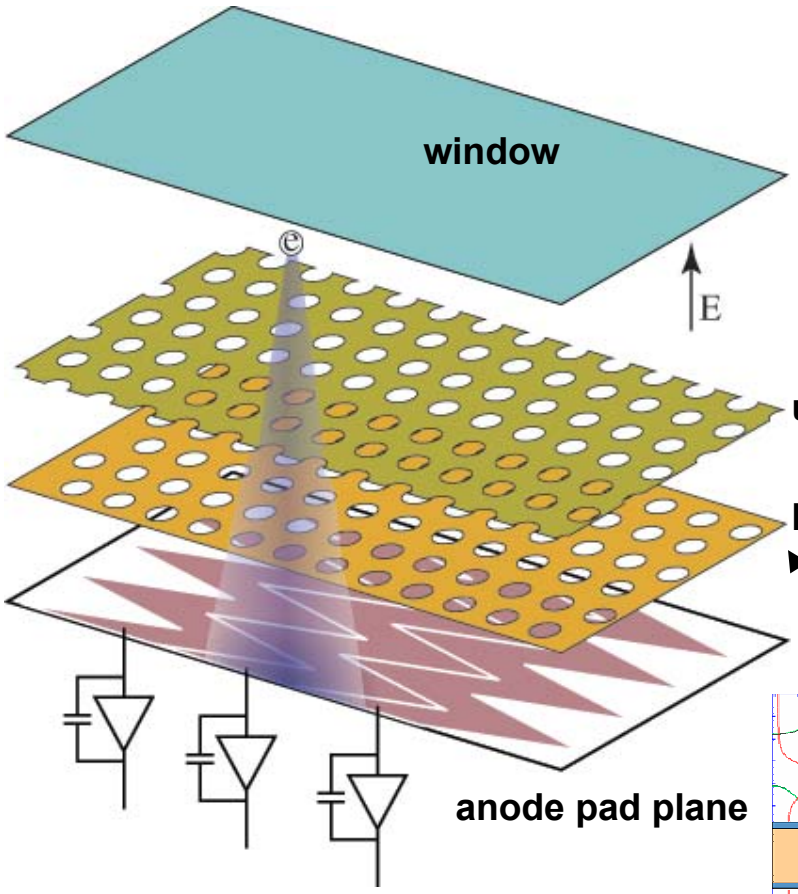


anode pad plane
electronics per pad
~ 8000 channels

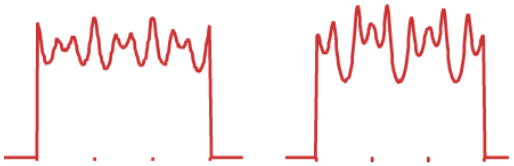


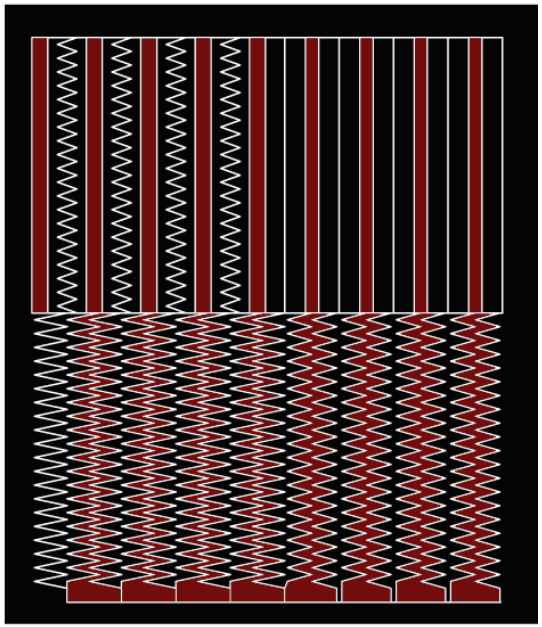
Spin ASYmmetry Array (SASY)

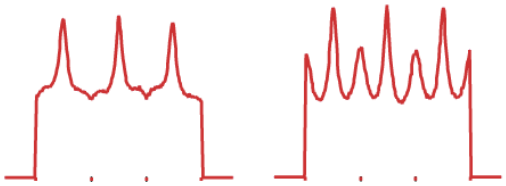
Interpolated Zigzag Pad Readout for Double Gas Electron Multiplier (GEM)

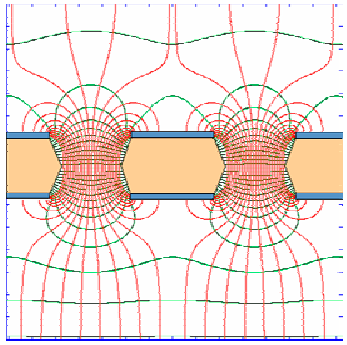


Bo Yu et al.,
TNS 50, 2003
in press





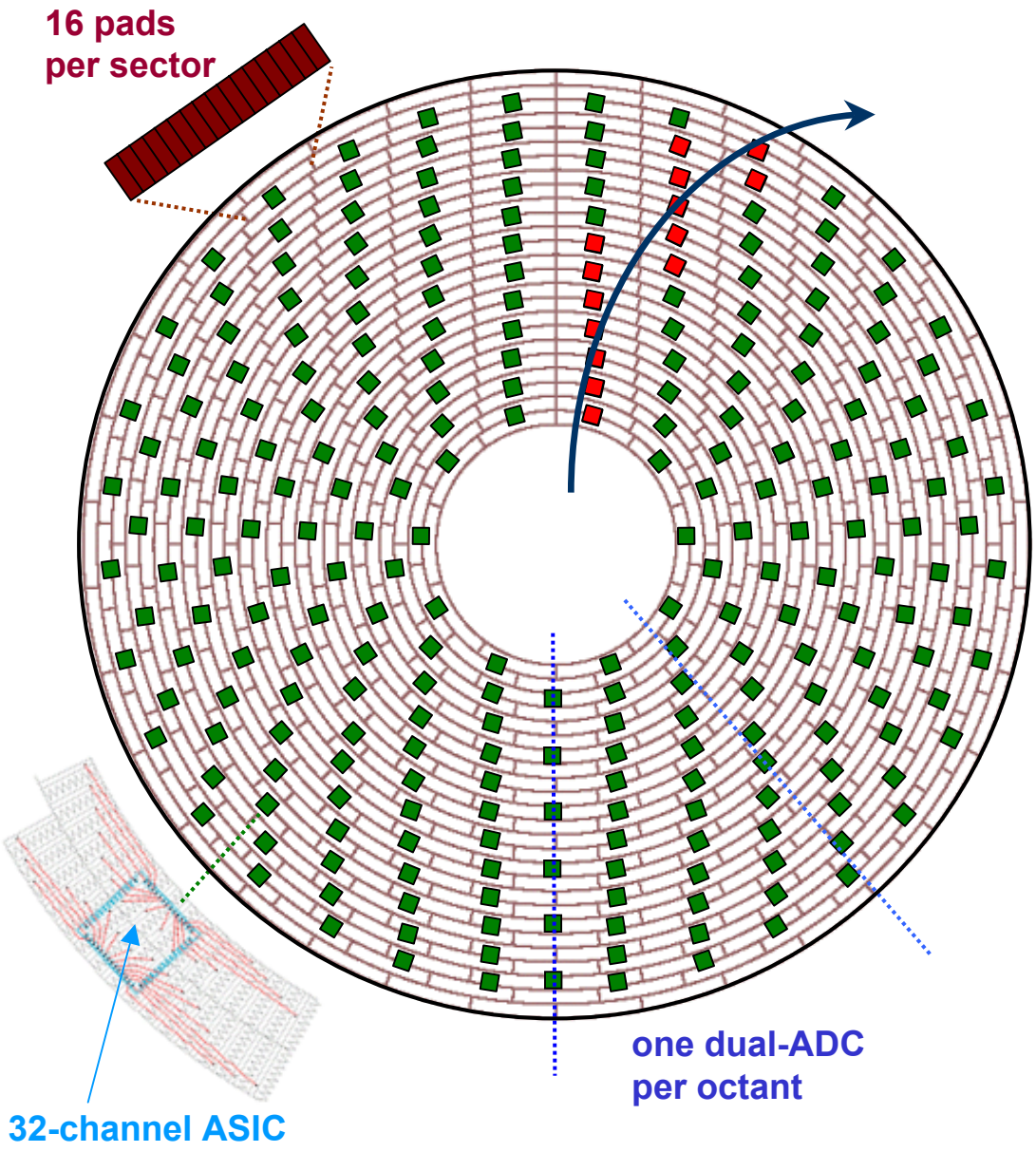




front-end electronics
~ 8000 channels

pitch 2mm
resolution 200μm rms

Front-End Electronics – Specifications



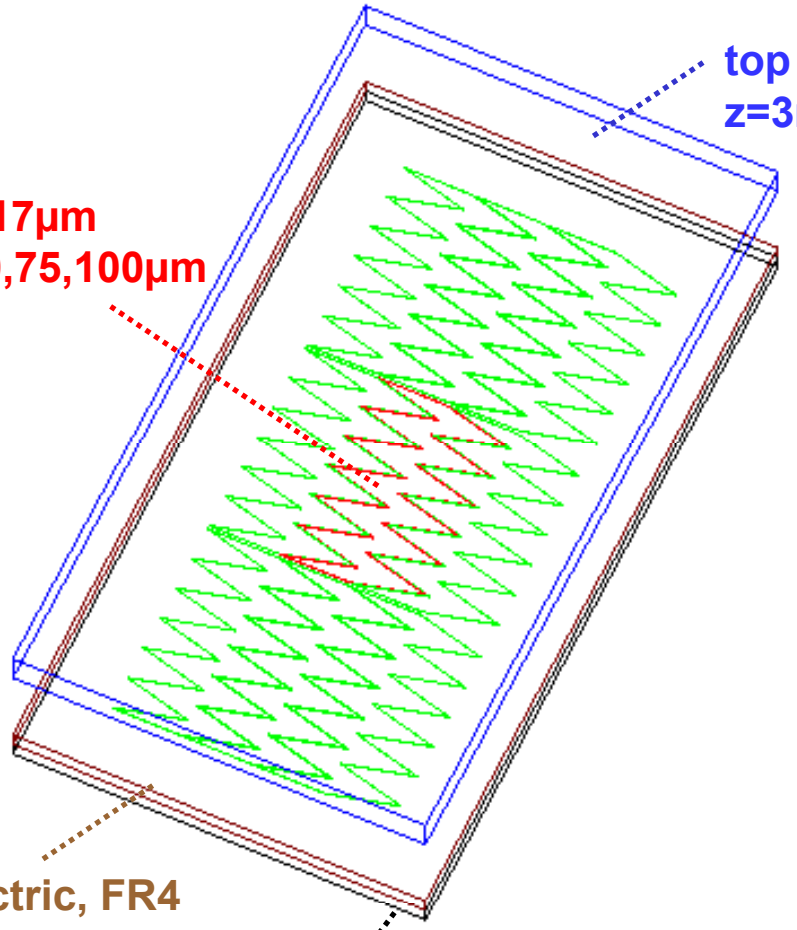
Tracking Measurement

- Low-rate low-multiplicity
- Energy - triggered pad
- Energy - neighbor pads (centroid)
- Timing of triggered pad (z)

Specifications

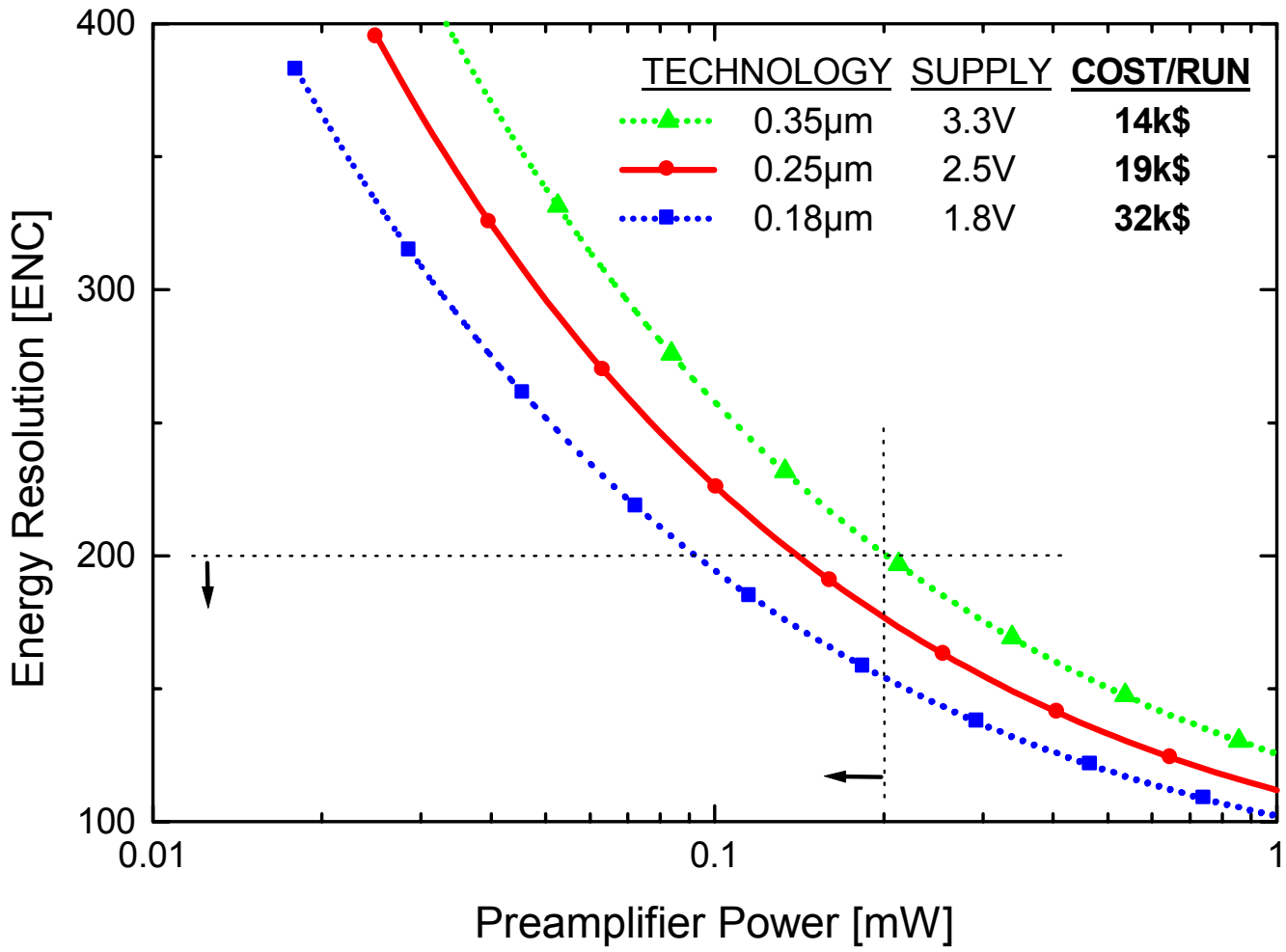
- ENC < 500e^- rms (GEM gain 500)
- Timing < 20ns rms (drift time 5μs)
- Preamplifier/shaper/BLH
- Adjustable gain ≈ 17-32 mV/fC
- Peak-detector
- Neighbor channel/chip enable
- Timing-detector (TAC)
- Channel masking
- Calibration
- On-chip buffers
- Token/flag readout

Simulated Pad Capacitance



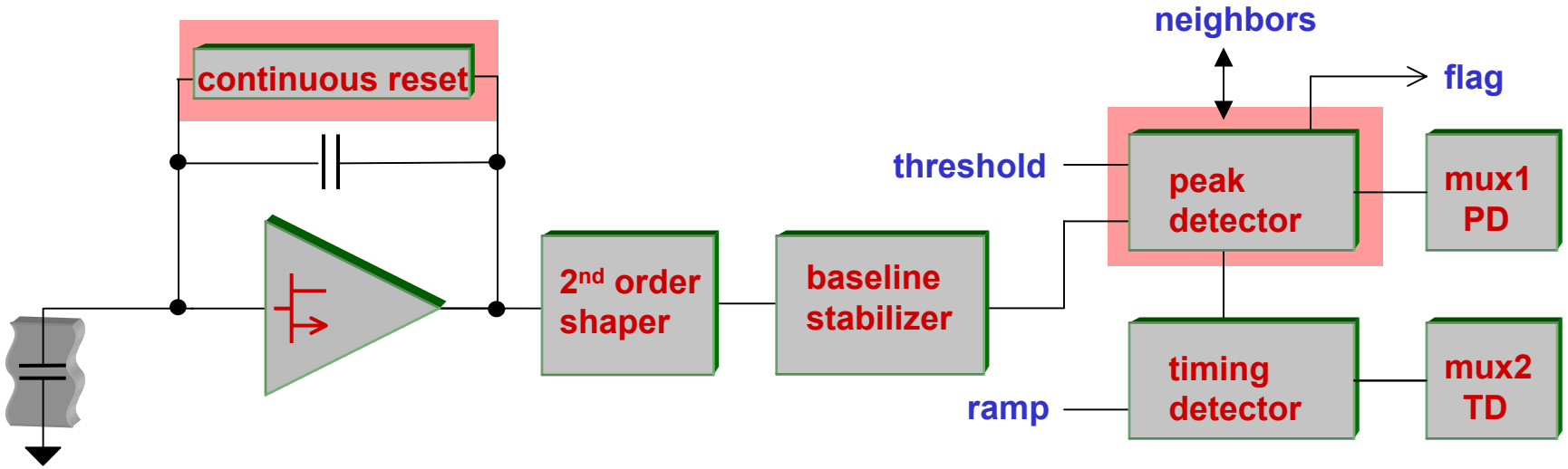
gap [µm]	C_{BOT}	C_{TOP}	C_X	C_{XY}	C_{TOT} *[fF]*
50	967	37	82	1742	**4652**
75	983	37	68	1457	**4070**
100	998	38	60	1292	**3725**

Front-End Electronics – Preamplifier Power



- **32-channel ASIC - layout is pad-limited ≈ 3 x 3 mm²**
- **power / channel ≈ 1mW (preamplifier < 200µW)**
- **energy resolution < 250 rms electrons (600ns peaking time, 5pF)**

ASIC Readout Channel - Block Diagram



INPUT n-MOSFET
- optimized for operating region
- ENC<250 rms electrons
- NIM A480, p.713

CONTINUOUS RESET
- feedback MOSFET
- self adaptive
- low noise
- fully compensated
- NIM A421, p.322
- TNS 47, p.1458

SHAPER
- amplifier with passive feedback
- dual stage multiple feedback
- 2nd order, 600ns peaking time
- adjustable channel gain (3-bit)

BASELINE STABILIZER (BLH)
- band-gap referenced
- low-frequency feedback
- slew-rate limited follower
- high dc stability < 1mV
- low channel dispersion < 4mV
- TNS 47, p.818

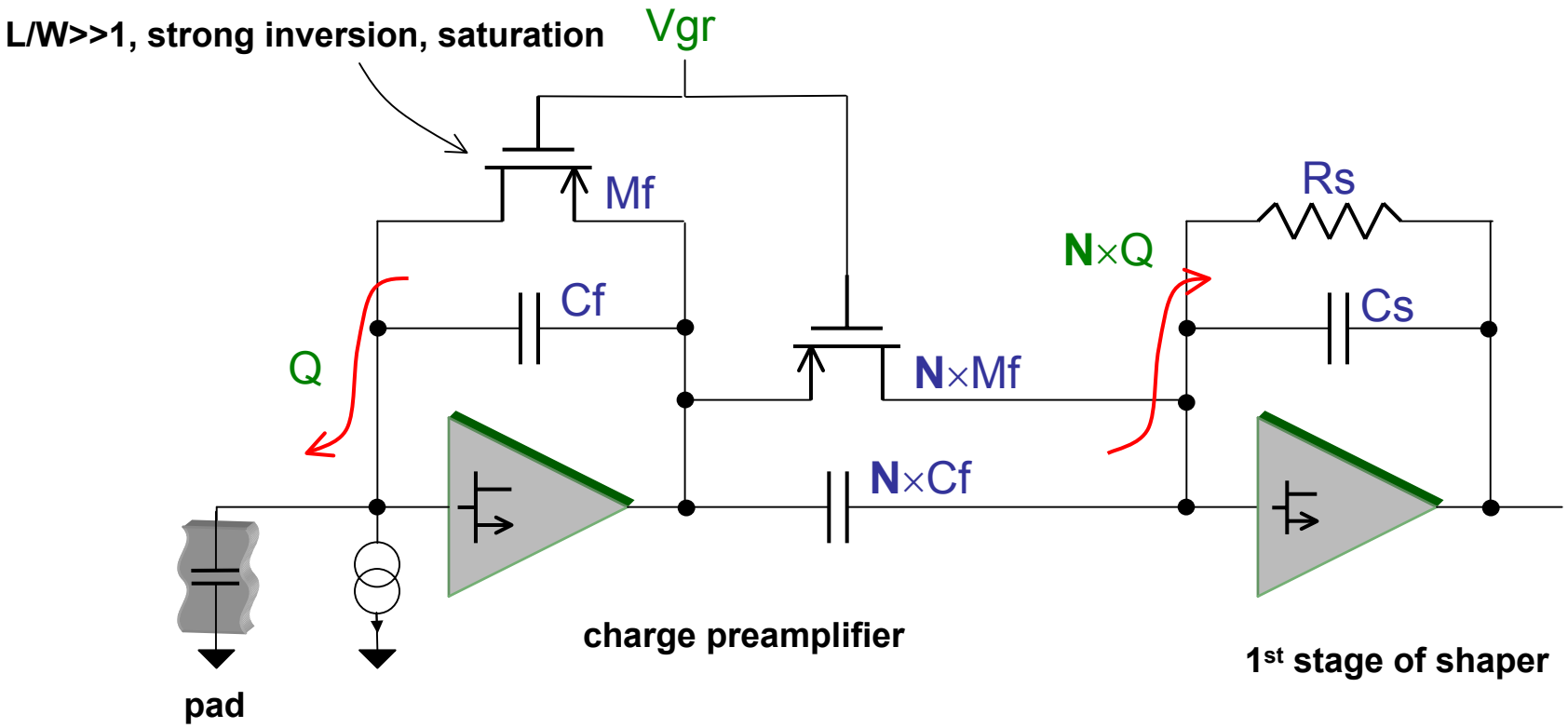
PEAK DETECTOR
- two-phase configuration
- offset error cancellation
- high absolute accuracy < 0.2%
- NIM A484, p.544

TIMING DETECTOR
- time-to-amplitude converter
- internal or external ramp
- two-phase configuration
- timing resolution < 20ns rms

≈ 350 µW

≈ 900 µW

Continuous Reset – Single Stage

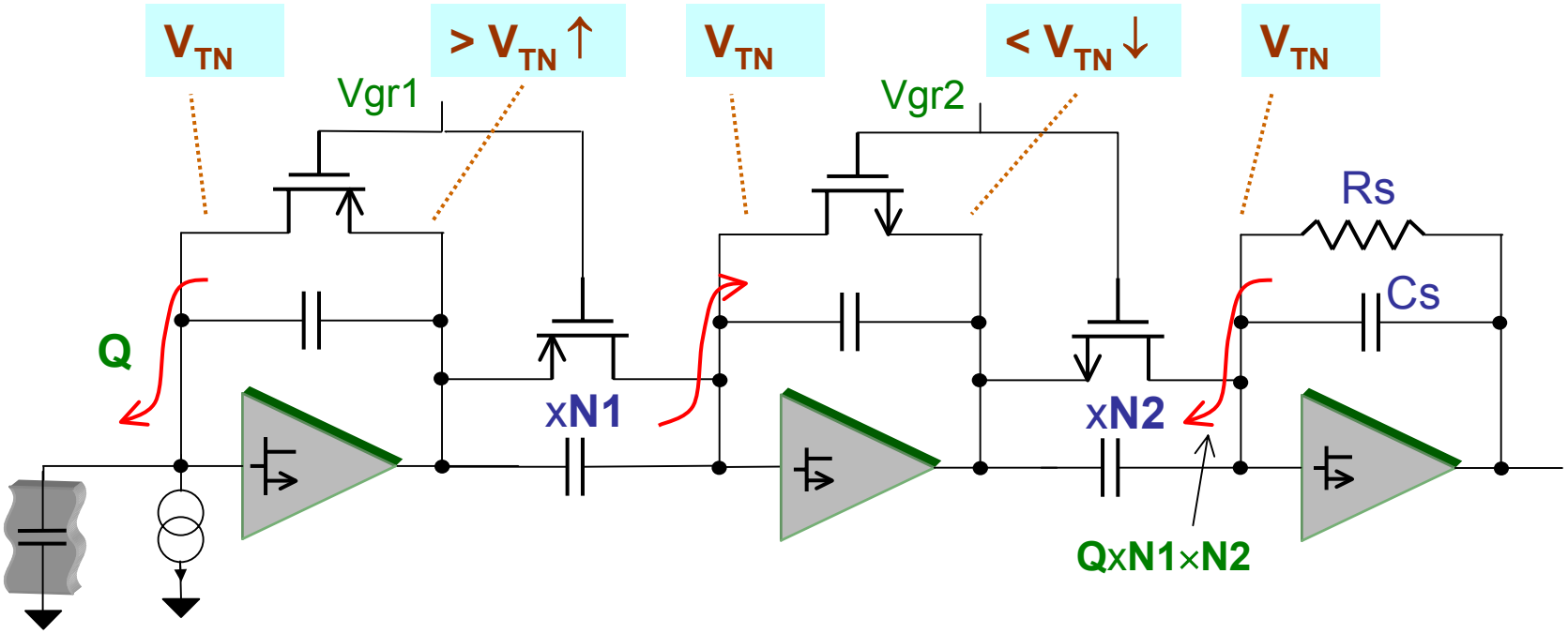


- charge gain **N**
- high linearity
- low noise
- (self-adaptive)

$$\frac{2kT}{Rs}\frac{1}{N^2} \equiv q \cdot I_{eq}$$

$$Rs = 200k\Omega\ ,\ N=16 \ \rightarrow\ I_{eq} \approx 1nA$$

Continuous Reset – Dual Stage

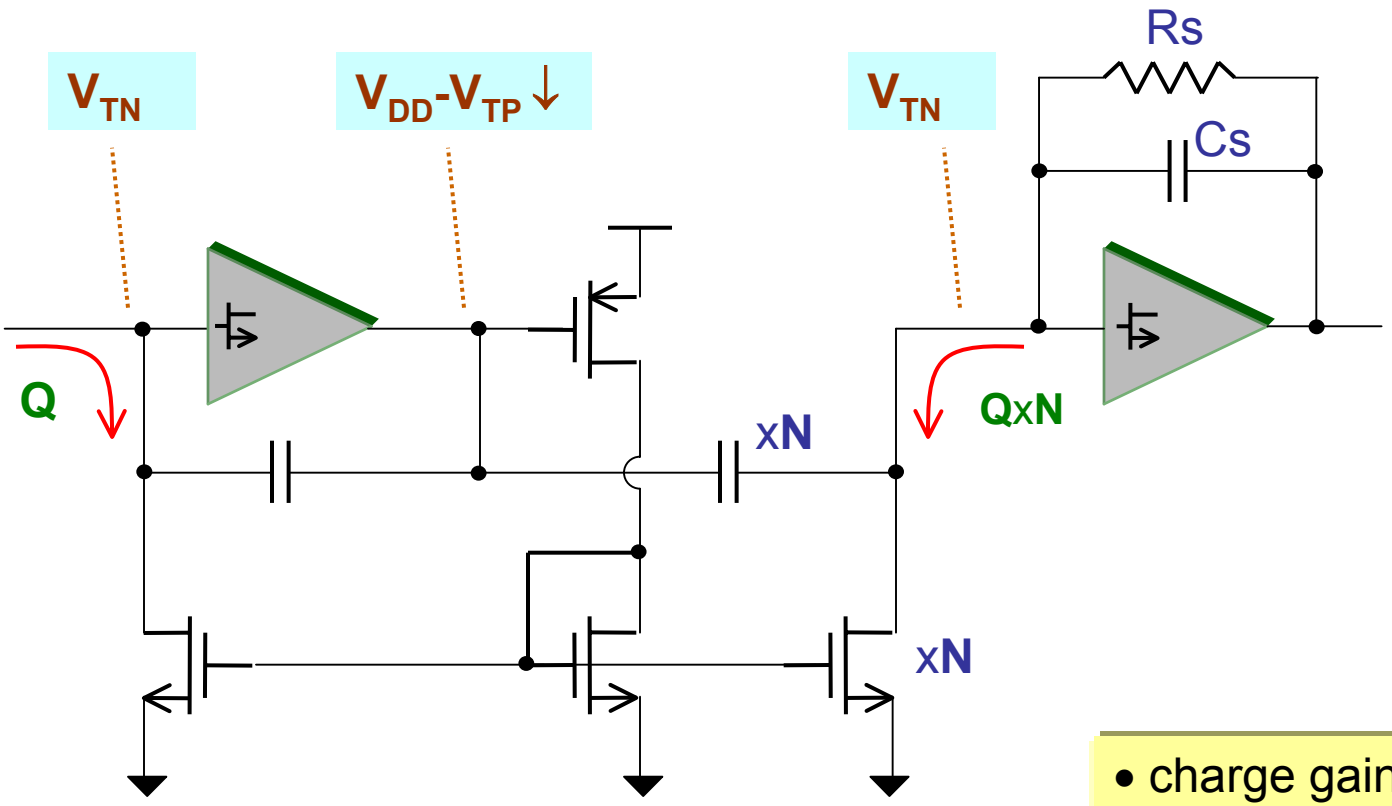


- charge gain N1xN2
- high linearity
- low noise
- self-adaptive

$Rs = 200k\Omega\ ,\ N1xN2 = 16x4 \rightarrow I_{eq} \approx 60pA$

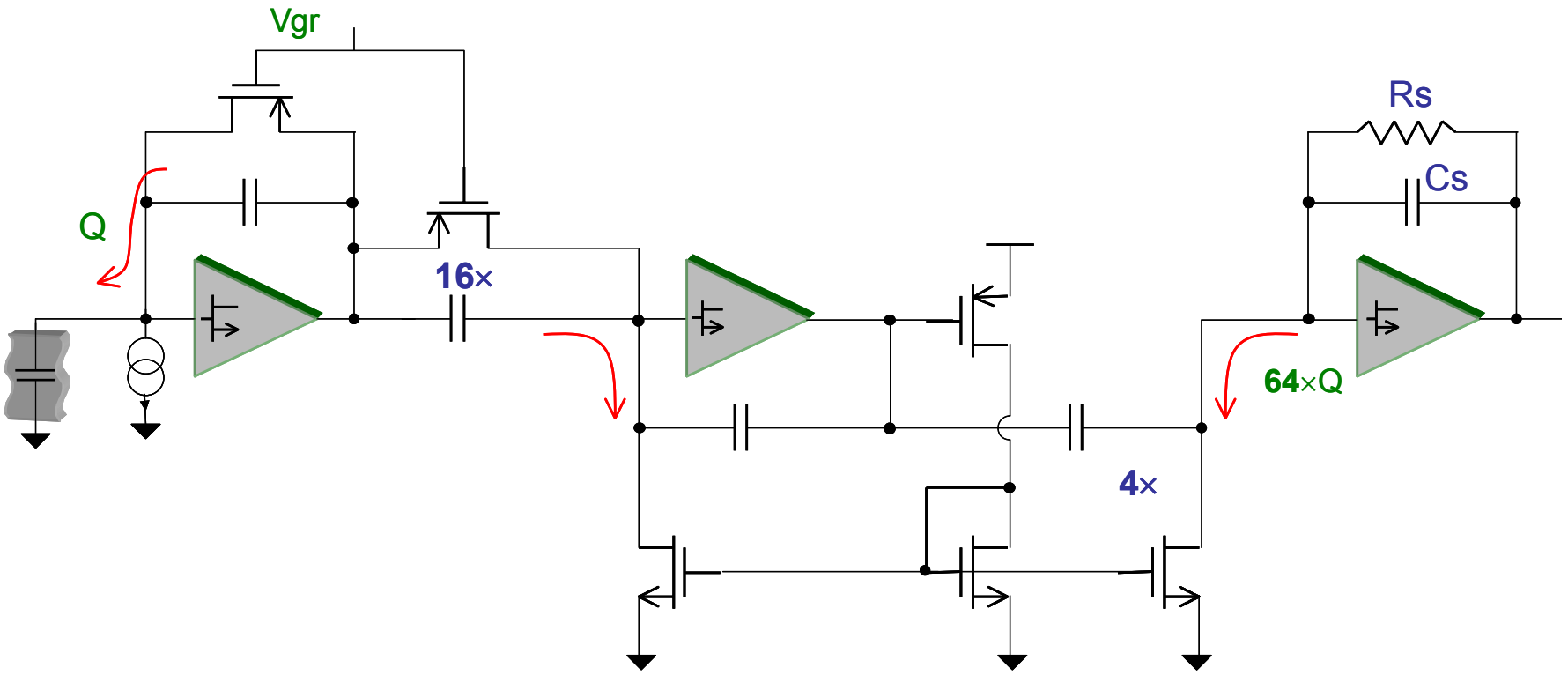
low-voltage → low dynamic range

Continuous Reset – Low Voltage Approach



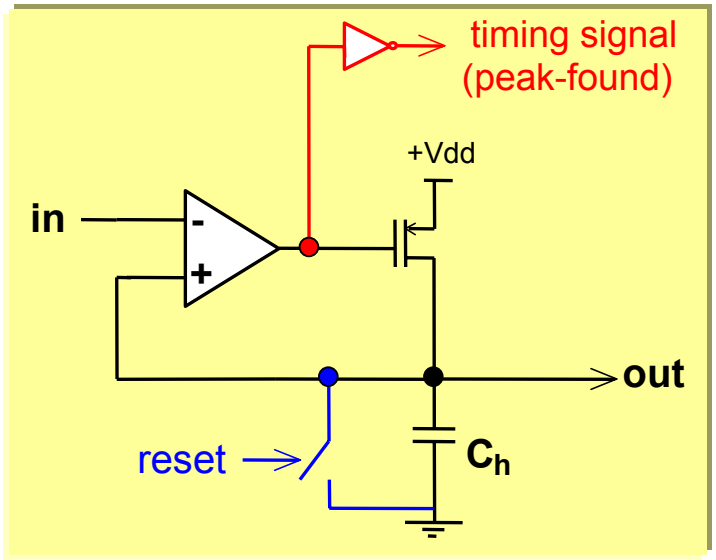
- charge gain **N**
- high linearity
- low noise
- self-adaptive

Continuous Reset – Low Voltage Approach – Dual Stage



N = 64

Peak Detector – Classical CMOS Configuration

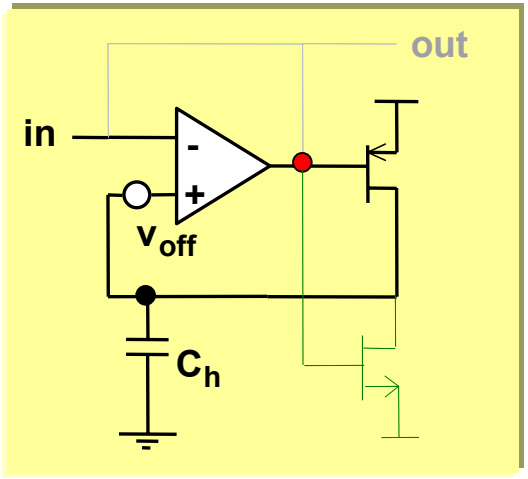


+ detects and holds peak **without external trigger**
+ provides accurate **timing** signal (peak found)
- **low accuracy** (op-amp offset, CMRR)
- **poor drive capability**

Peak Detector - Two-Phase Configuration

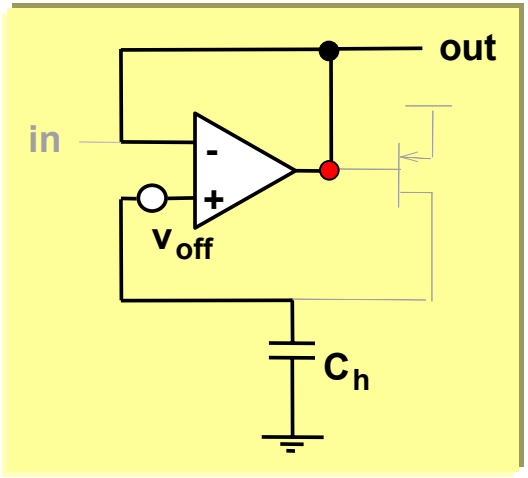
Write Phase

- **sub-threshold** : track mode
- **over-threshold** : peak-detect mode
  - like ***classical*** configuration



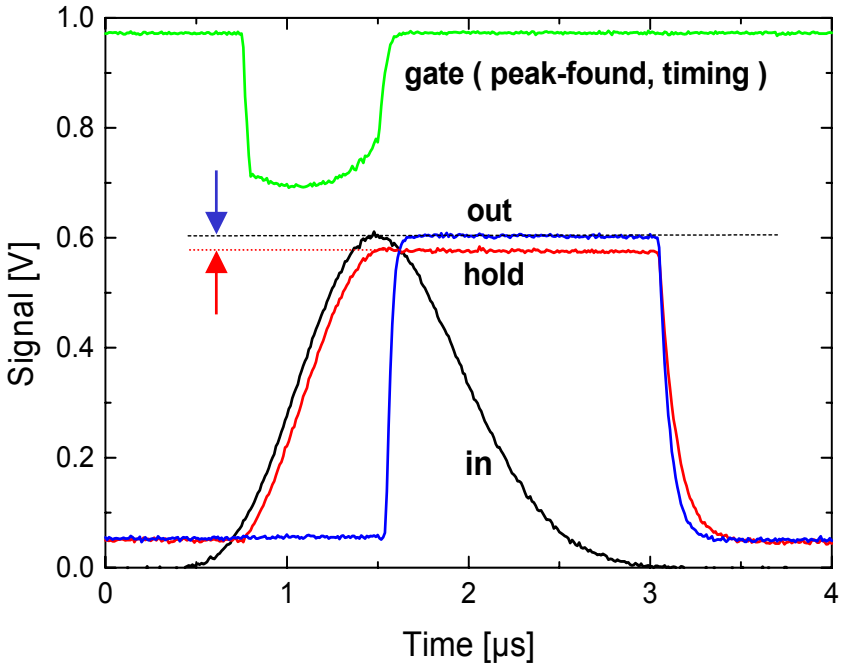
Read Phase

- self-switching (peak found, **timing**)
- op-amp re-used as buffer
- op-amp errors canceled
- enables rail-to-rail sensing
- high drive capability

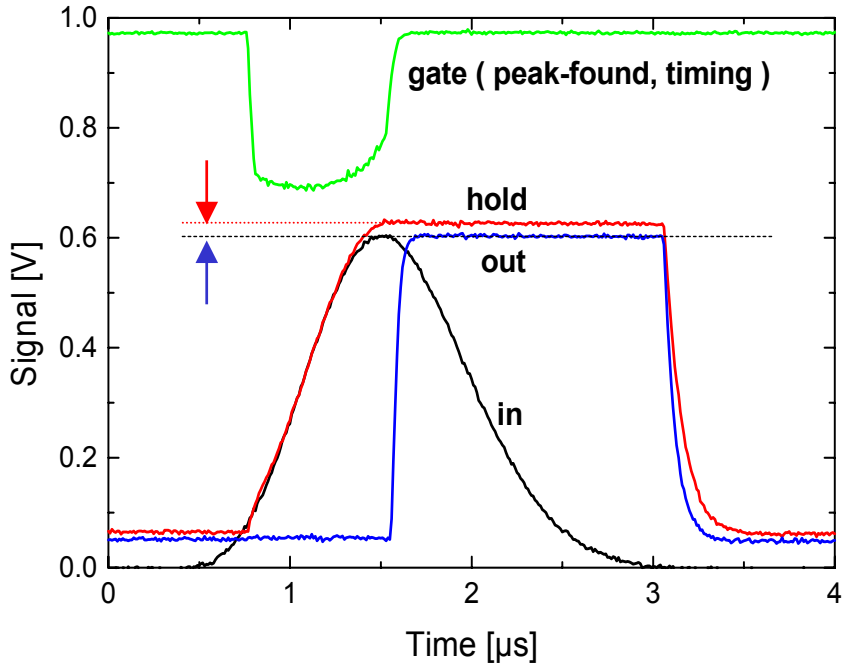


Peak Detector - Two-Phase Configuration

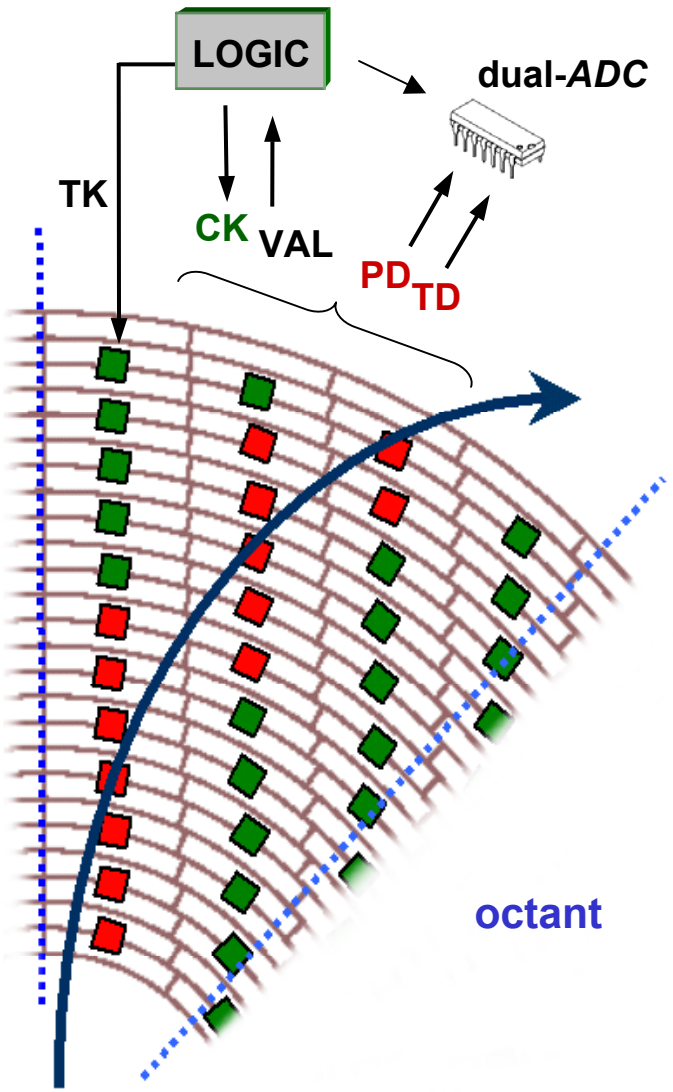
chip 1 – negative offset

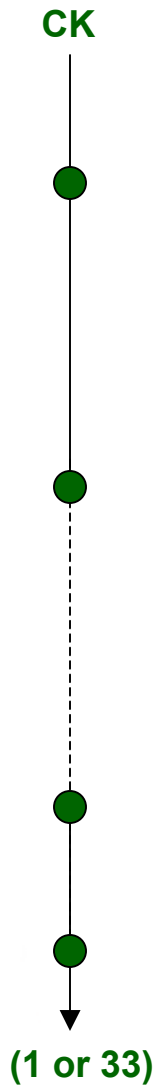


chip 2 – positive offset



Token Passing with Flag Readout





ToKen to **first chip**

check **VAL**ag (chip)

VAL low — **VAL high**

TK to first channel

check **VAL** (chan)

VAL low — **VAL high**

PD, TD to *ADC*

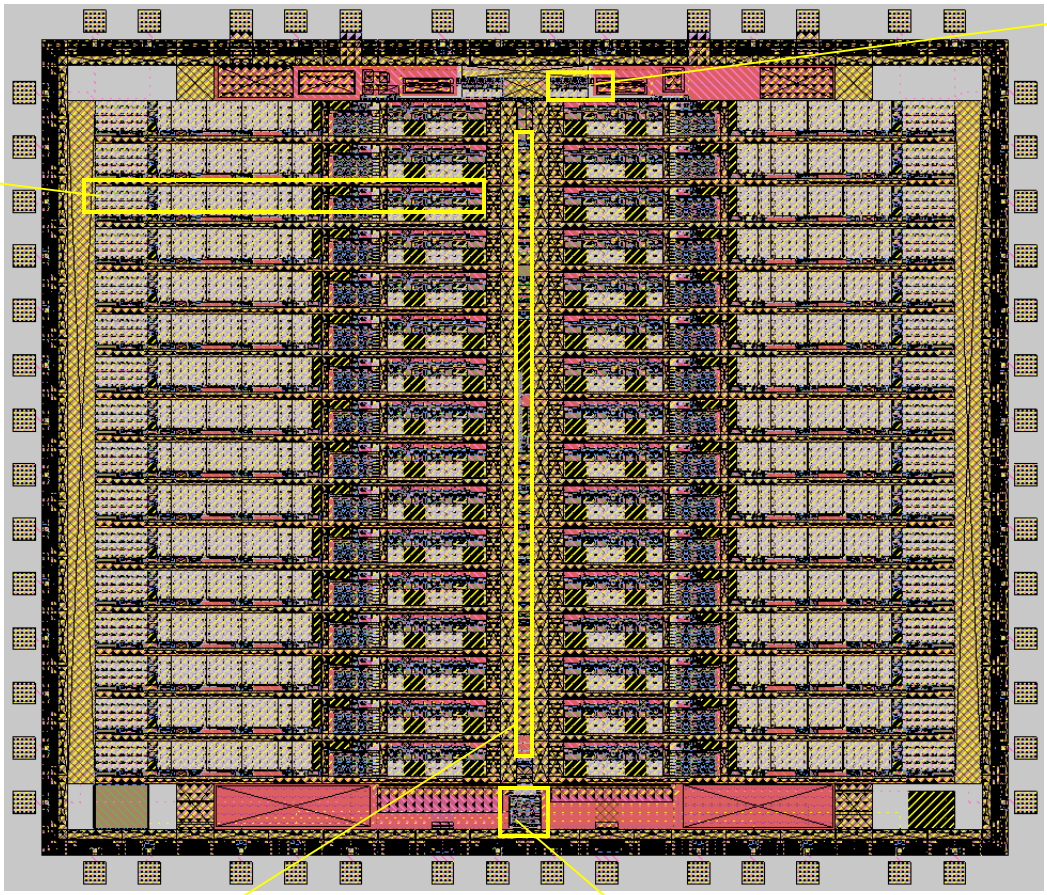
TK to **next** channel

:

TK to **last** channel

TK to **next chip**

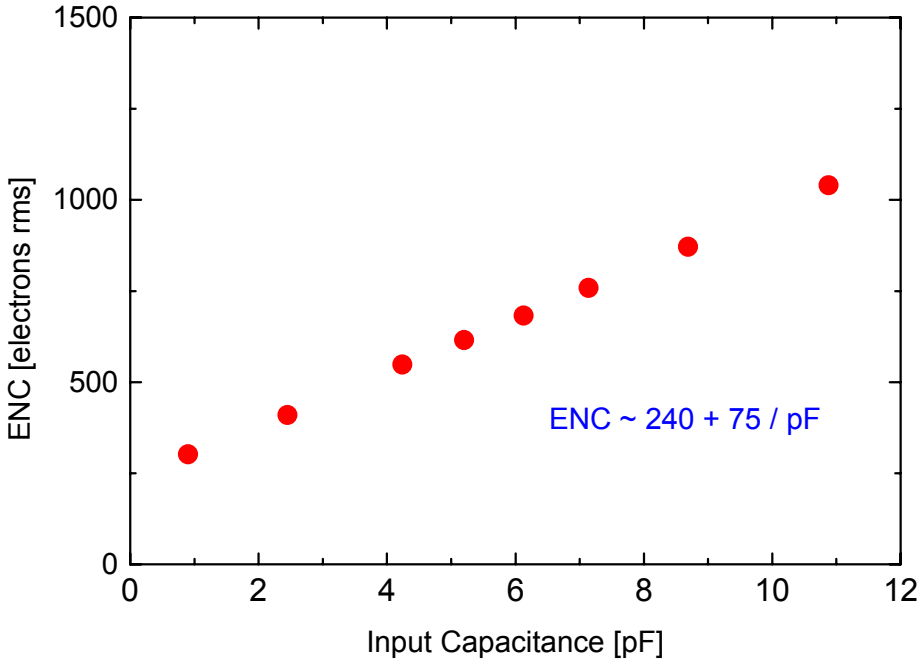
Layout



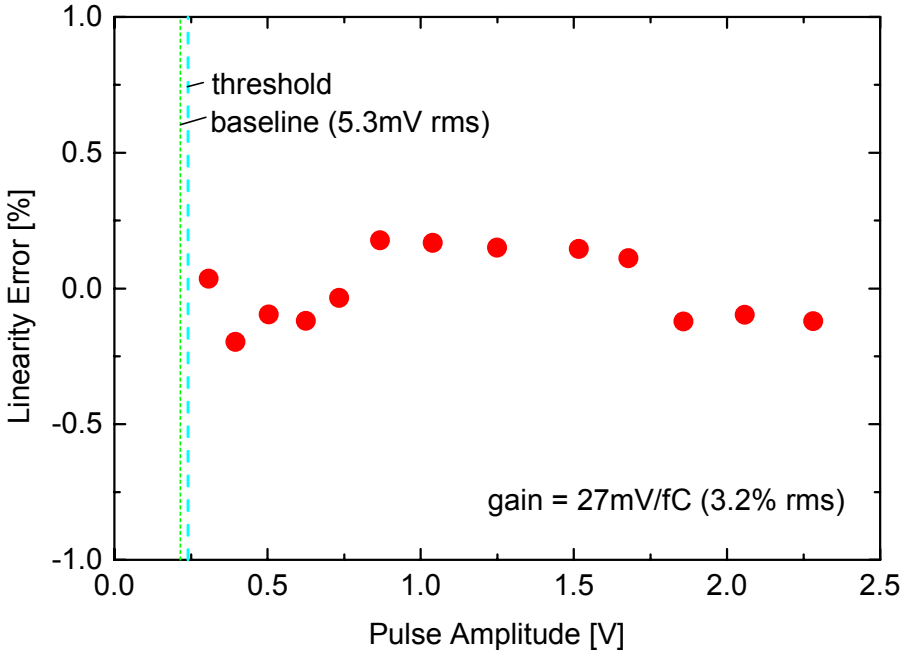
- TSMC 0.25µm
- 32 channels
- 3.1 x 3.6 mm²
- 47k MOSFETs
- 43mW
- QFN package (56)

Experimental Results

Energy Resolution

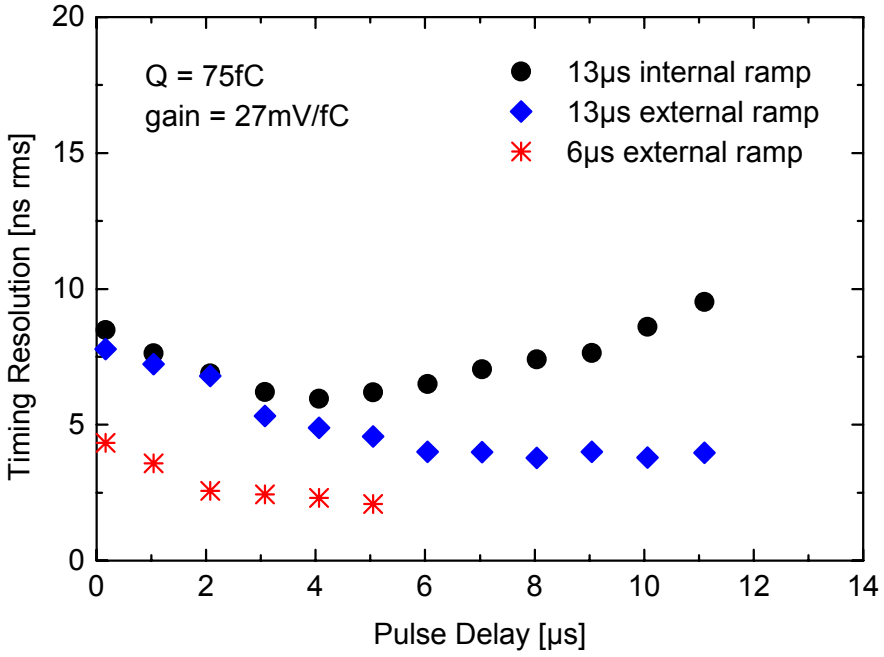


Linearity

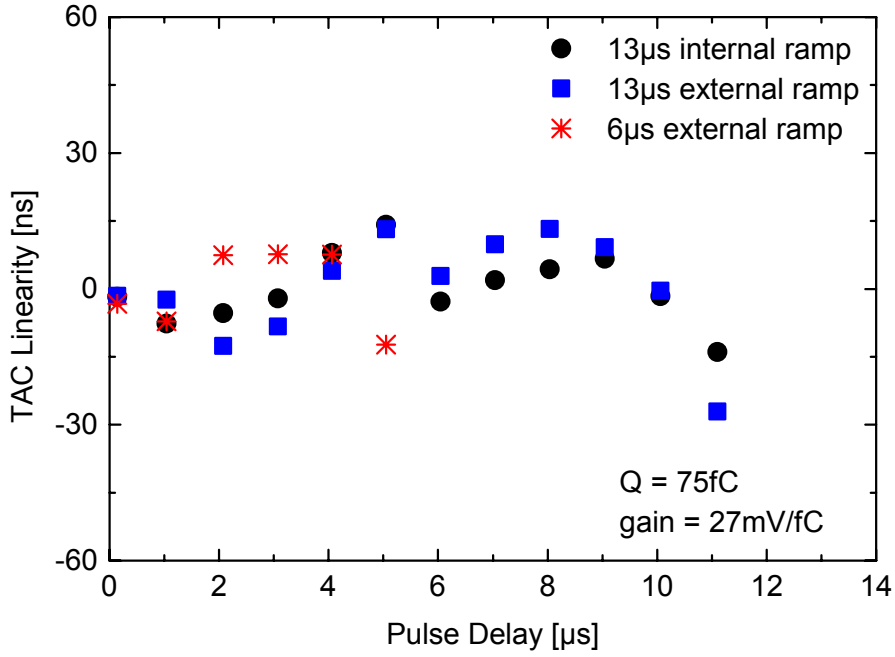


Experimental Results

Timing Resolution vs Delay

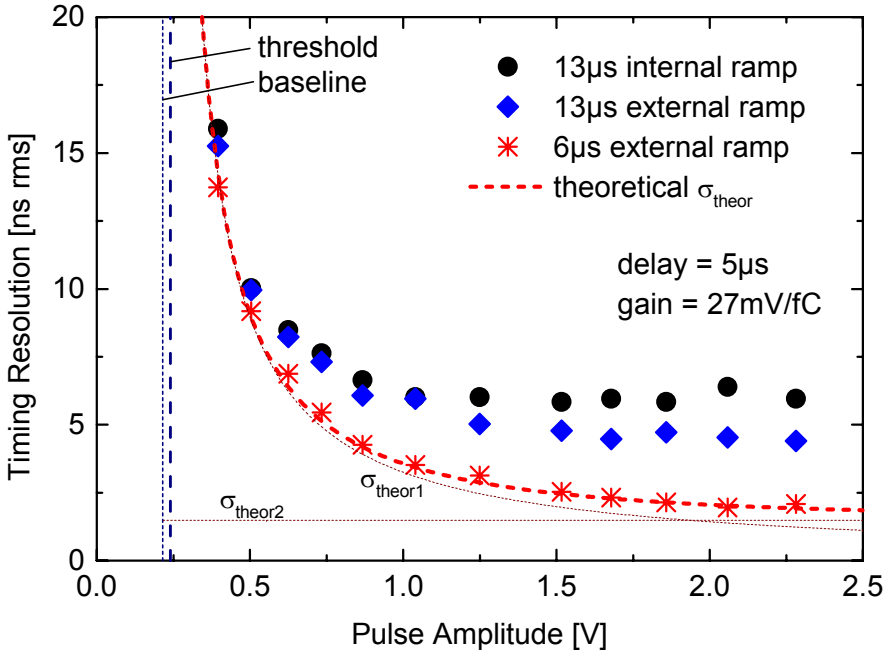


TAC Linearity

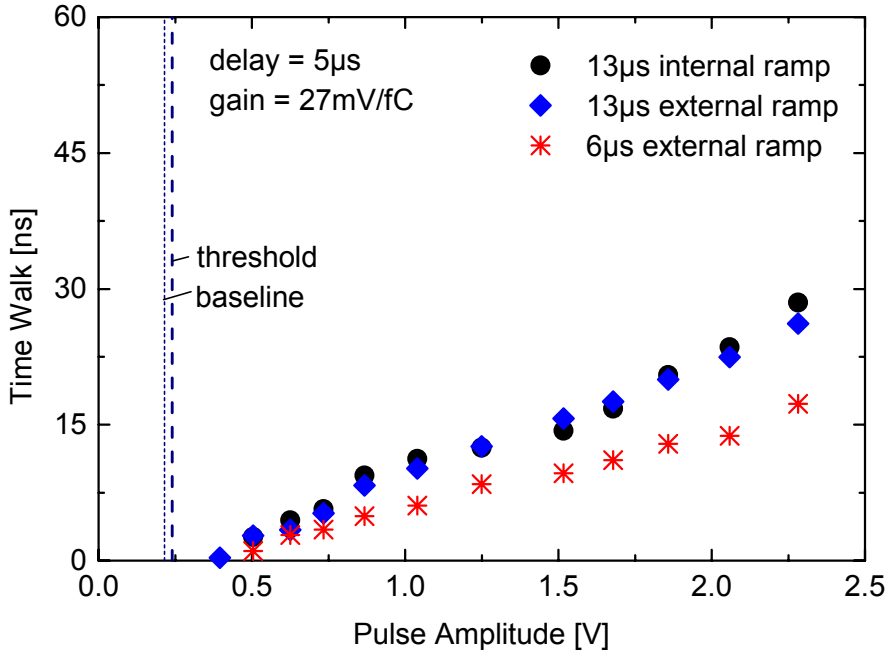


Experimental Results

Timing Resolution vs Energy

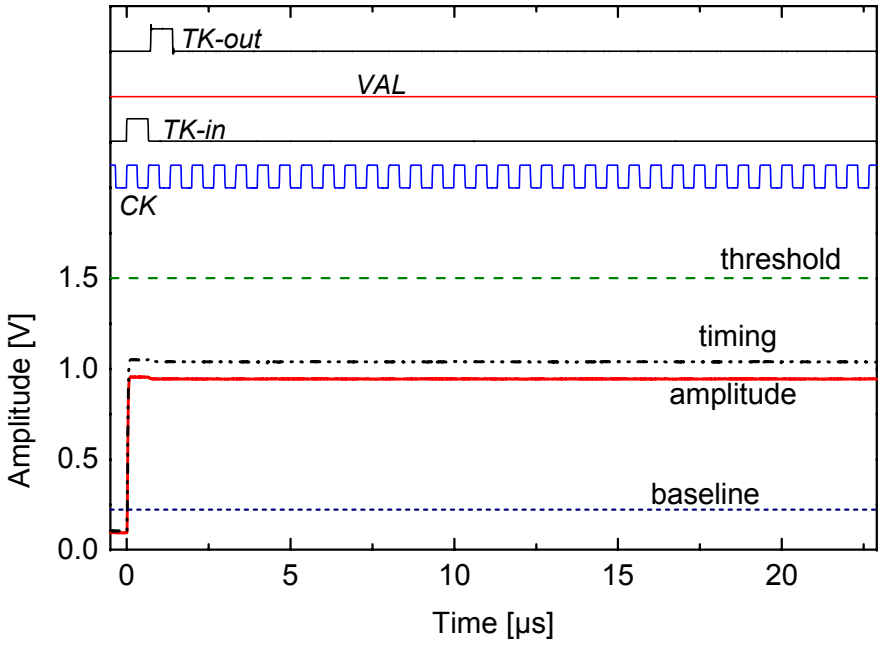


Time Walk

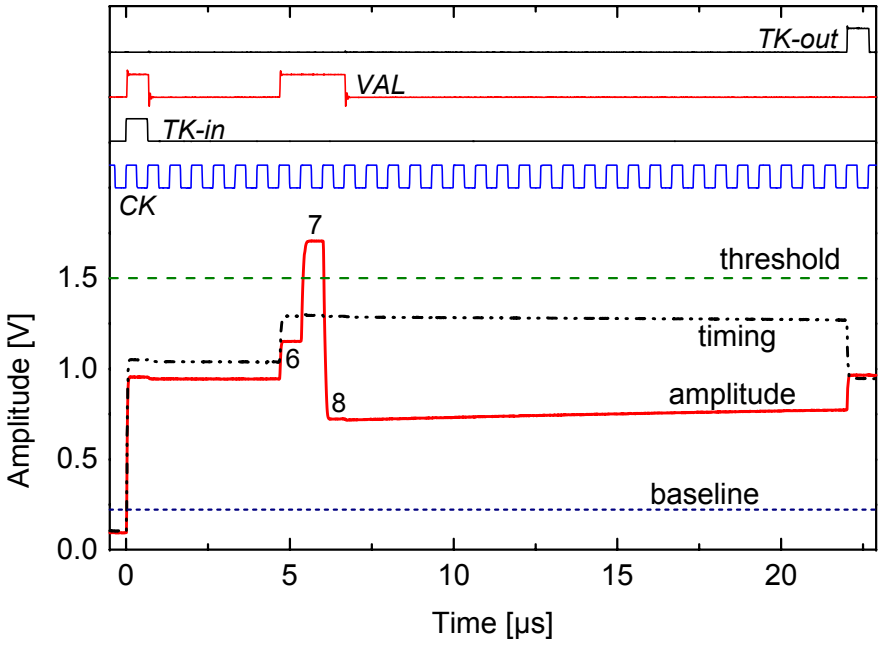


Experimental Results

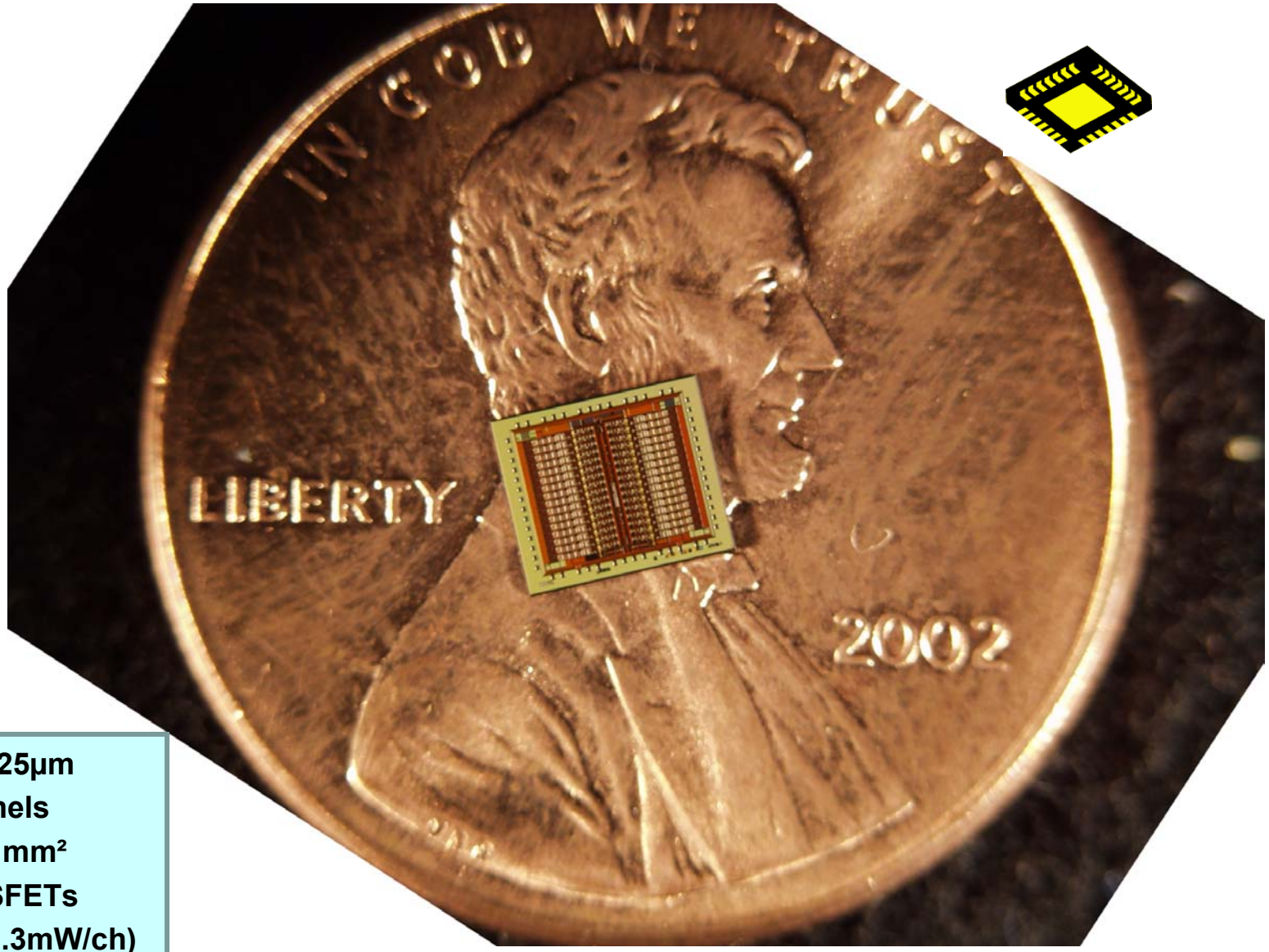
Readout – empty chip



Readout – data on chip



Die Photo



- TSMC 0.25µm
- 32 channels
- 3.1 x 3.6 mm²
- 47k MOSFETs
- 43mW (1.3mW/ch)
- QFN package (56)

Photo by Anand Kandasamy

Summary

- 32-channel front-end ASIC for TPC
- Energy measurement
- Timing measurement
- Neighbor channel enabling
- High-linearity low-voltage continuous reset
- High-accuracy two-phase peak detector
- Token passing with flag sparsifying readout

Acknowledgment

- Anand Kandasamy and John Triolo – Instrum. Div. , BNL
- DOE