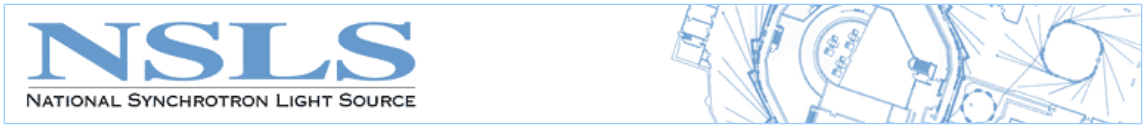

High-Rate, High-Resolution Detector for EXAFS Experiments

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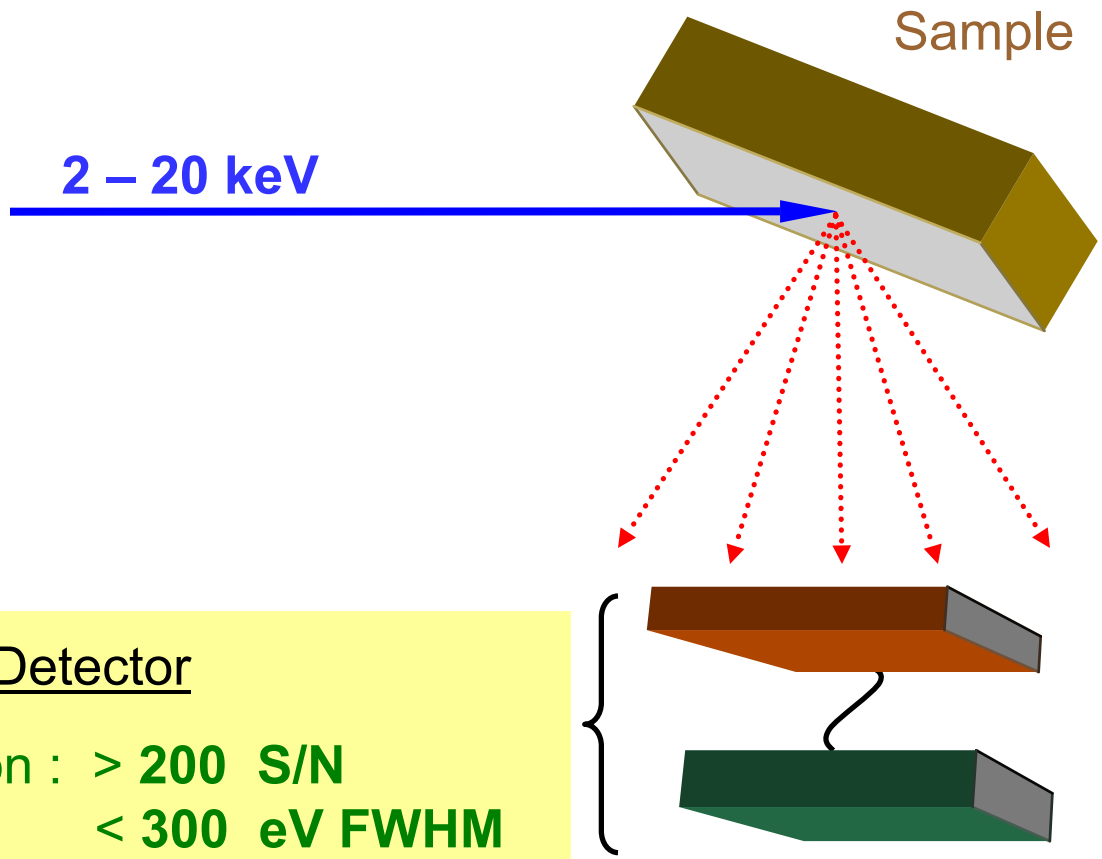
Anthony J. Kuczewski, D. Peter Siddons
***National Synchrotron Light Source**, Brookhaven National Laboratory, Upton, NY*

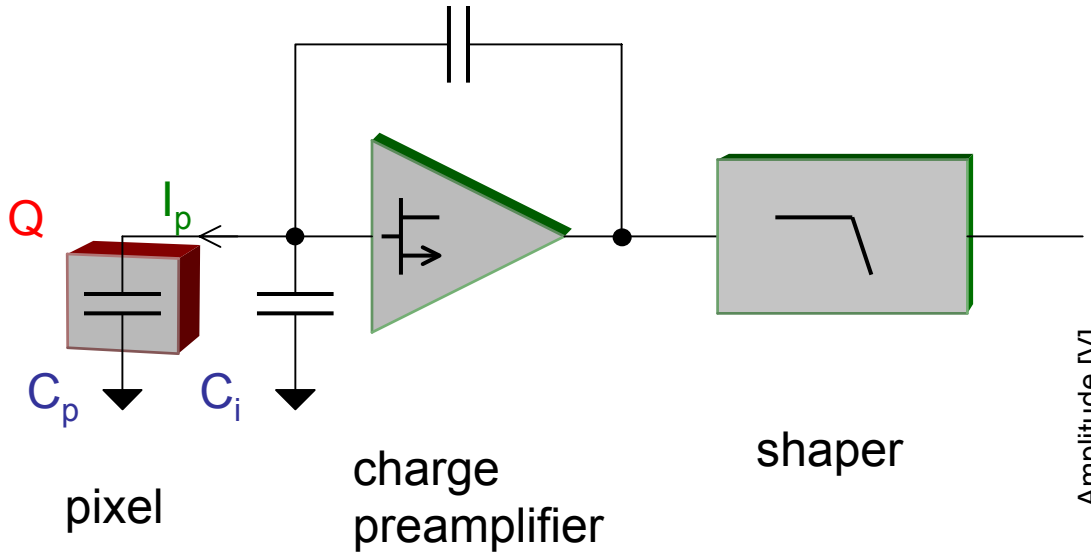
Typical fluorescence EXAFS spectroscopy geometry



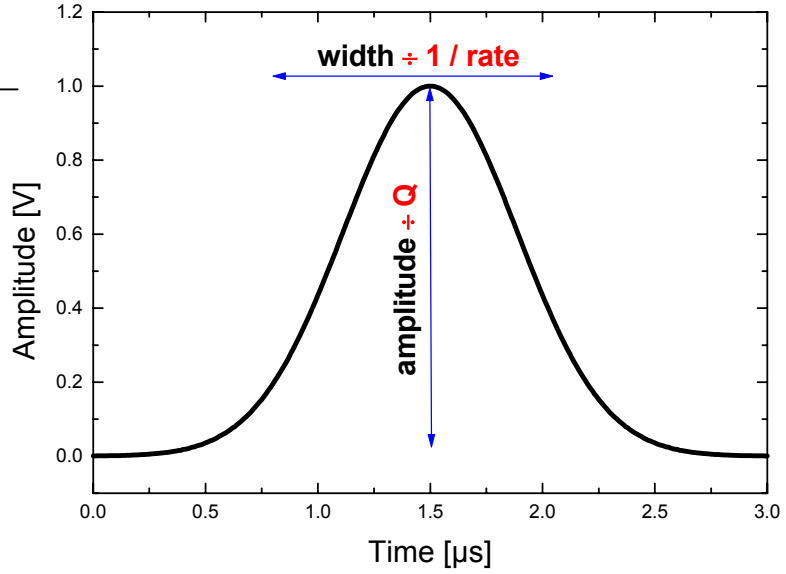
Detector

- Resolution : > **200 S/N**
  < **300 eV FWHM**
- Rate : ≈ **10 MHz/cm²**
  ≈ **100 kHz/pixel**
- Spectroscopy (energy windows)

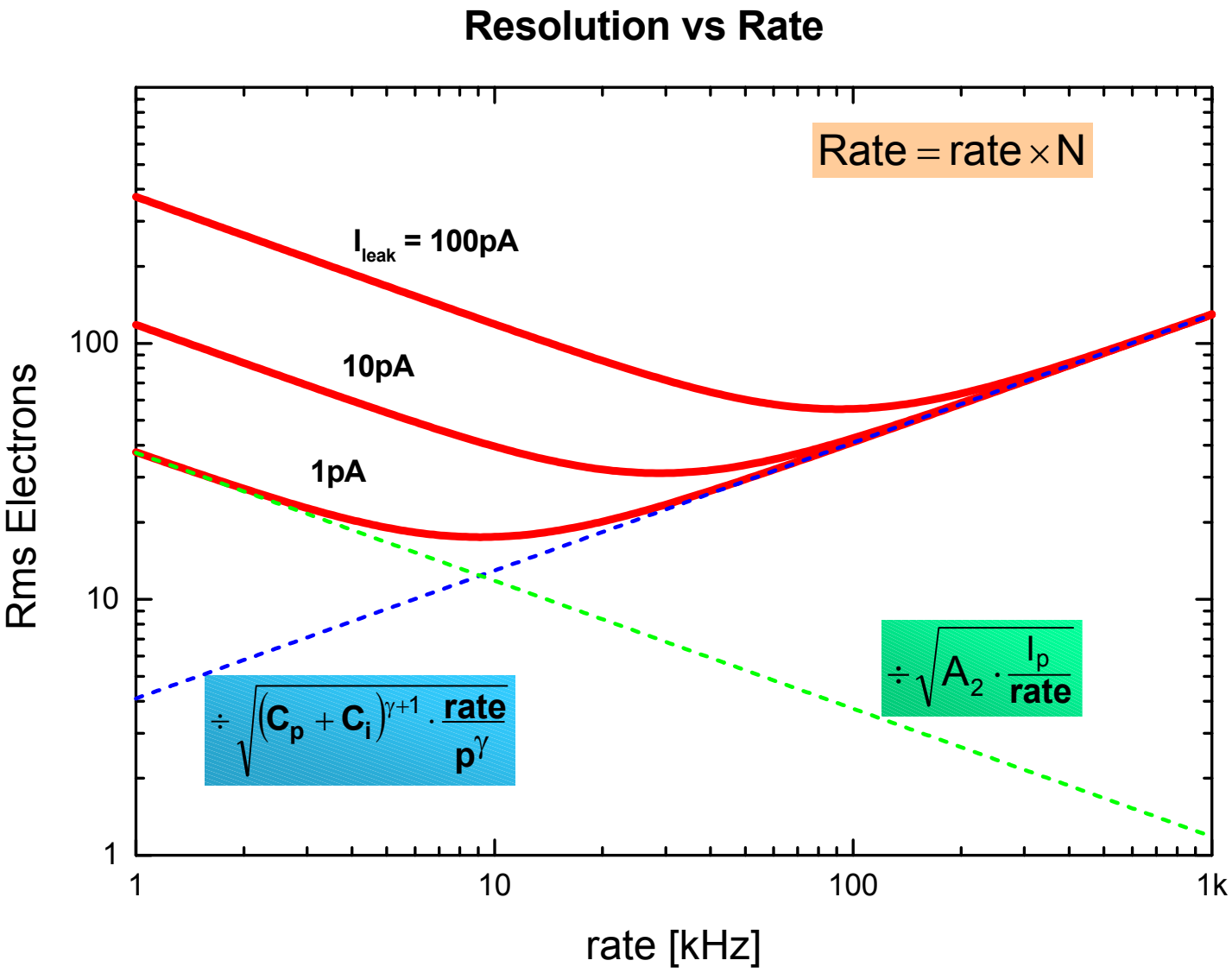
Resolution vs Rate



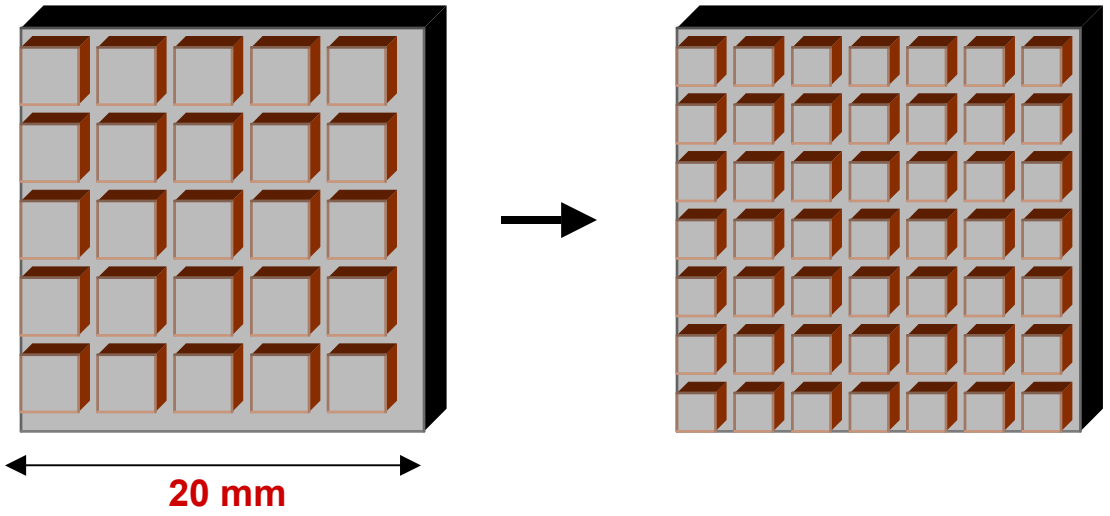
$$\text{rate} = \frac{\text{Rate}}{N} \quad (N = \text{number of pixels})$$



$$ENC^2 = A_1(\gamma)\left(C_p + C_i\right)^{\gamma+1}\frac{\text{rate}}{p^{\gamma}} + A_2\frac{I_p}{\text{rate}} \qquad 0 < \gamma < 1$$

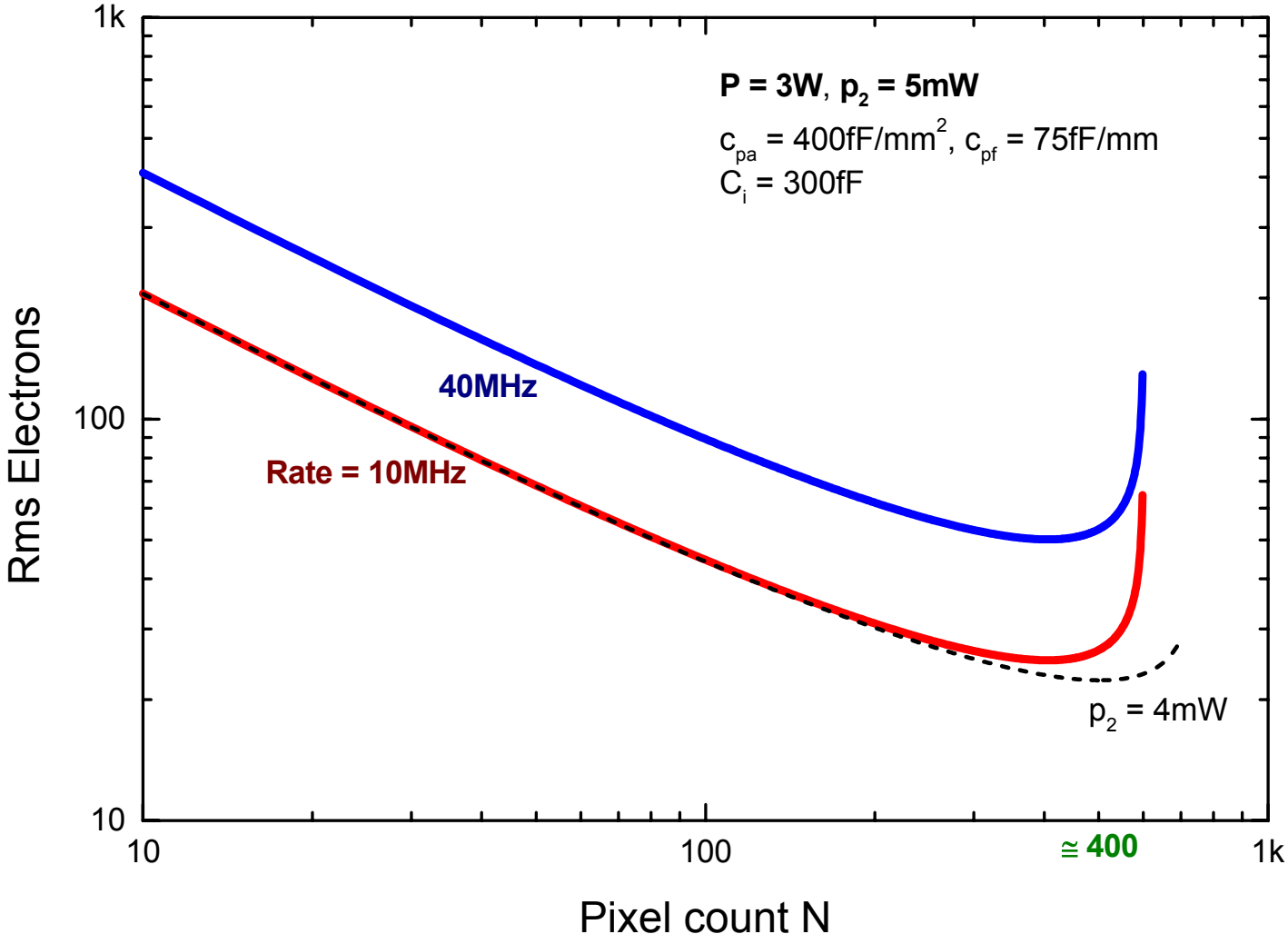

Resolution vs Rate
Rate = rate × N
I_leak = 100pA
10pA
1pA
100
10
1
Rms Electrons
1
10
100
1k
rate [kHz]
÷ √((C_p + C_i)^(γ+1) · rate / p^γ)
÷ √(A_2 · I_p / rate)

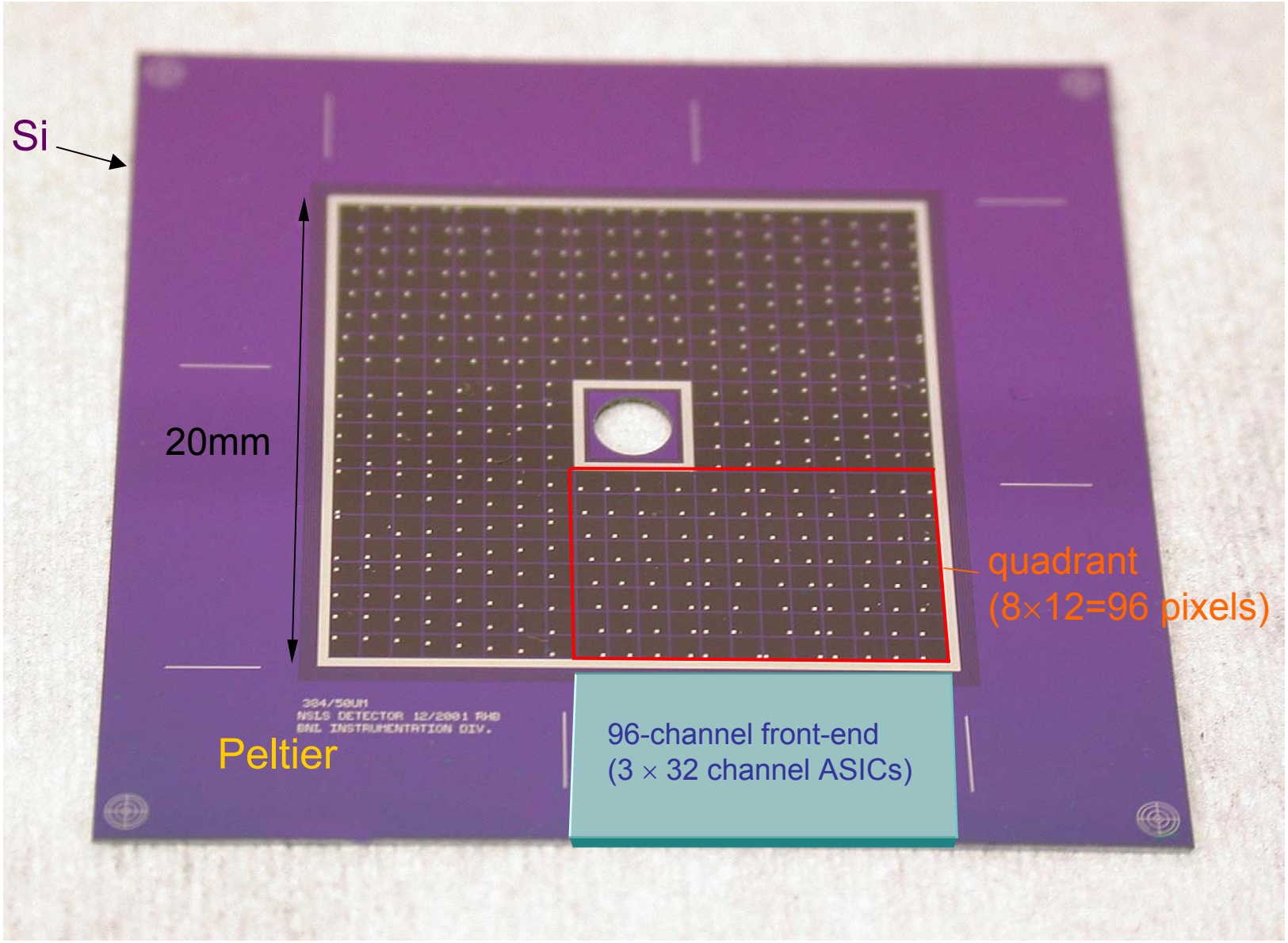
Optimum pixellation



$$ENC^2 \div \left(C_p(N) + C_i\right)^{\gamma+1} \frac{\frac{\text{Rate}}{N}}{\left(\frac{P}{N} - p_2\right)^{\gamma}}$$

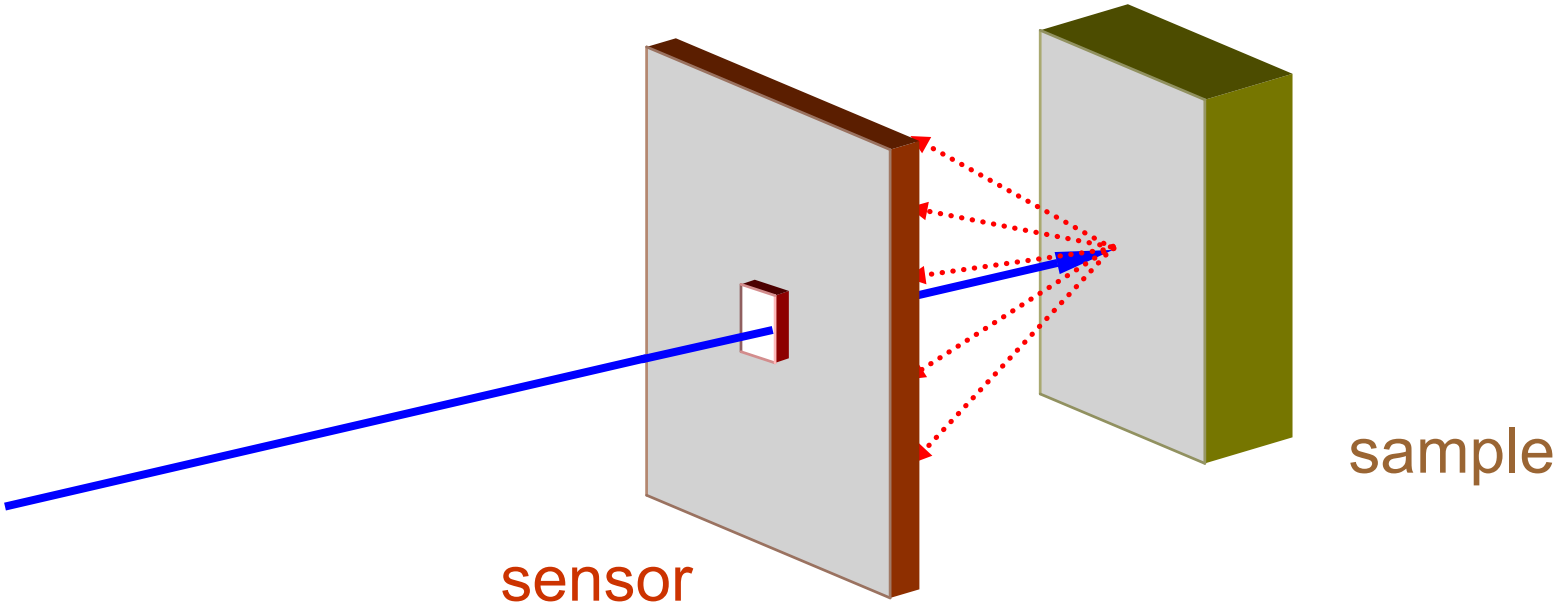
Optimum Pixellation



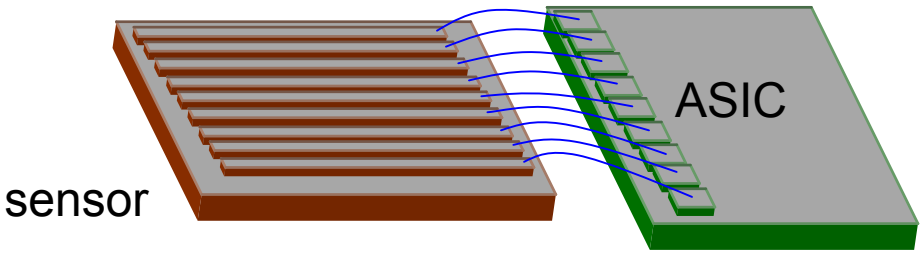


Si n-type high resistivity wafer 250μm thick,
N = 384 p^+ ≈1mm×1mm pixels, C_p ≈ 700-1000fF
Versions with gaps of 10μm, 20μm, 50μm

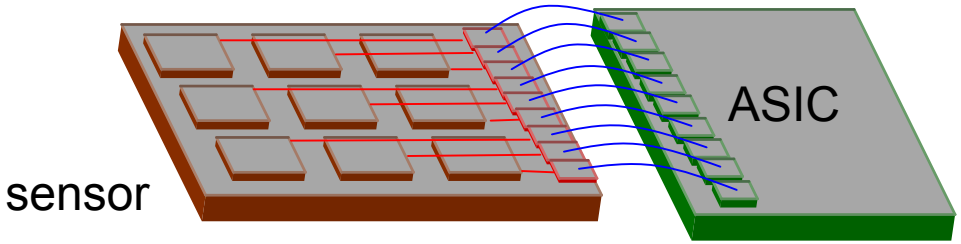
Beam through



Interconnecting pixel to front-end electronics

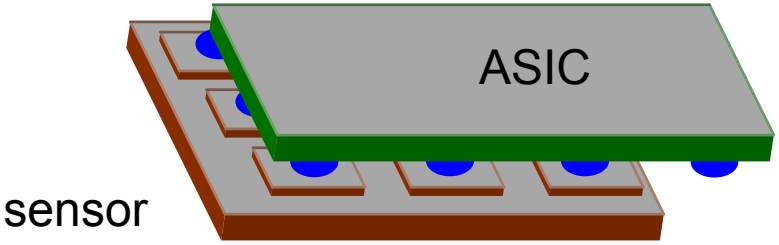


+ interconnect parasitic
+ bond length
- fringe capacitance
- charge sharing and trapping

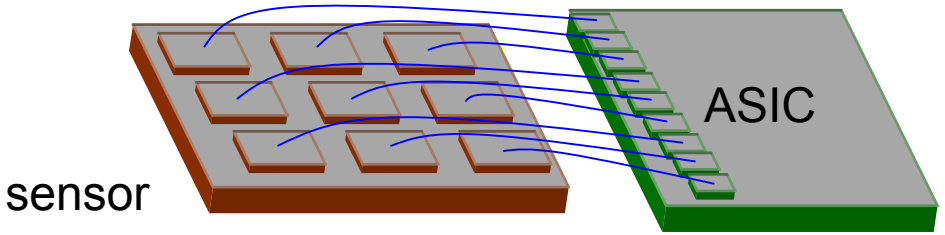


+ bond length
- interconnect parasitic
- dielectric losses

6mm×10µm, Si_3N_4 (ε_r=6.5,$tan(\delta) \approx$ 1m), 3µm, δ**$C_i \approx$1.2pF**
δ**$FWHM_{loss}$** = 8.5/q·$\sqrt{(2kTC_i tan(\delta))} \approx$ **180eV**

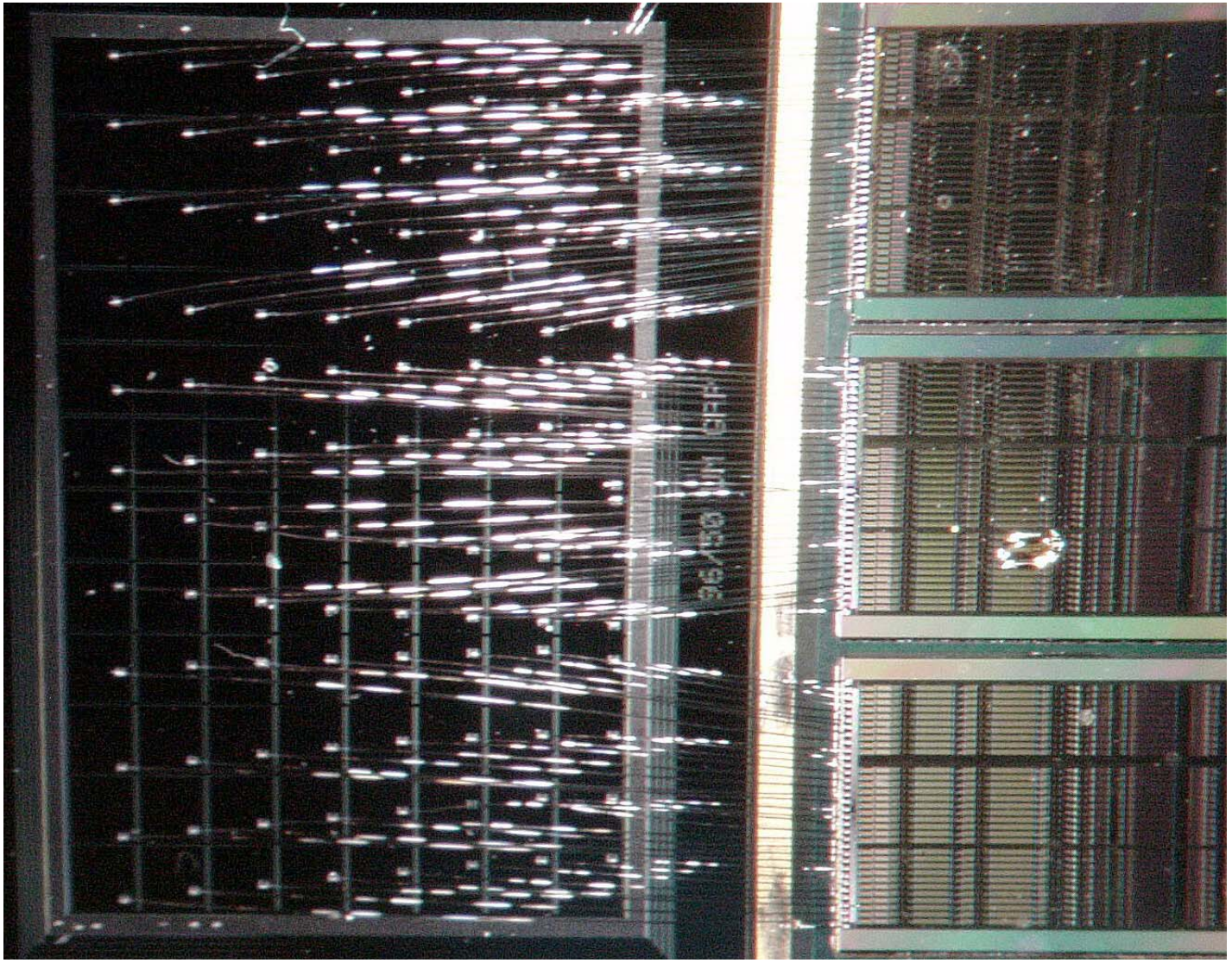


+ interconnect parasitic
- constraint on ASIC area and layout
- fluorescence from Pb (Sn/Pb/Ag)
- illumination from segmented side



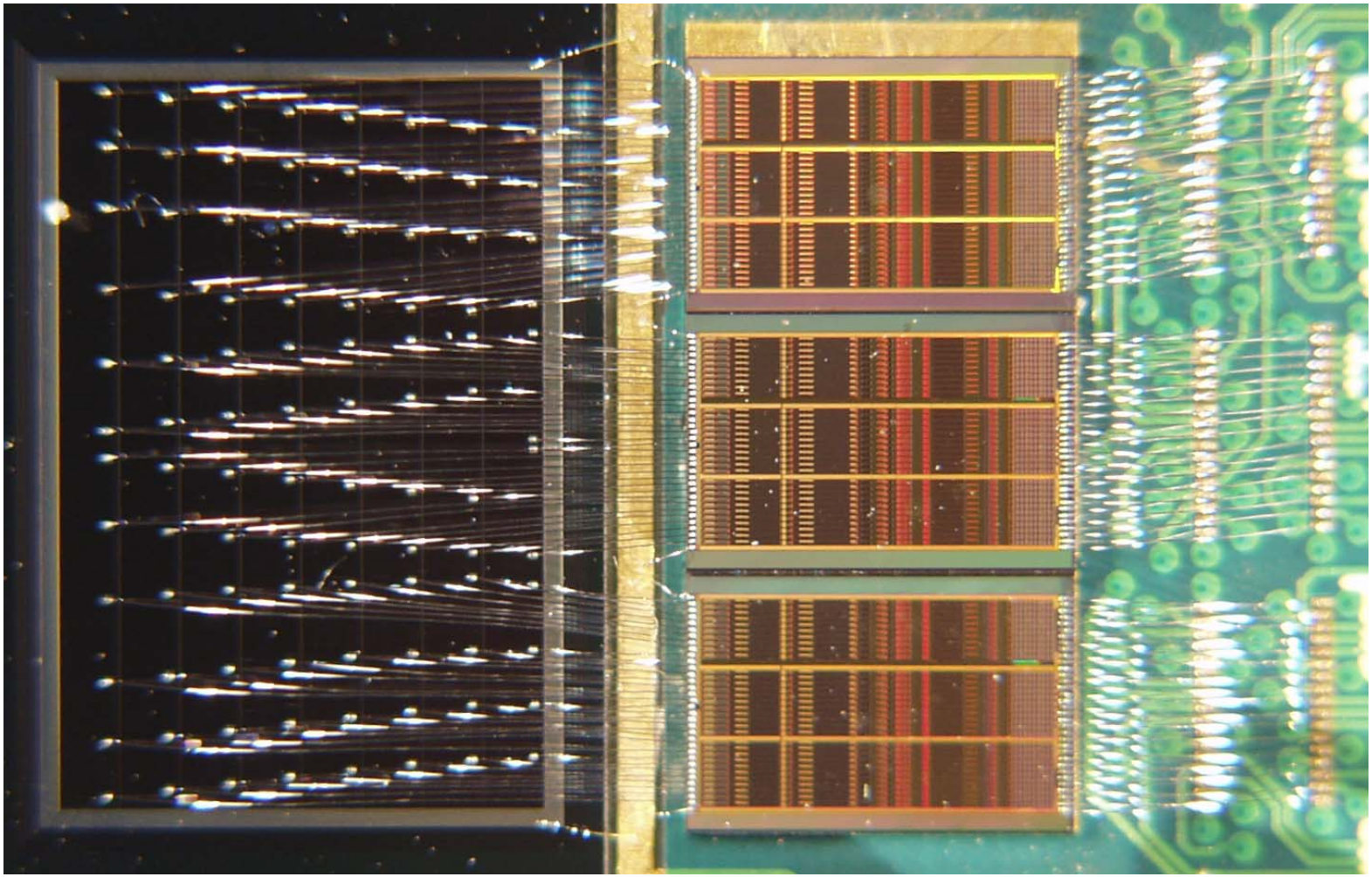
+ dielectric losses
± interconnect parasitic
- bond length

Sensor – ASIC photo



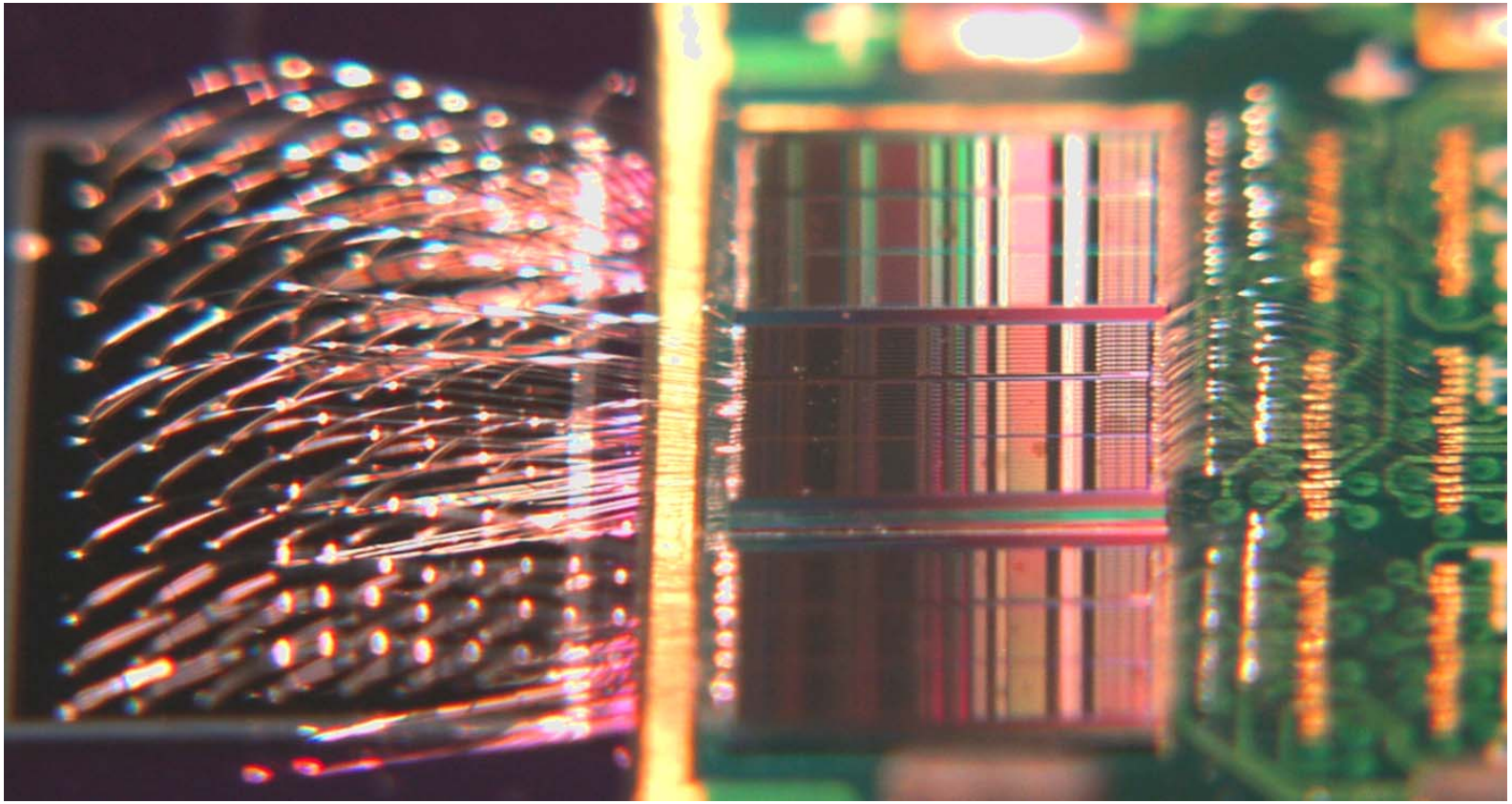
one quadrant

Sensor – ASIC photo



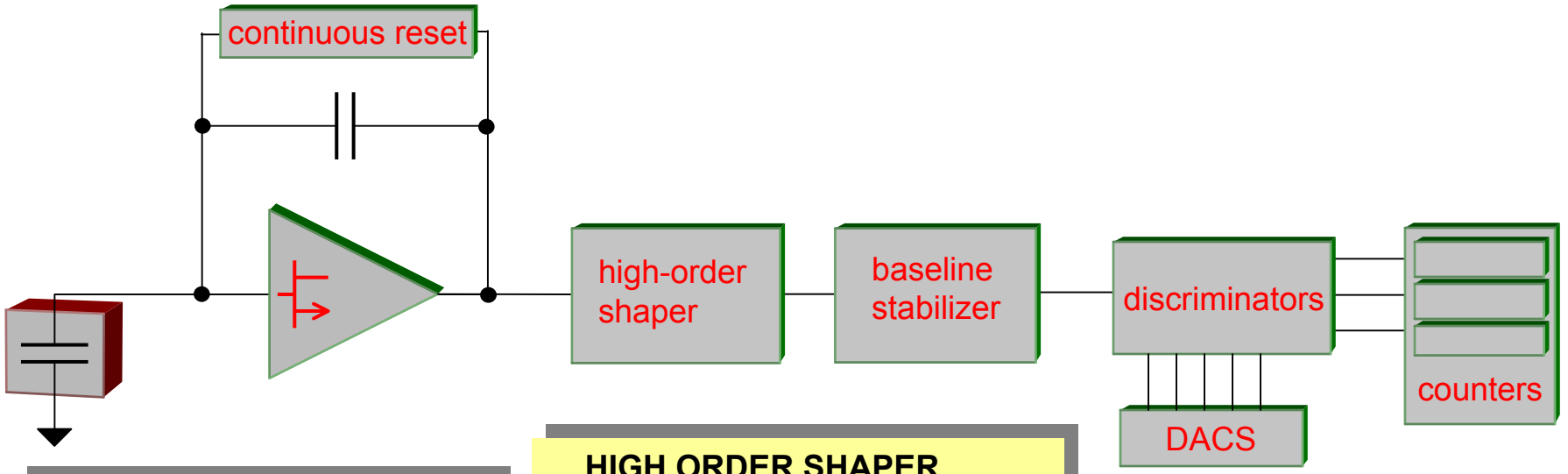
one quadrant

Sensor – ASIC photo



one quadrant

ASIC channel overview



INPUT p-MOSFET
- optimized for operating region
- NIM A480, p.713

CONTINUOUS RESET
- feedback MOSFET
- self adaptive sub-pA - nA
- low noise < 3.5e$^-$ rms @ 1μs
- highly linear < 0.2% FS
- US patent 5,793,254
- NIM A421, p.322
- TNS 47, p.1458

≈ 3 mW

HIGH ORDER SHAPER
- amplifier with passive feedback
- 5th order complex semigaussian
- 2.6x better resolution vs 2nd order
- TNS 47, p.1857

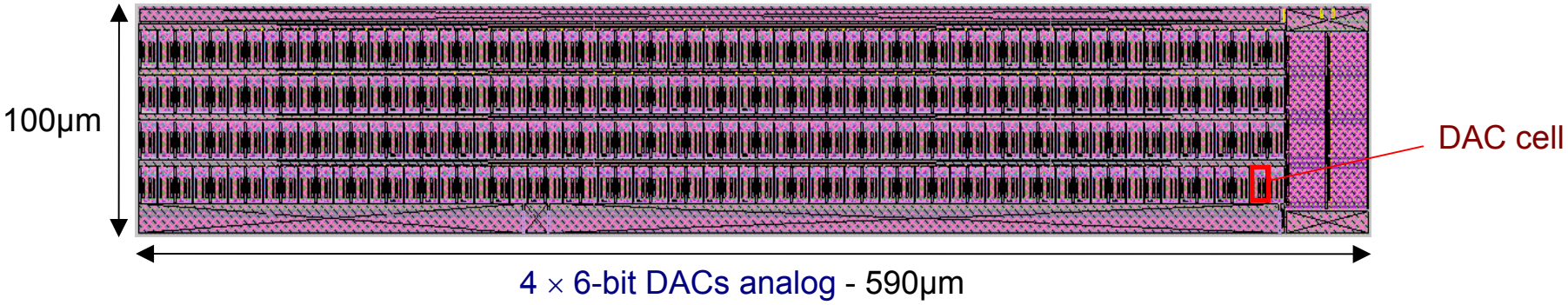
BASELINE STABILIZER (BLH)
- low-frequency feedback, BGR
- slew-rate limited follower
- DC and high-rate stabilization
- dispersion < 3mV rms
- stability <2mV rms @ rt×tp<0.1
- TNS 47, p.818

DISCRIMINATORS
- five comparators
- 1 threshold + 2 windows
- four 6-bit DACs (1.6mV step)
- dispersion (adj) < 2.5e$^-$ rms

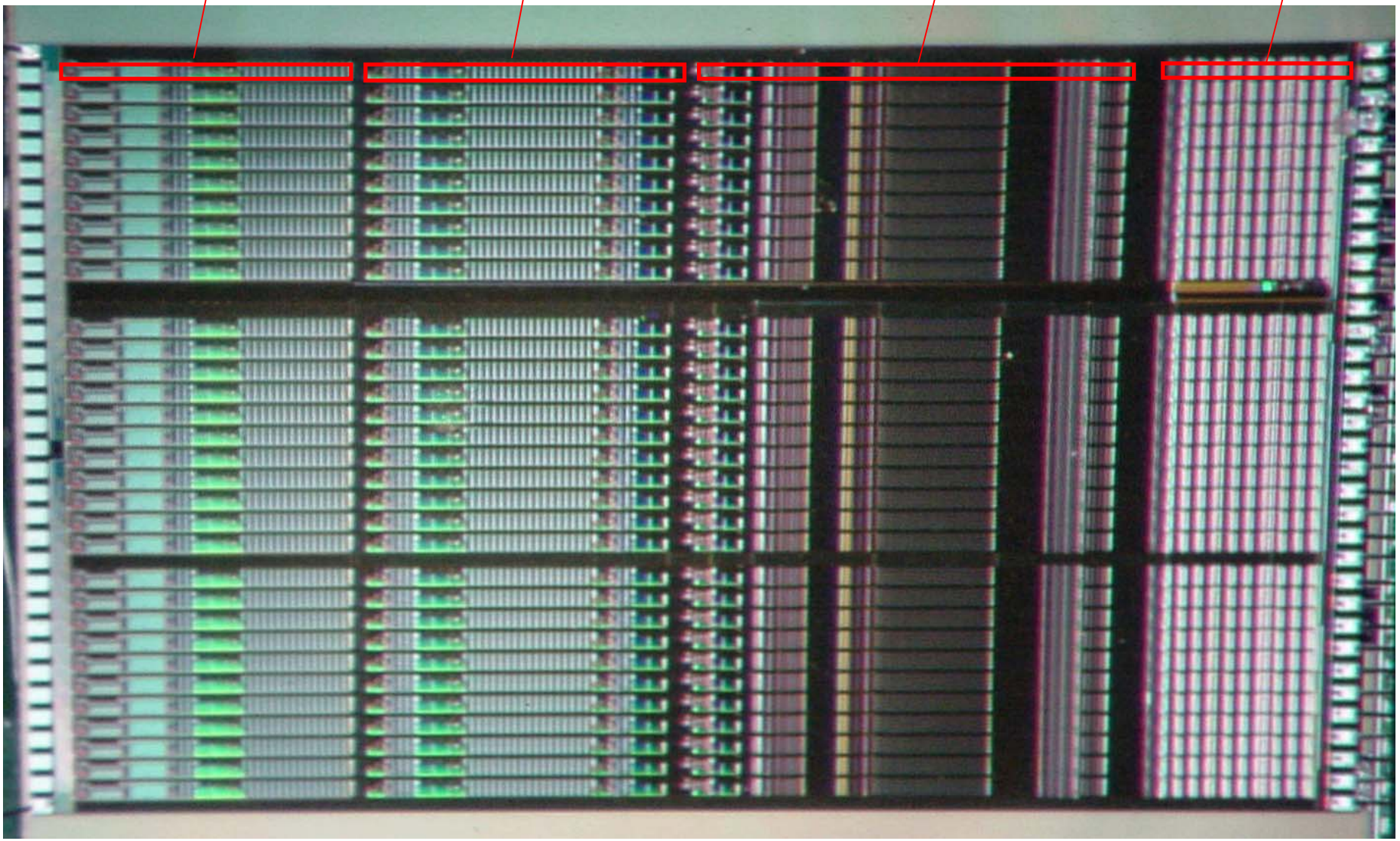
COUNTERS
- three (one per discriminator)
- 24-bit each

≈ 5 mW

ASIC layout cells



ASIC photo

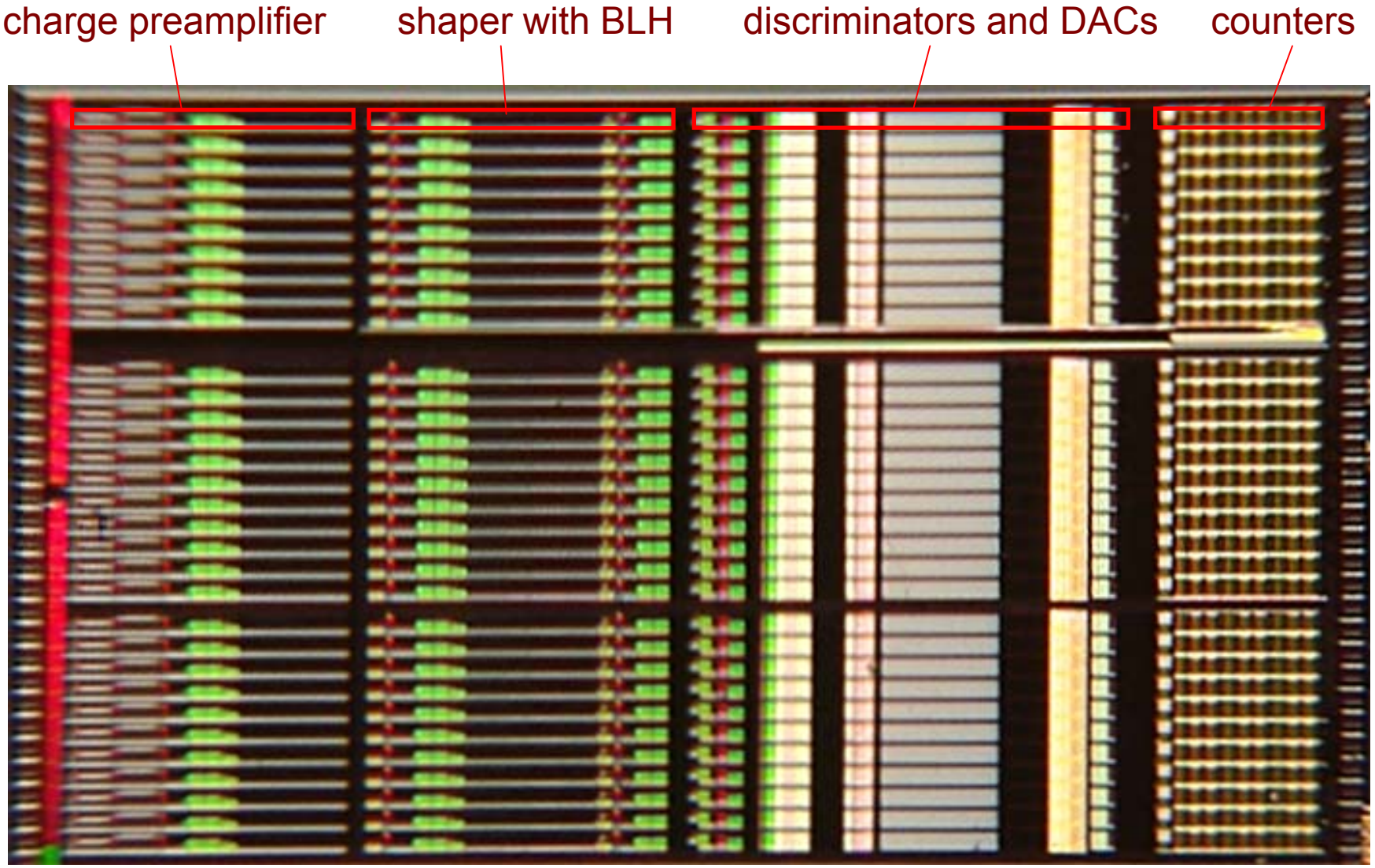


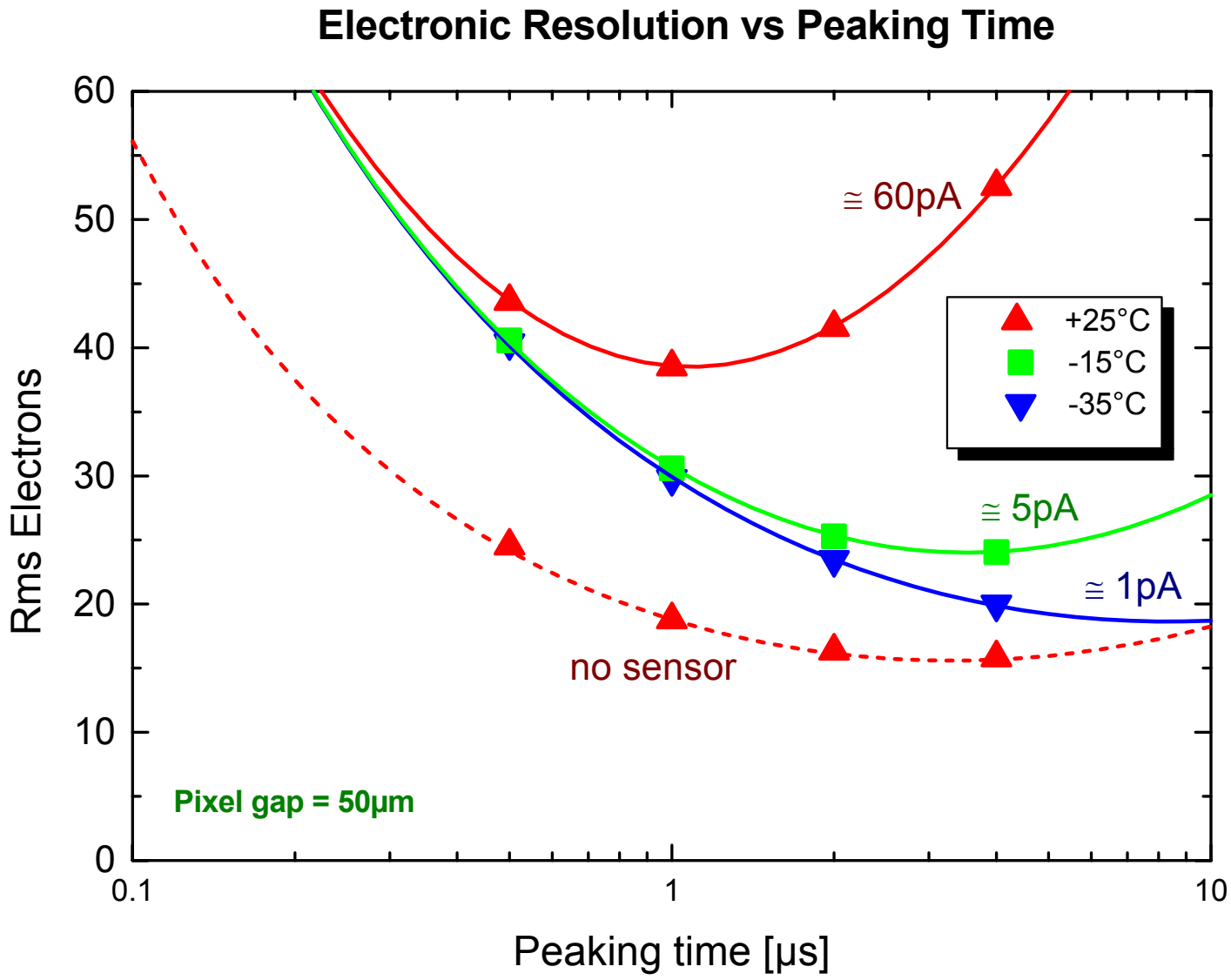
32 channels, 3.6 × 6.3 mm²

ASIC photo

32 channels
3.6 × 6.3 mm²
0.35µm CMOS

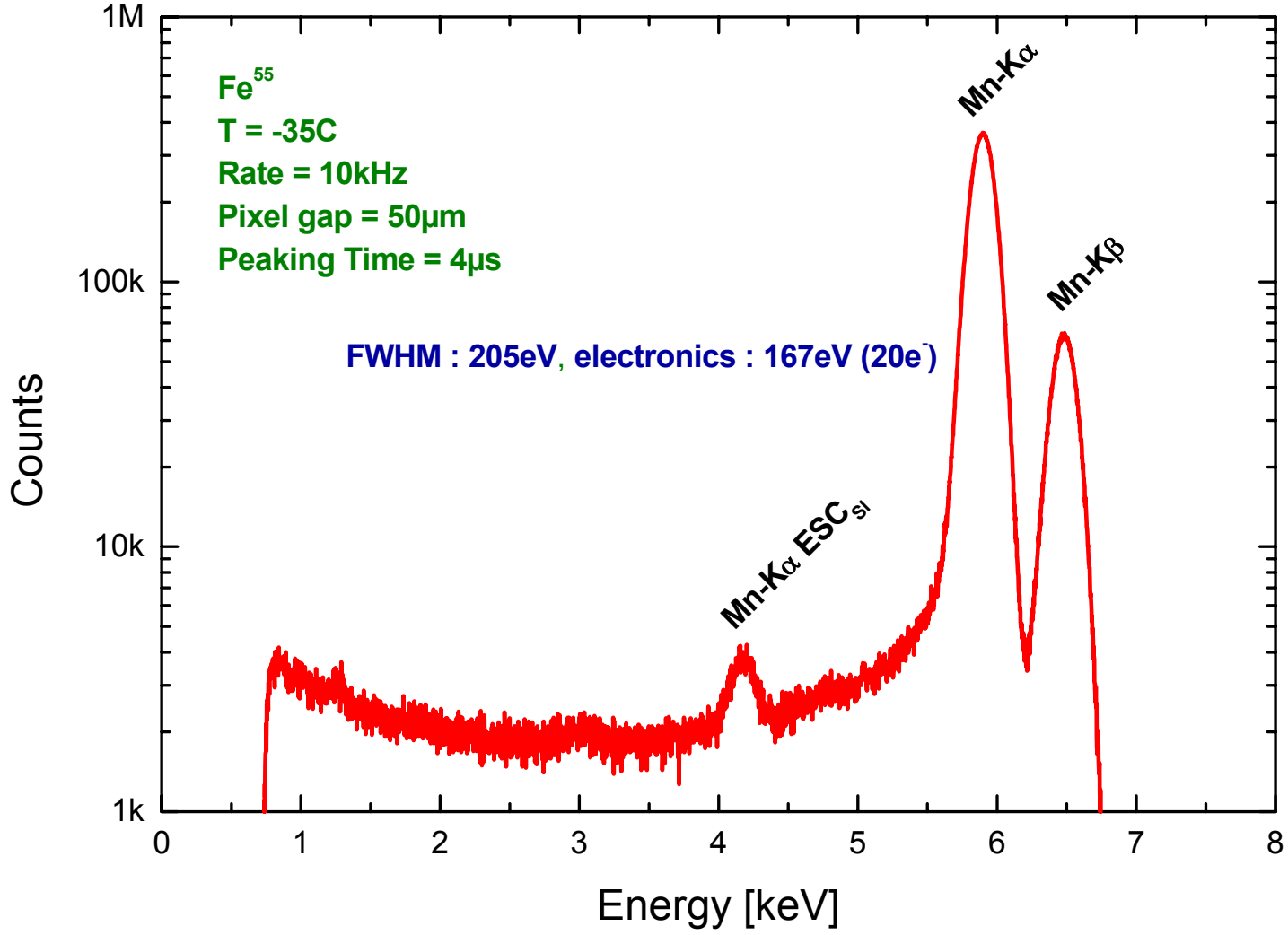
ASIC photo


charge preamplifier
shaper with BLH
discriminators and DACs
counters

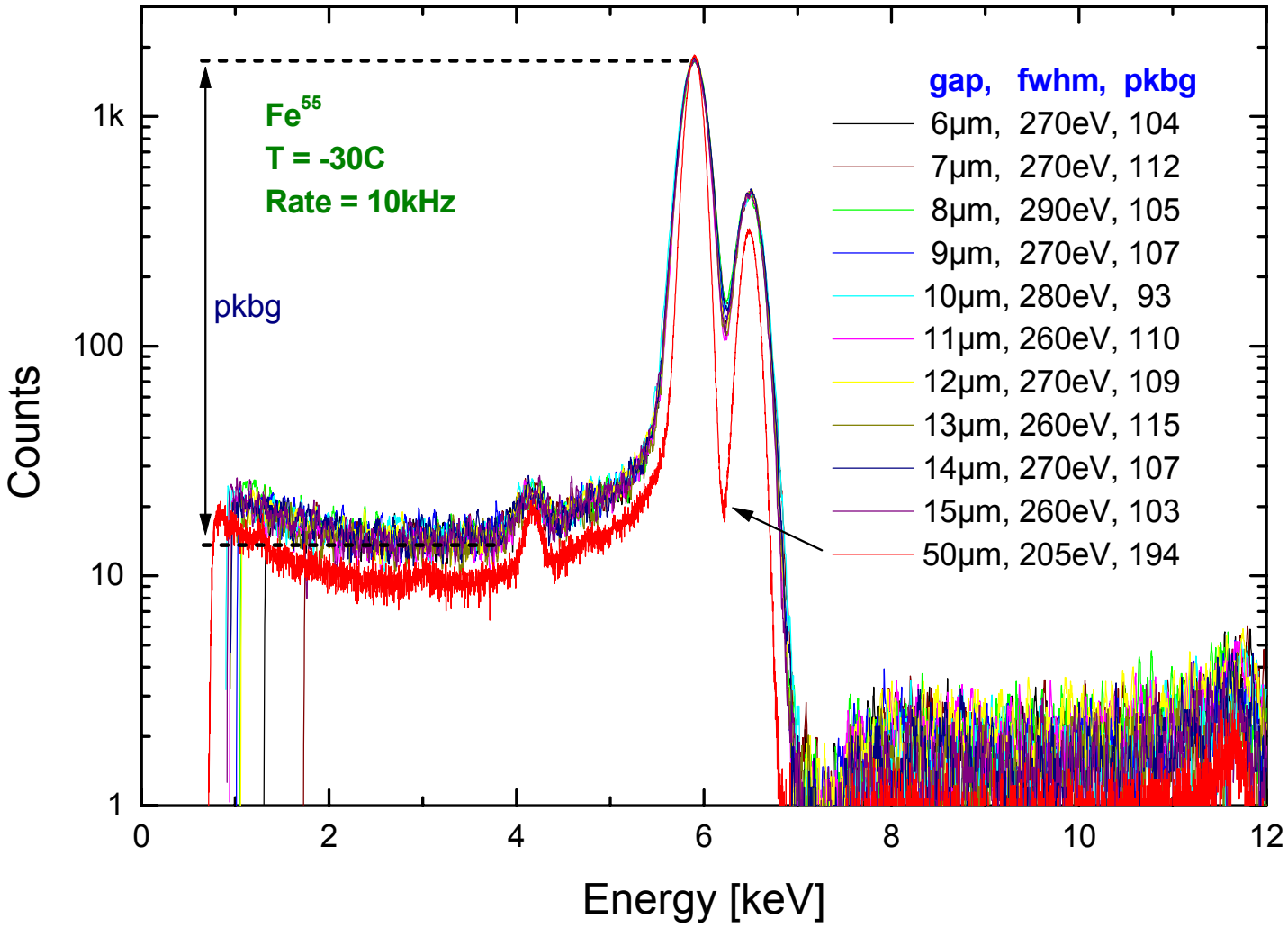


$C_p \approx 700fF$, $C_{i\text{-}bond} \approx 50\text{-}200fF$, $C_{i\text{-}pad} \approx 220fF$

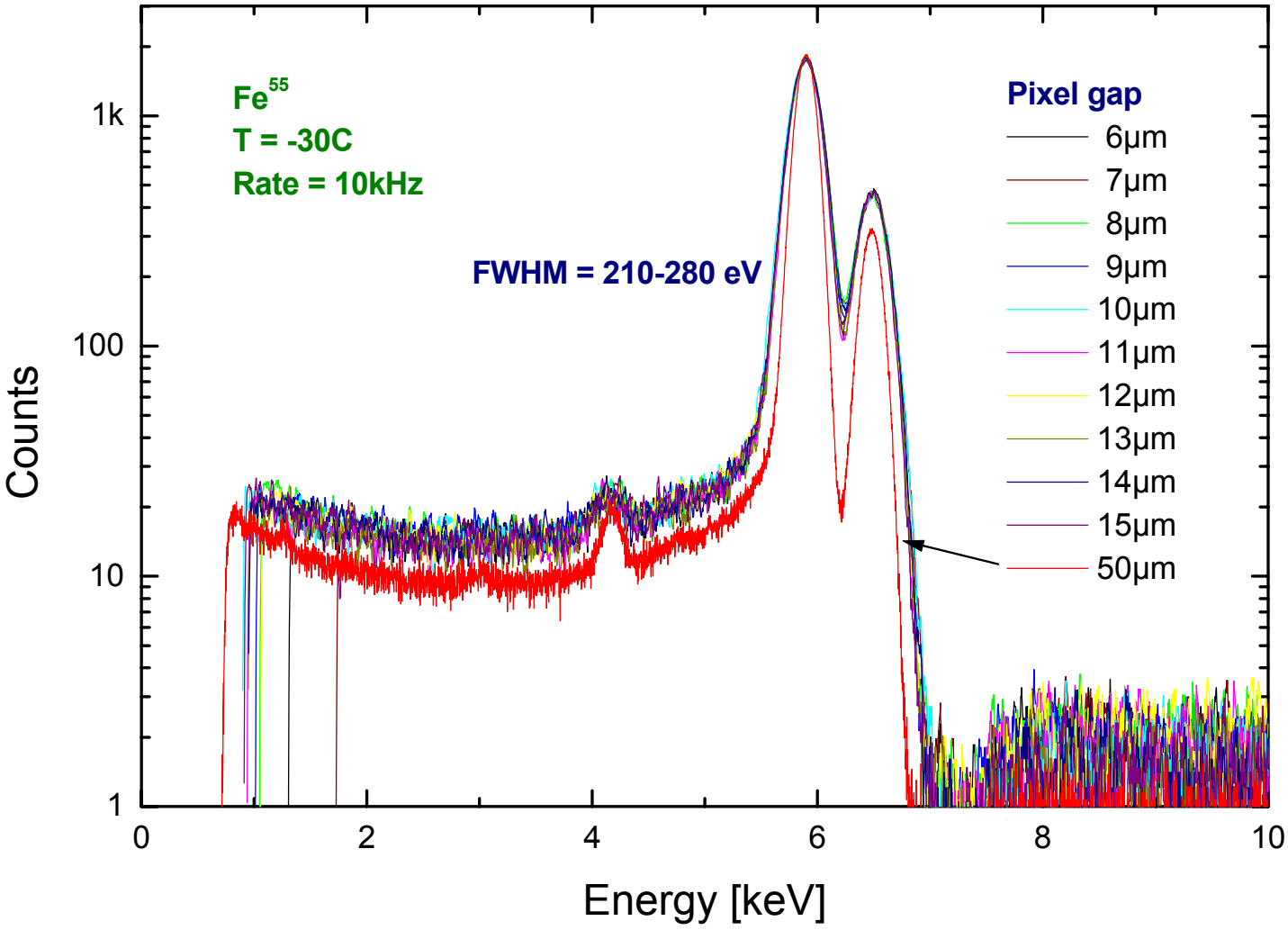
Energy Resolution - single channel



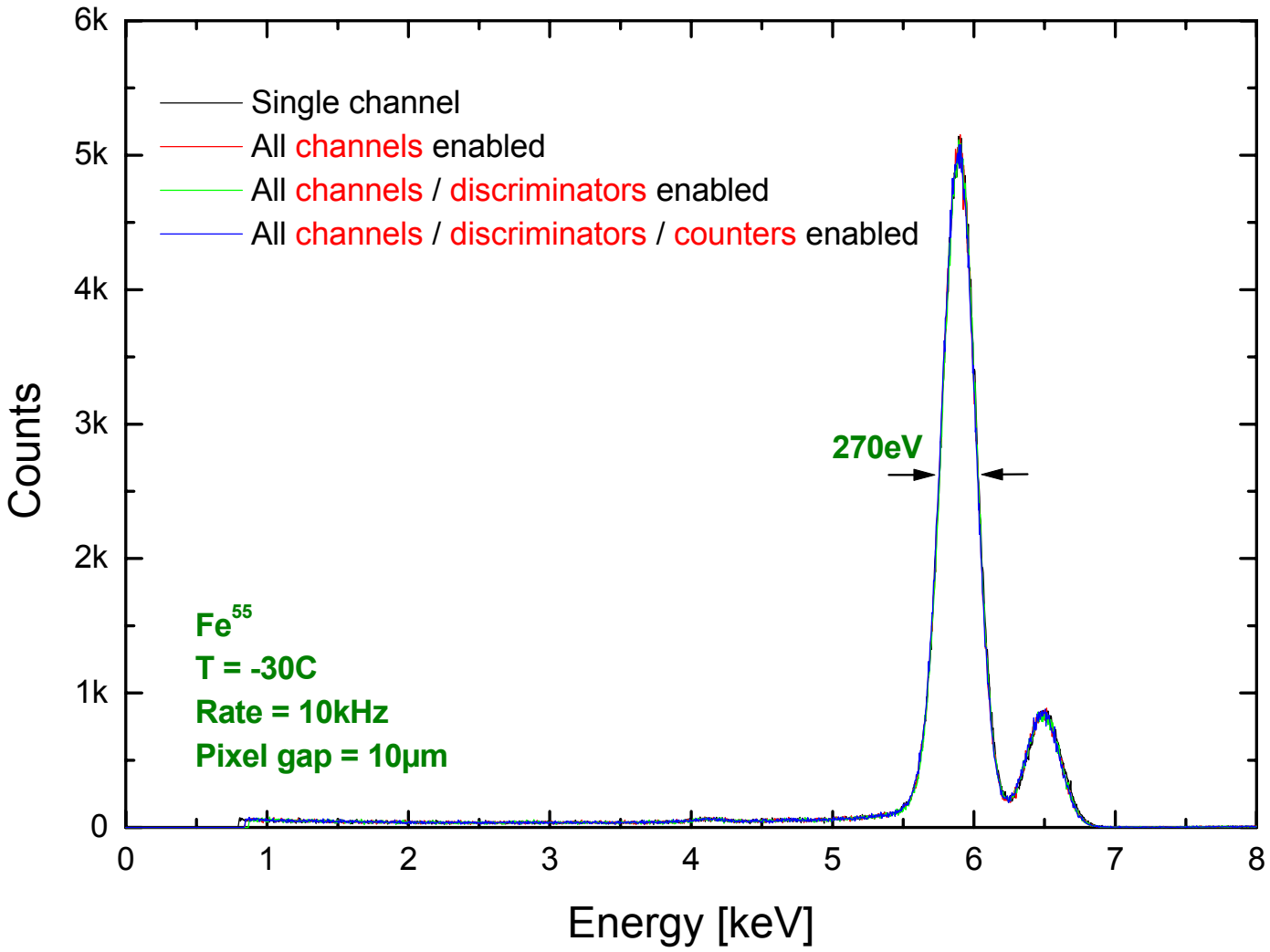
Energy Resolution vs Pixel Gap

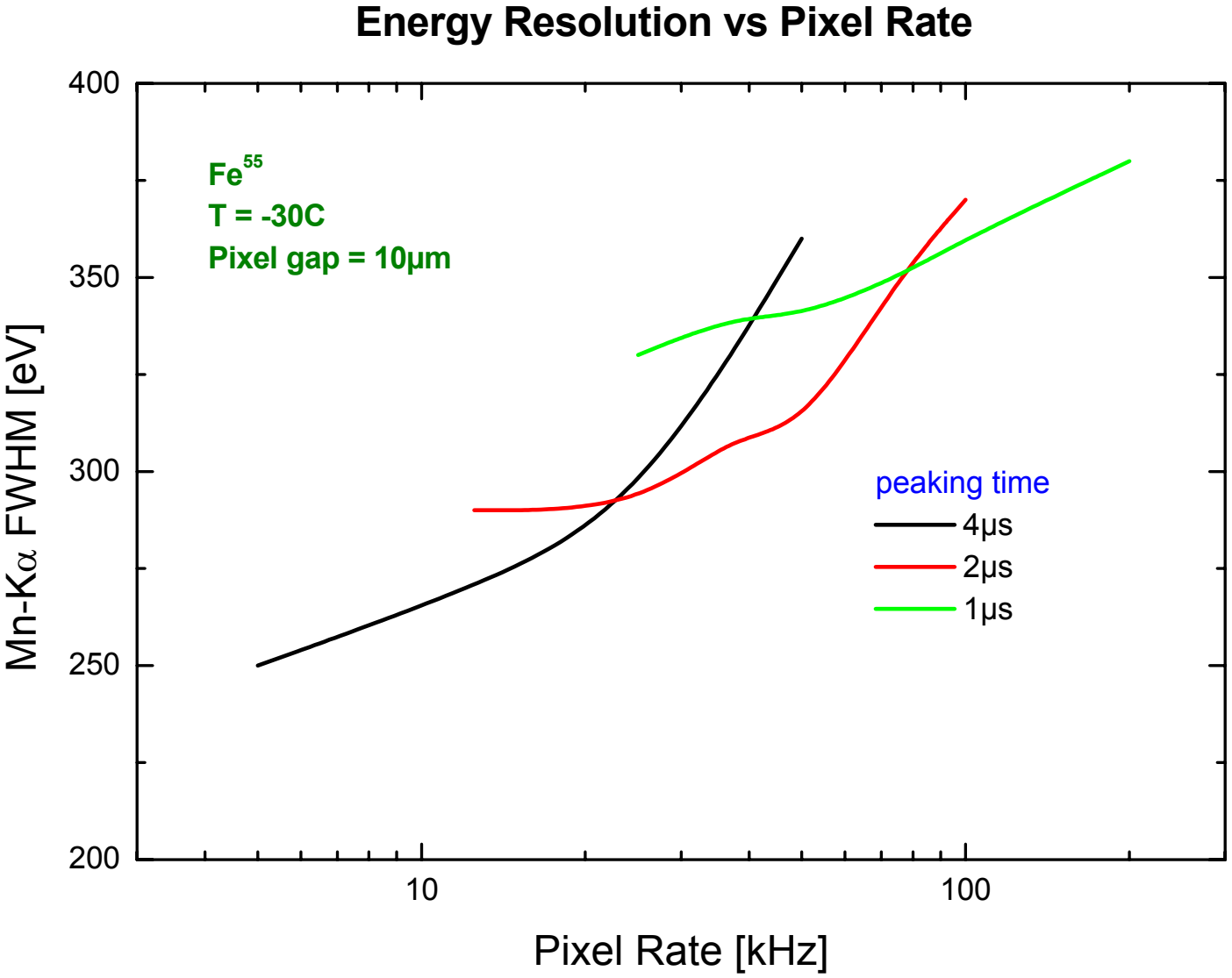


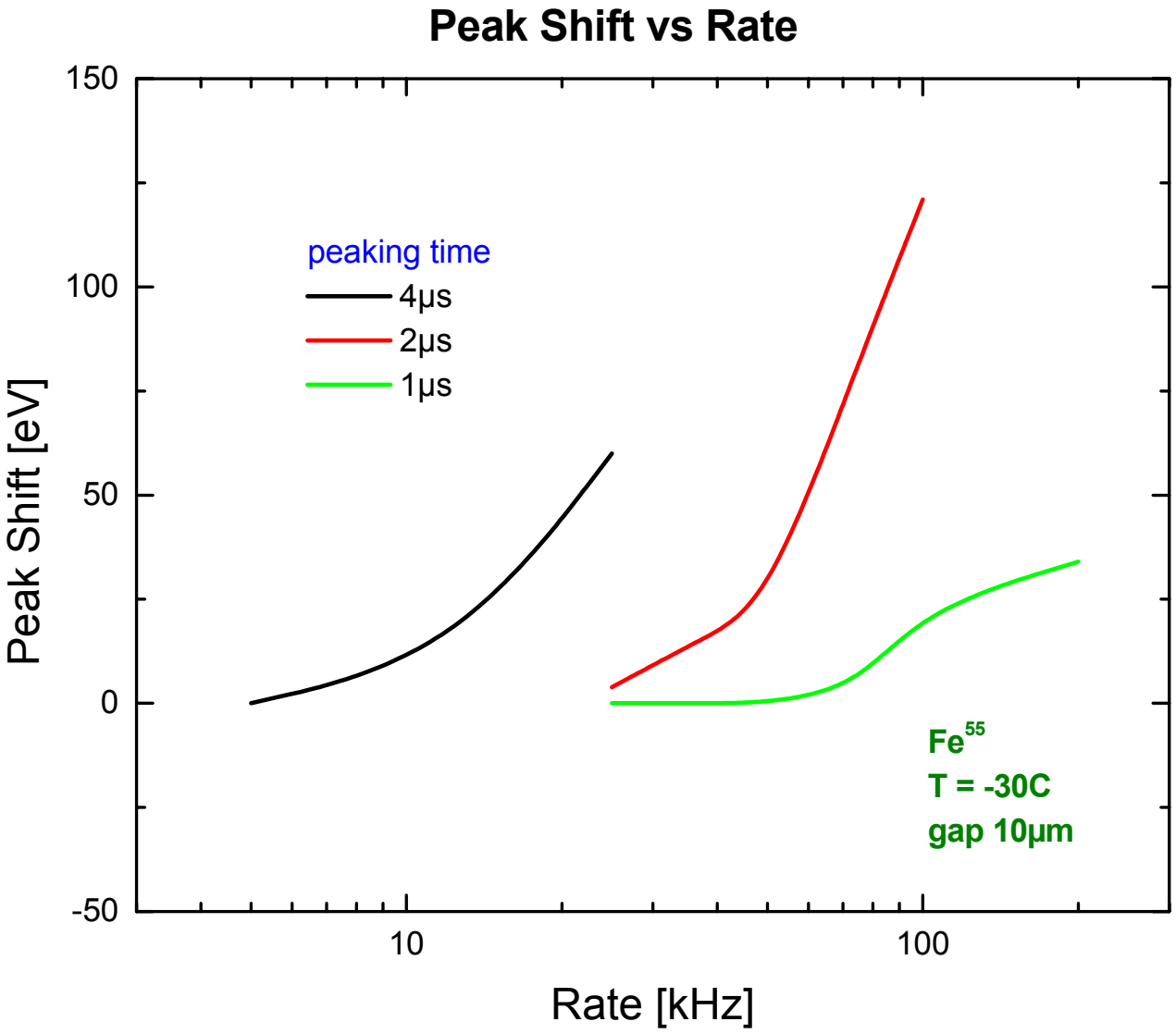
Spectral Quality vs Pixel Gap



Energy Resolution vs Mixed Signal




Energy Resolution vs Pixel Rate
Fe55
T = -30C
Pixel gap = 10µm
peaking time
4µs
2µs
1µs
Mn-Kα FWHM [eV]
400
350
300
250
200
10
100
Pixel Rate [kHz]

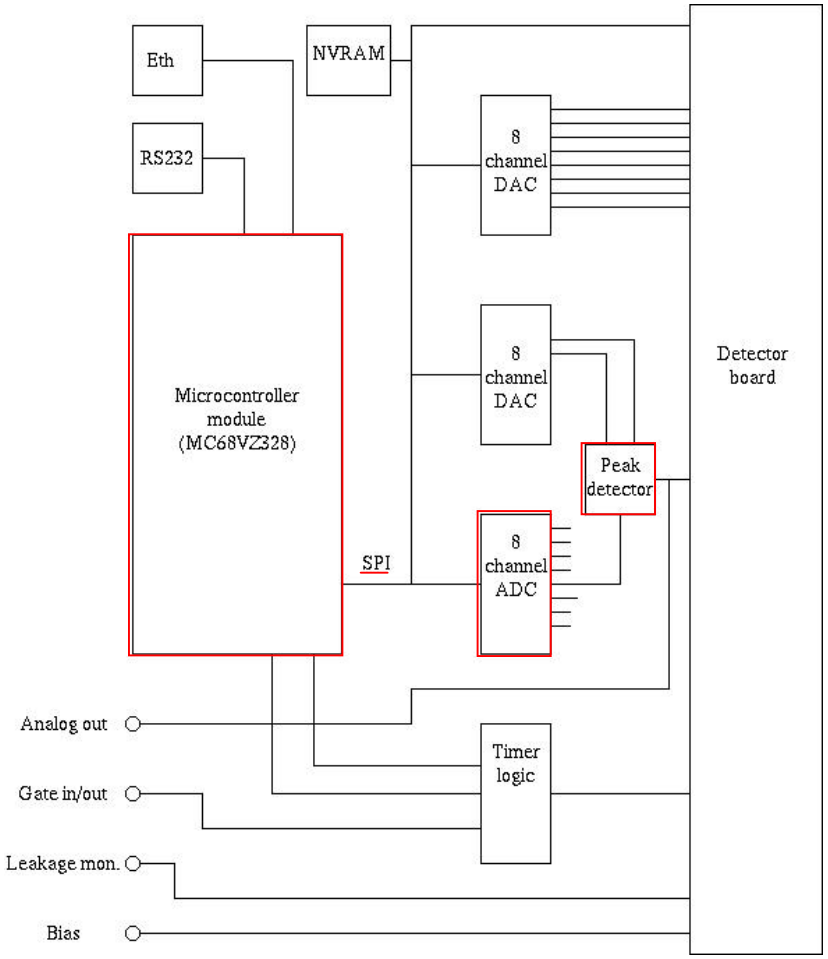

Peak Shift vs Rate
150
100
50
0
-50
Peak Shift [eV]
10
100
Rate [kHz]
peaking time
4µs
2µs
1µs
Fe55
T = -30C
gap 10µm

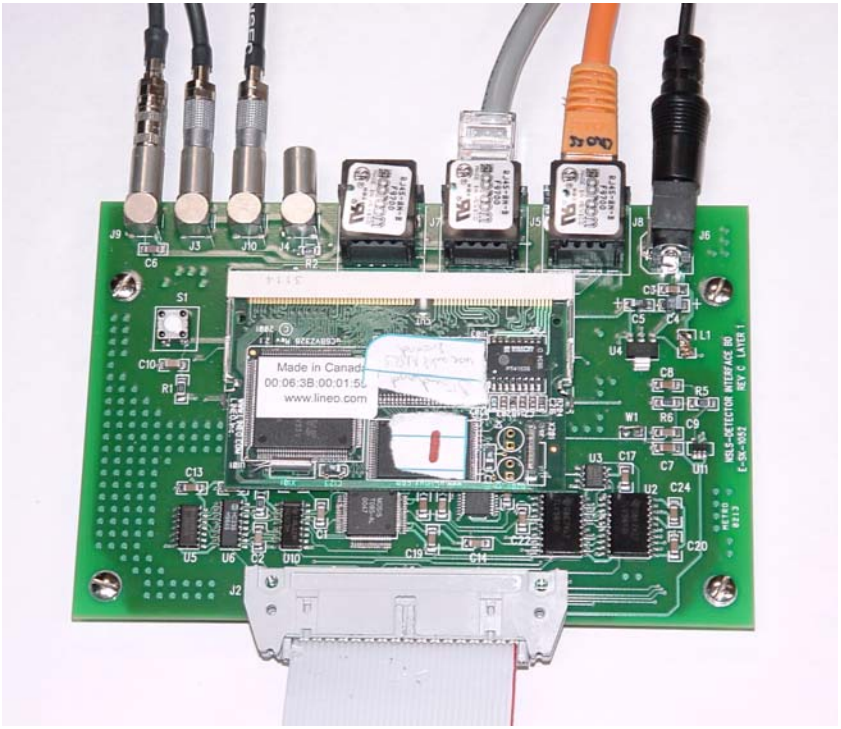
ASIC overview

Technology	CMOS 0.35µm 3.3V 2P4M
Size	≈ 3.6 × 6.3 mm^2
# MOSFETs	≈ 180,000
# Channels	32
power / channel	≈ 8 mW
# Discriminators	three / channel (1 thr., 2 win.)
threshold adjustment	four 6-bit DACs (1.6mV step)
threshold dispersion (adj)	≈ 2.5 electrons rms
# Counters	three / channel
bits per counter	24
Gain (settable)	750, 1500 mV/fC
Peaking time (settable)	0.5, 1, 2, 4 µs
ENC @ 1µs	≈ 14 + 12/pF electrons rms
ENC @ 4µs	≈ 11 + 6/pF electrons rms

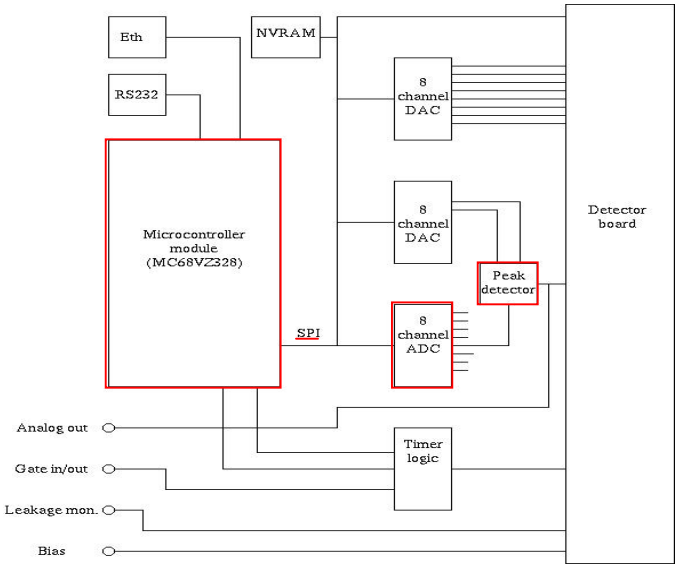
- self adaptive continuous reset
- high order shaper
- band-gap referenced output baseline
- output baseline stabilizer (BLH)
- test capacitors
- analog and pixel leakage monitors
- plug & play (fully self biasing)
- serial interface
    - counters readout
    - gain / peaking-time setting
    - monitors & test enable
    - channel masking
    - DACs setting
- token or chip-select mode

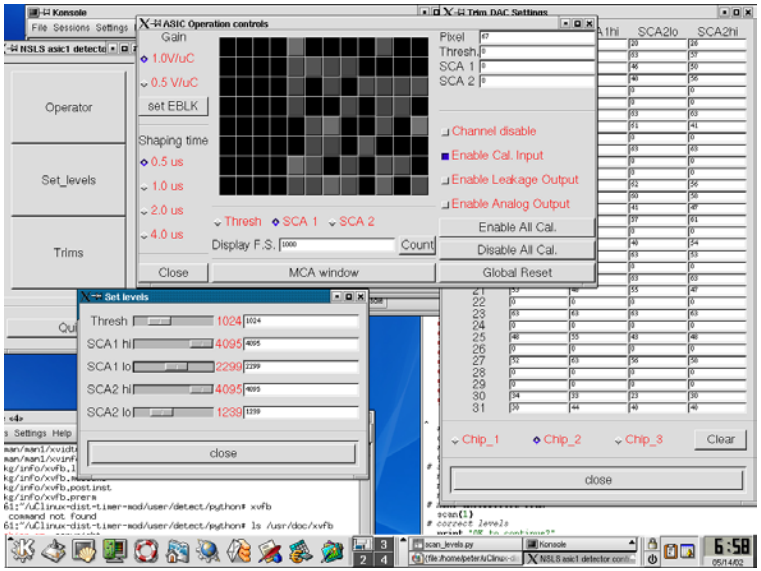
Readout

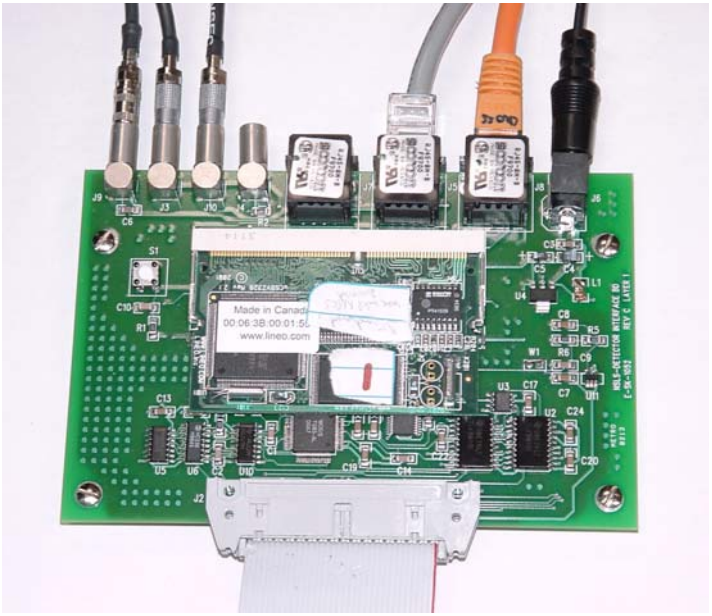

Eth
NVRAM
RS232
8 channel DAC
8 channel DAC
Microcontroller module (MC68VZ328)
Peak detector
Detector board
SPI
8 channel ADC
Analog out
Timer logic
Gate in/out
Leakage mon.
Bias

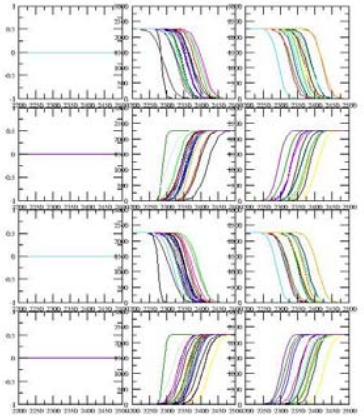


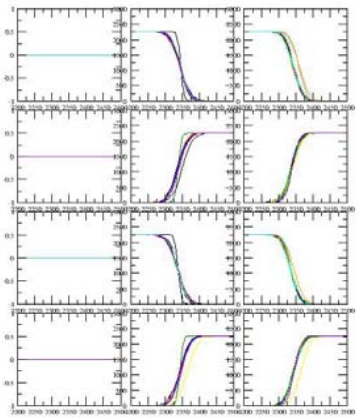
Readout Interface







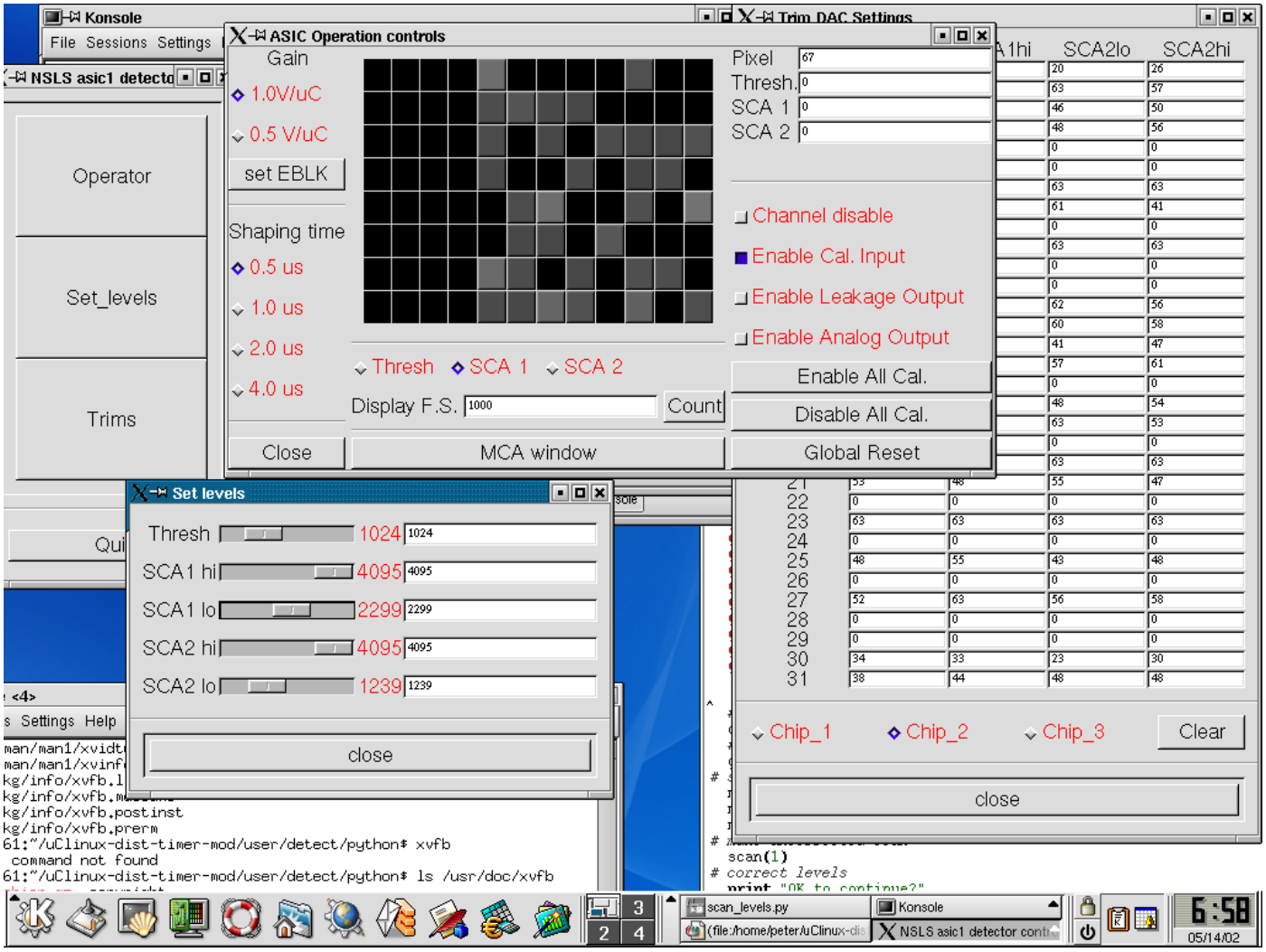




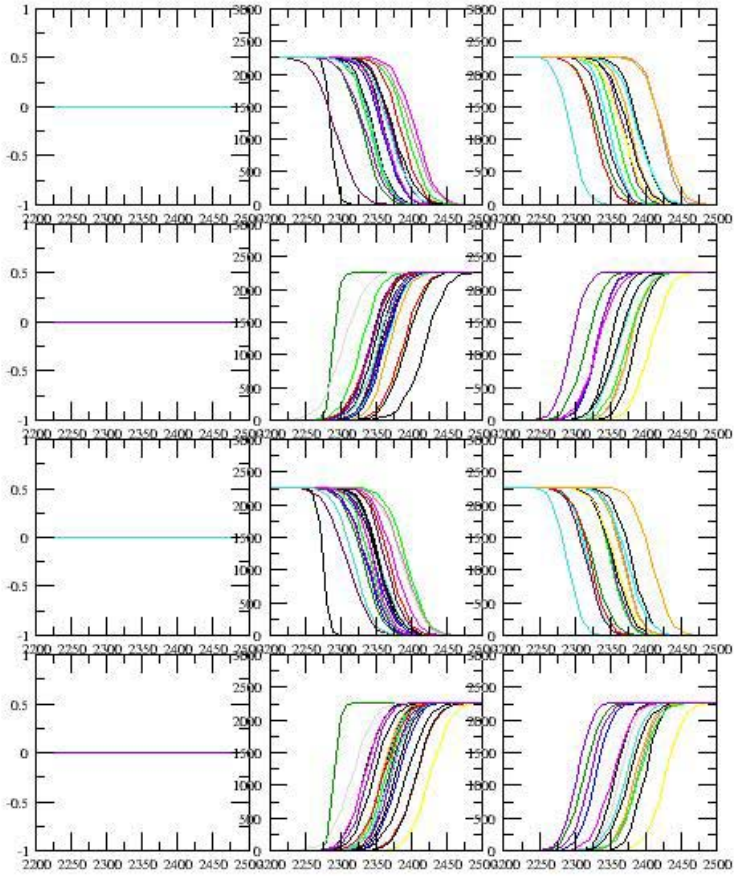
before correction $\sigma \approx$ 170e⁻ rms

after correction $\sigma \approx$ 2.5e⁻ rms

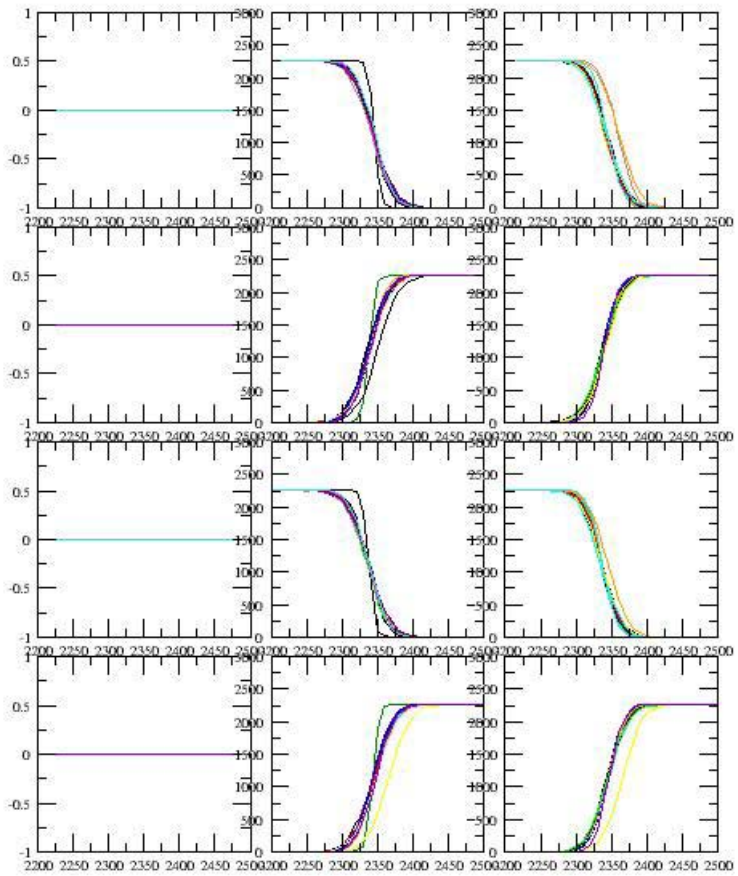
Readout interface



Automatic threshold equalization

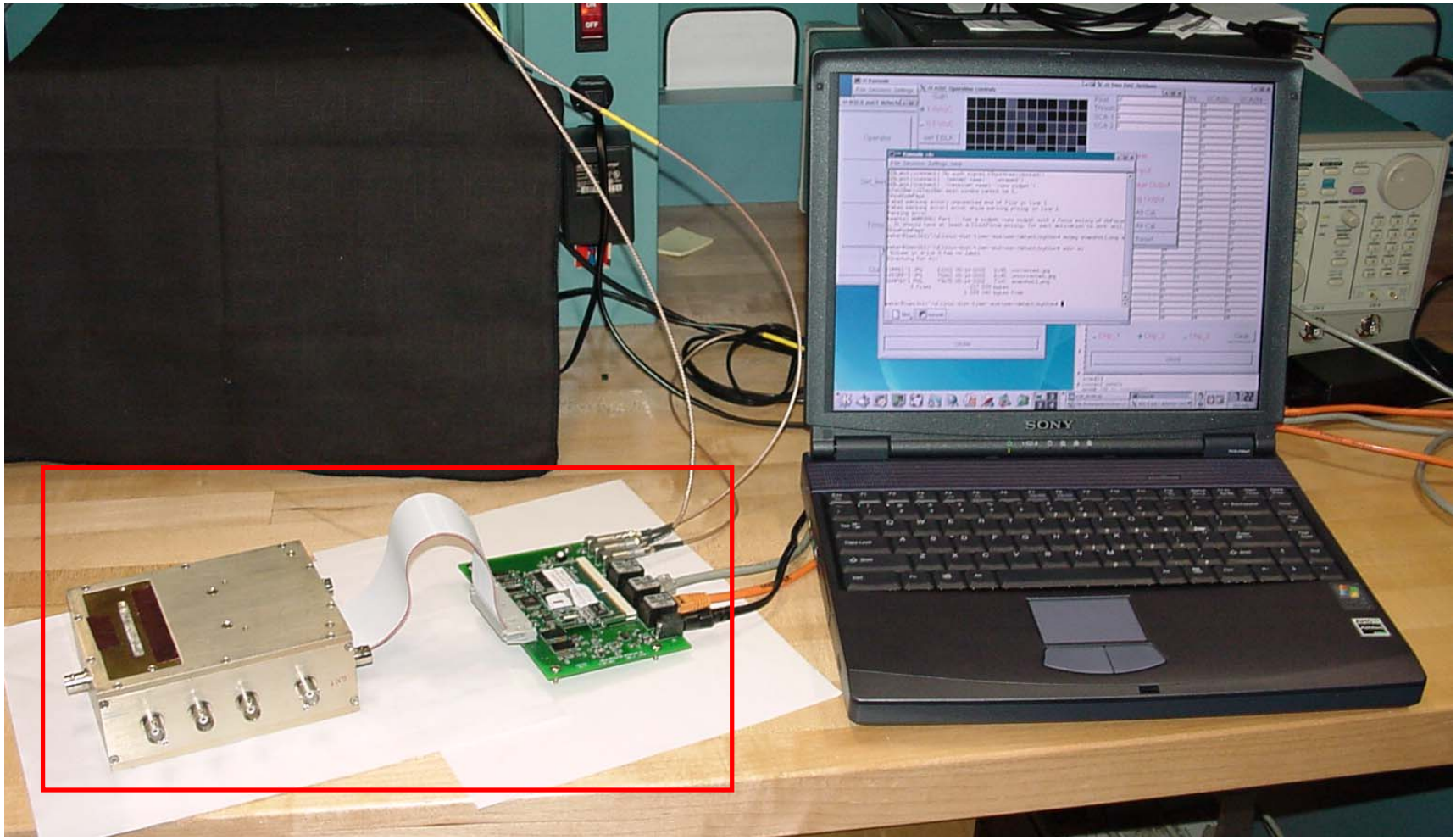


before correction $\sigma \approx 170e^-$ *rms*



after correction $\sigma \approx 2.5e^-$ *rms*

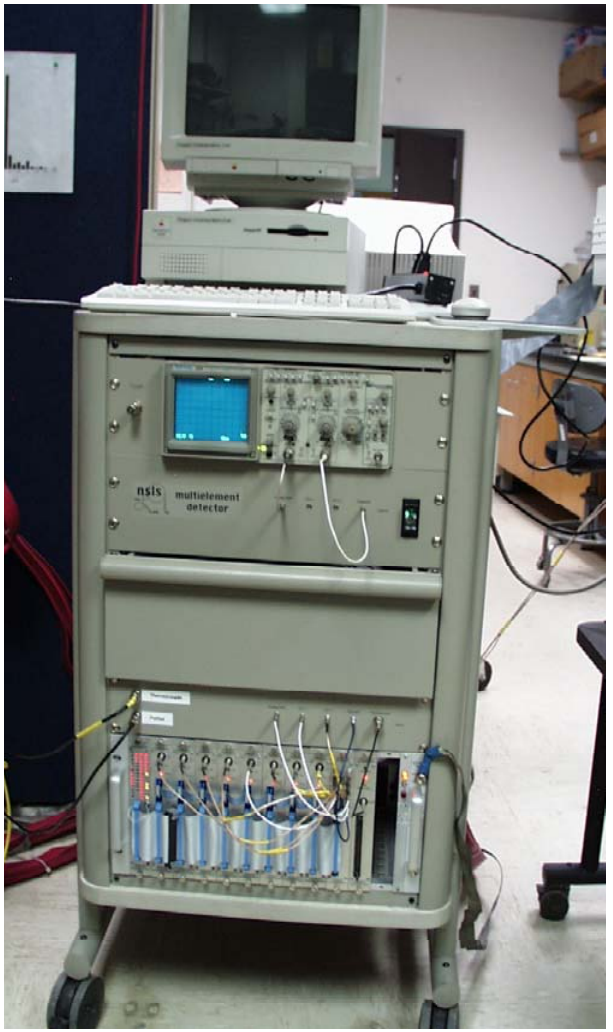
New EXAFS detector



≈ 400 channels, < 300 eV, > 10MHz

Current EXAFS detector

head - preamplifiers



rack – shapers …

≈ 100 channels, > 350 eV, < 1 MHz

Summary

New detector for EXAFS

- monolithic Si sensor, 384-mm^2 active area
- 384 1mm^2 pixels
- 32-channel ASICs

First results (single quadrant)

- ENC ≈ 11 + 6/pF e^- rms @ 4μs
- FWHM < 300eV @ rate < 100 kHz/pixel
- threshold dispersion < 2.5 e^- rms
- 50μm gap preferred

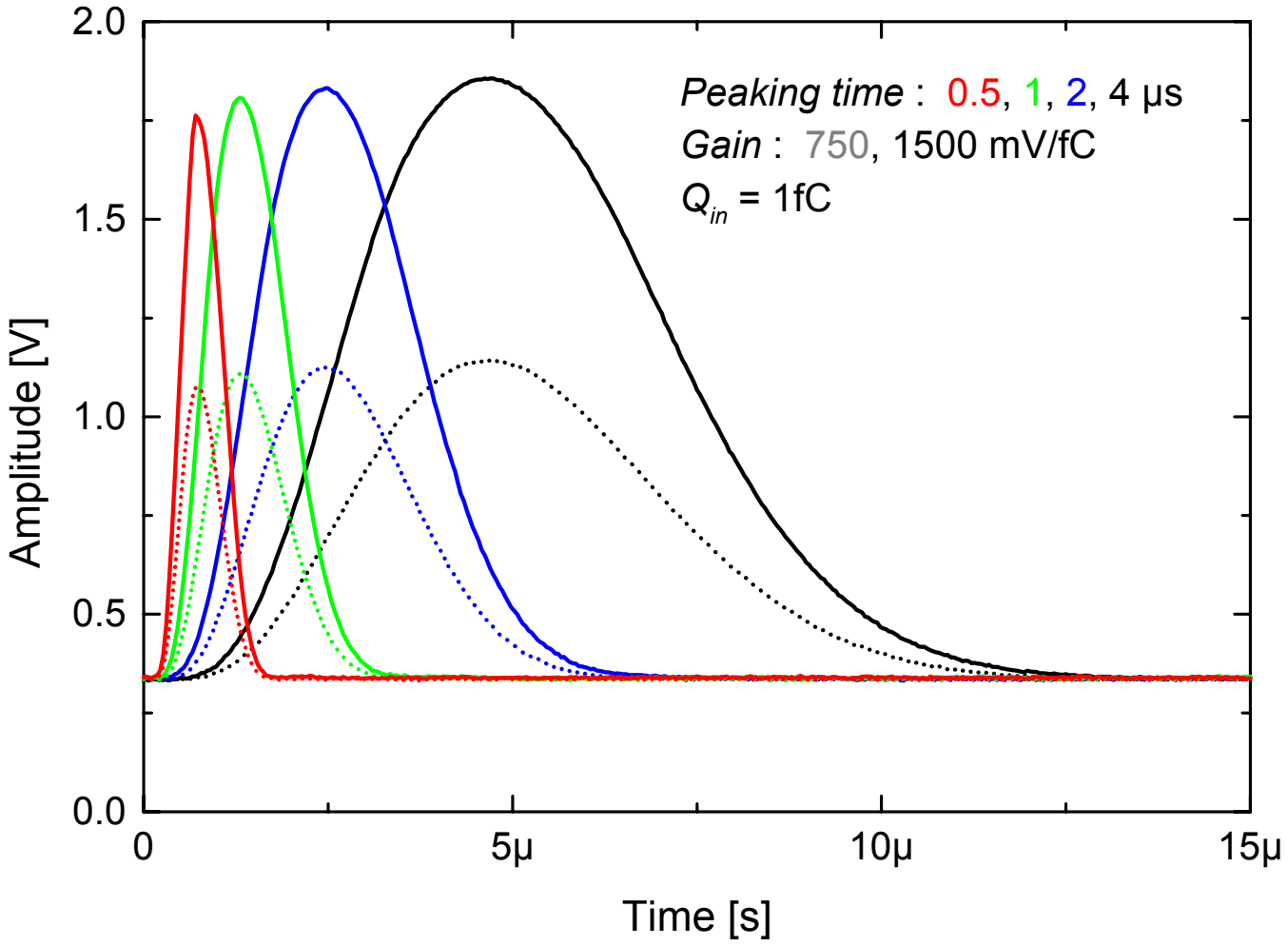
Future work

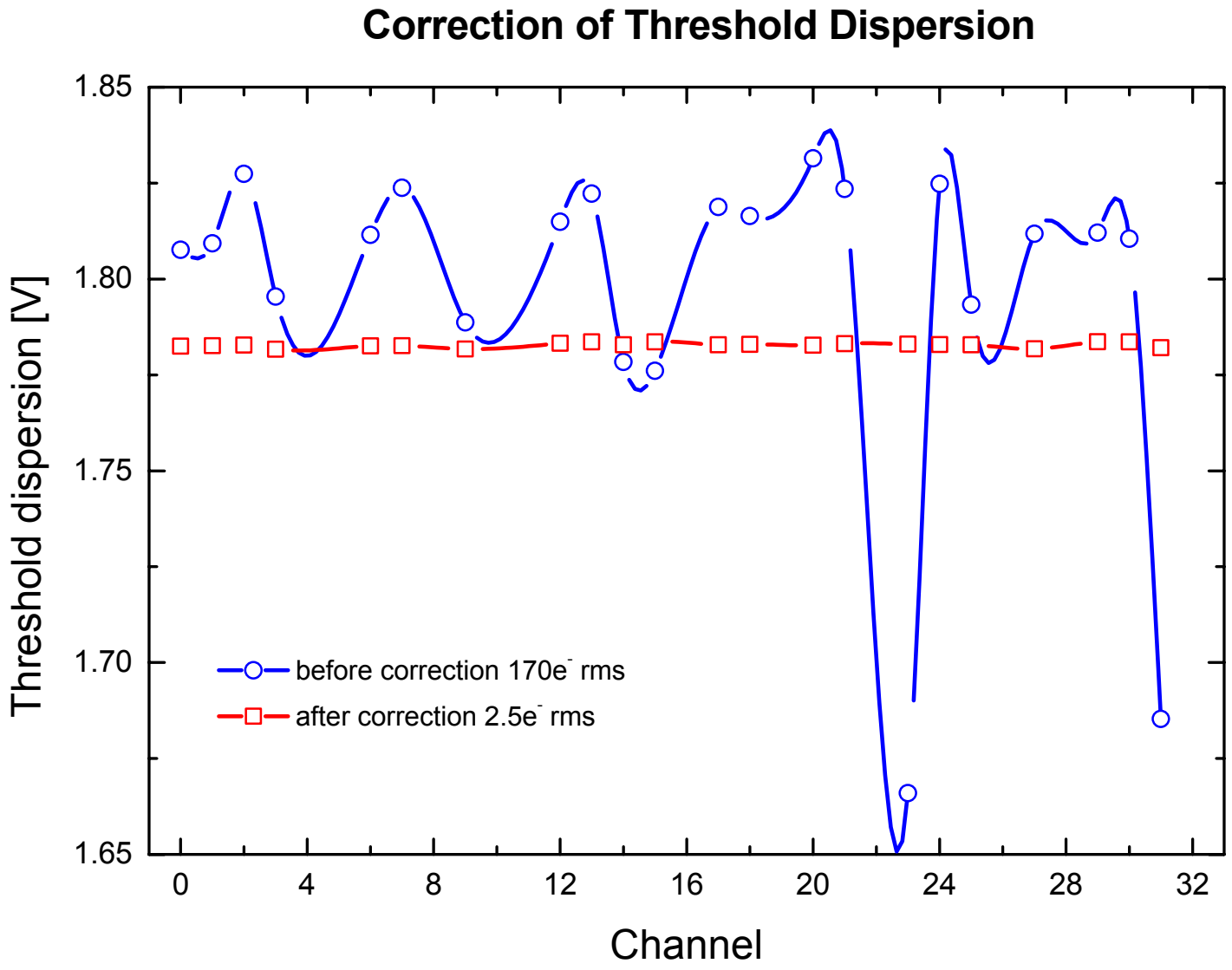
- one ASIC iteration
- four quadrant (12 ASICs) assembly / test
- on-field test at NSLS (BNL)

Acknowledgment

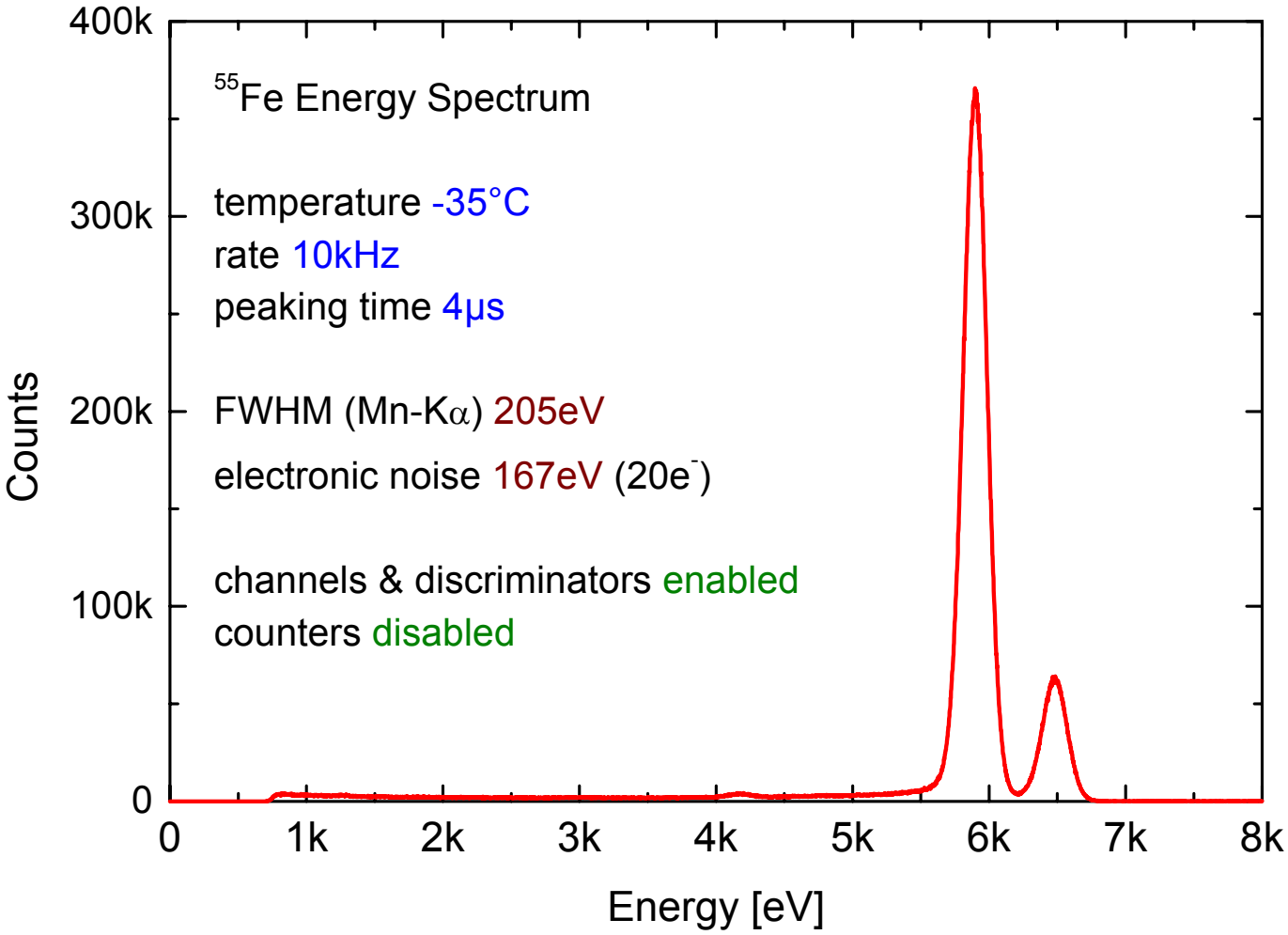
A. Kandasamy, V. Radeka, P. Rehak, G. C. Smith
D. Pinelli, J. Triolo

Settable gain and peaking time

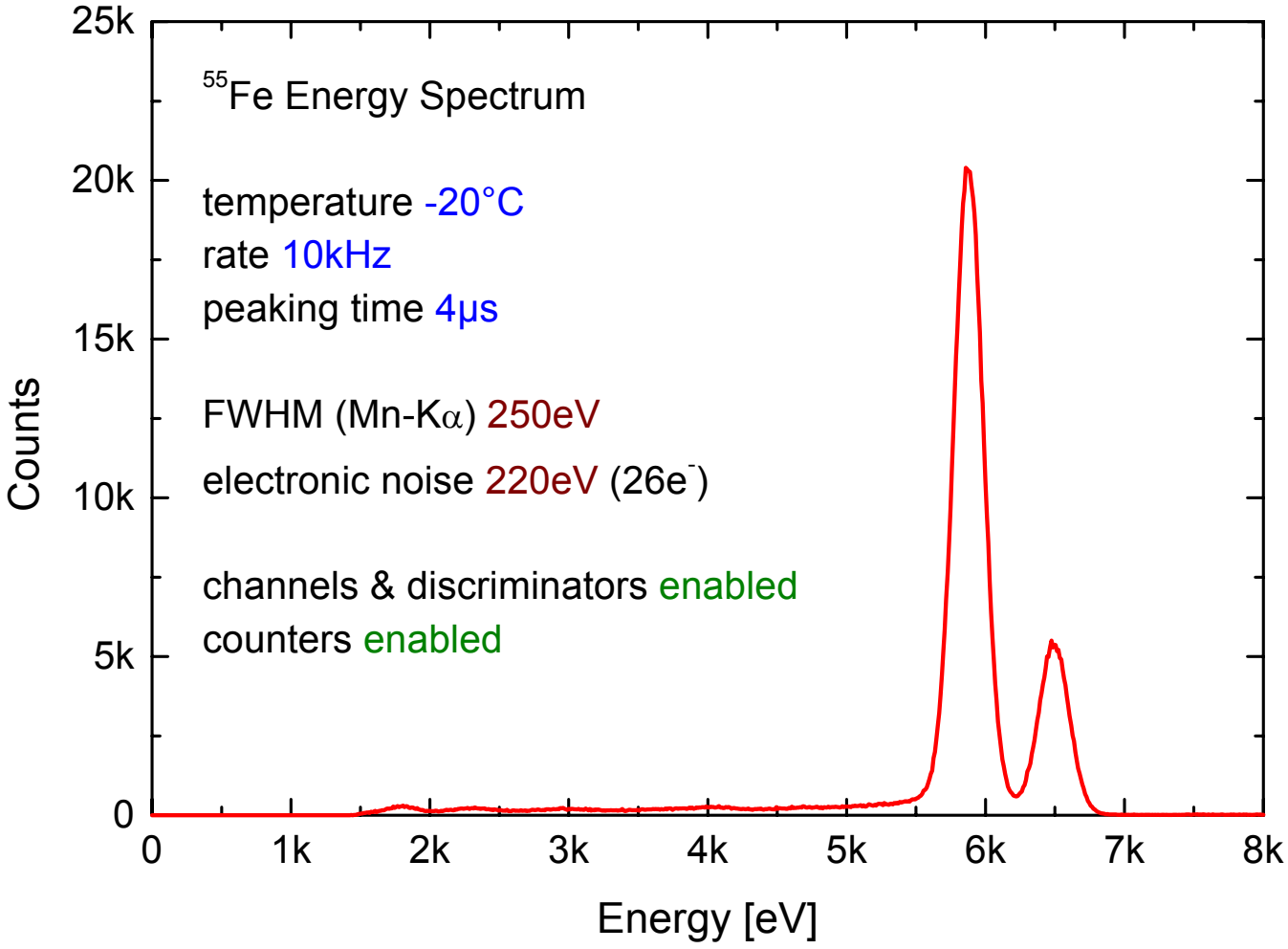



Correction of Threshold Dispersion
Threshold dispersion [V]
1.85
1.80
1.75
1.70
1.65
0
4
8
12
16
20
24
28
32
Channel
before correction 170e- rms
after correction 2.5e- rms

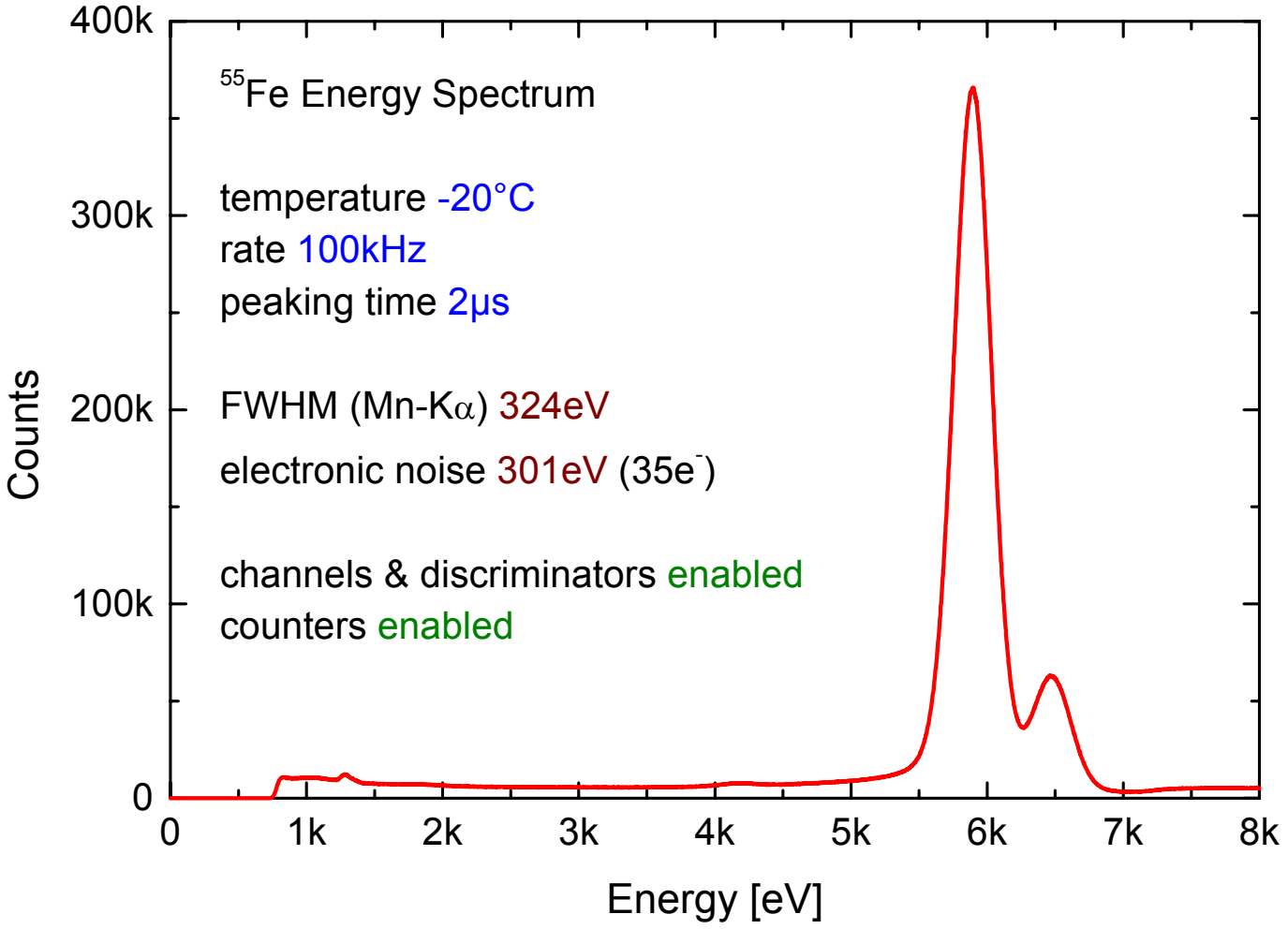
^{55}Fe spectrum



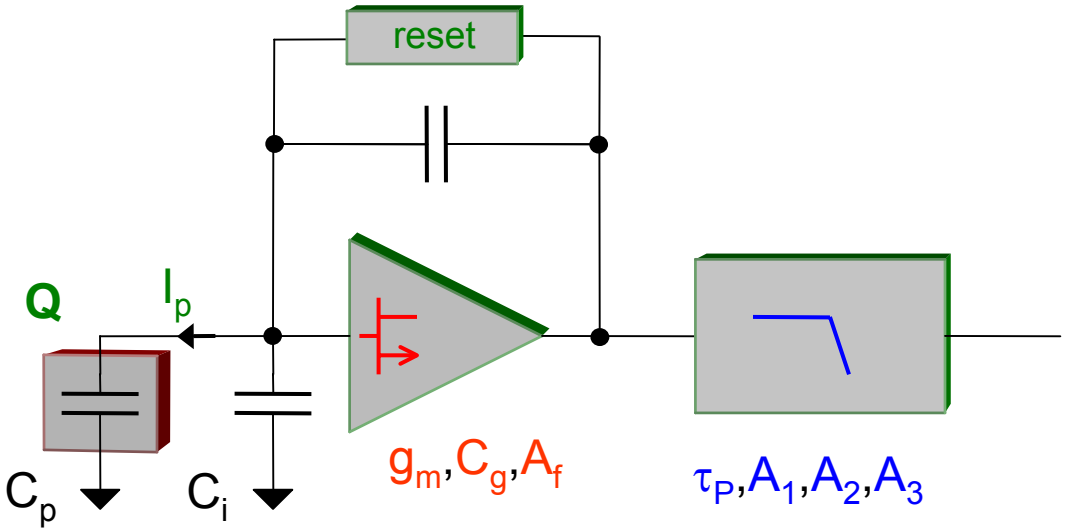
^{55}Fe spectrum

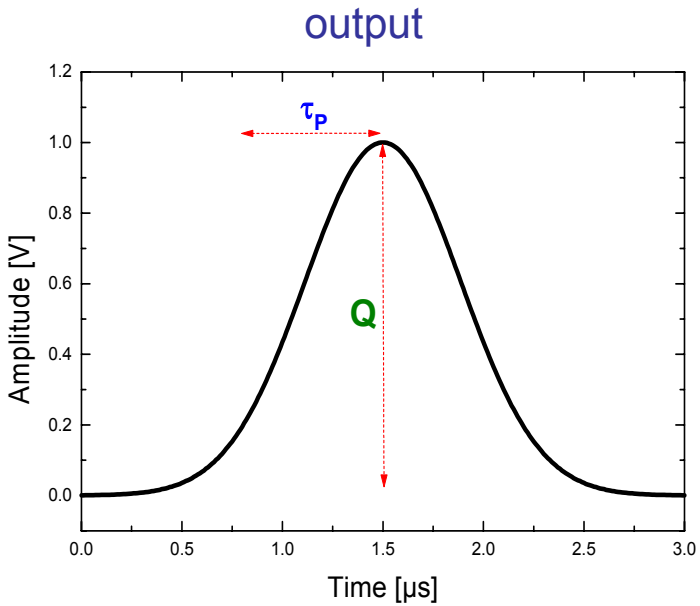


^{55}Fe spectrum



Input MOSFET optimization

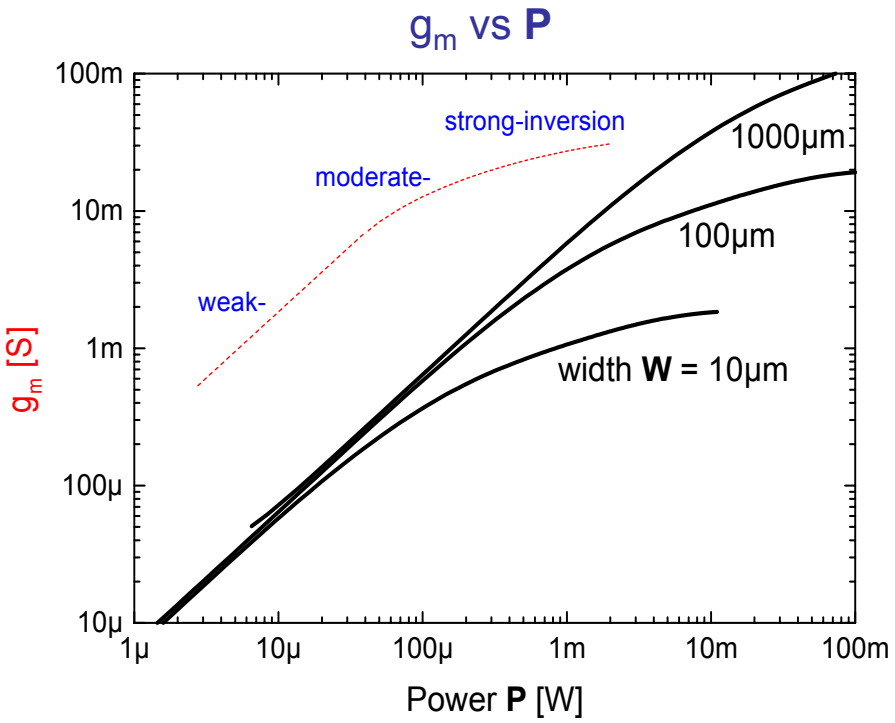


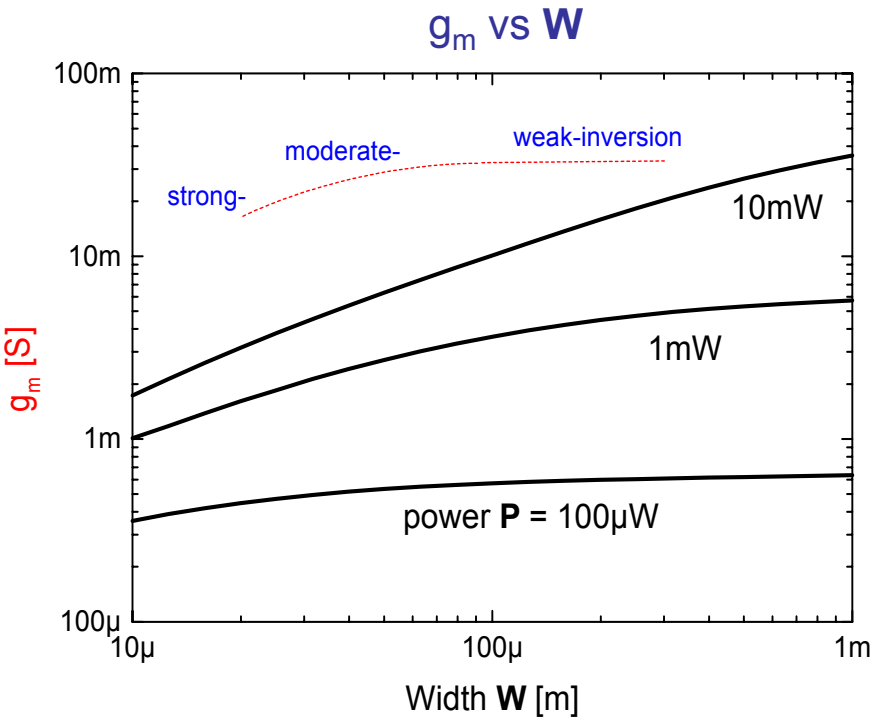


$$ENC^2 = \frac{A_1}{\tau_P}\frac{\left(C_p + C_i + C_g\right)^2}{g_m} + A_2 A_f \left(C_p + C_i + C_g\right)^2 + A_3 \tau_P \left(I_p + I_{rst}\right)$$

g_m, C_g, A_f, are functions of input MOSFET width **W** and power **P**

Input MOSFET optimization

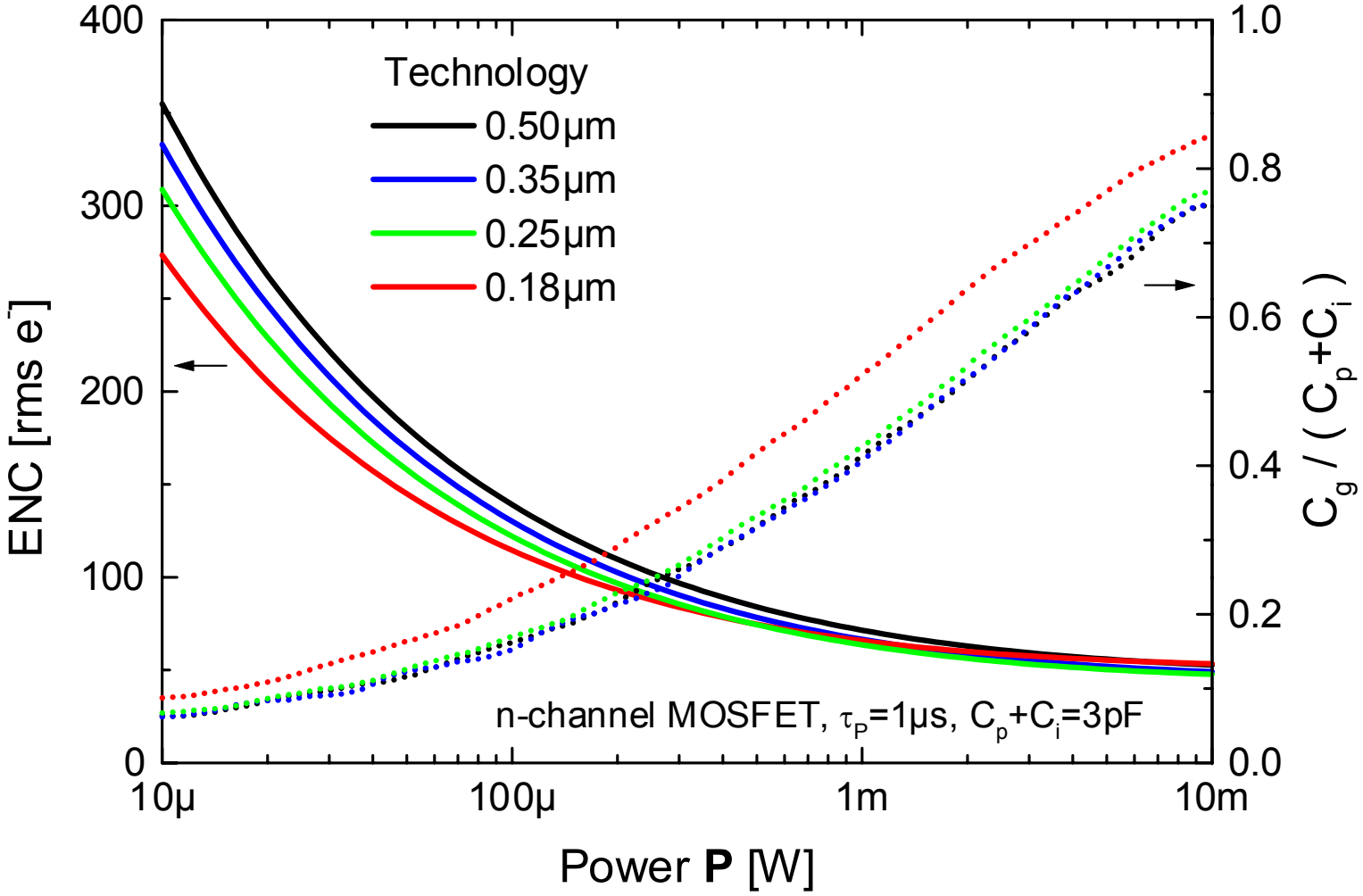




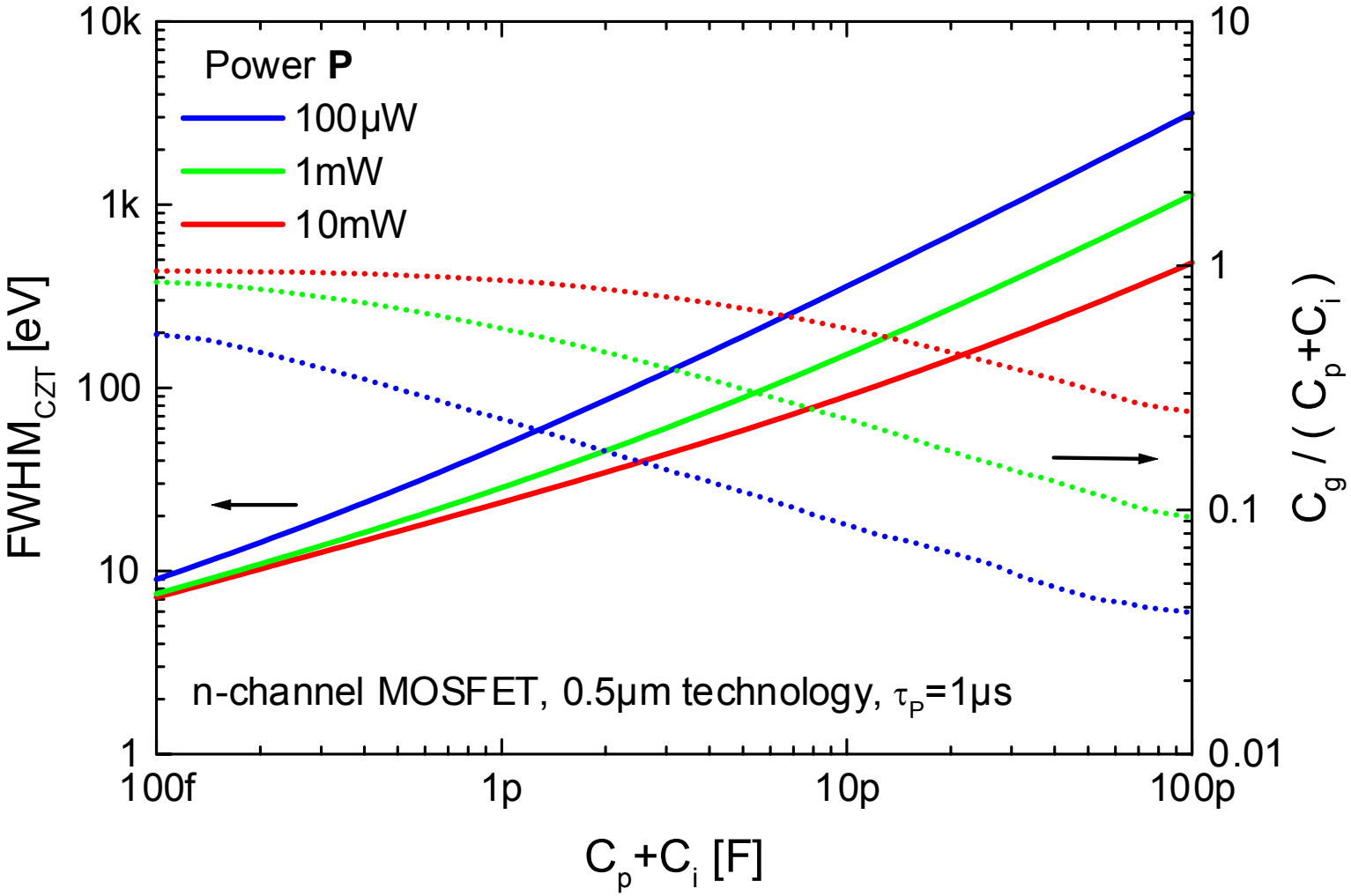
$$C_g \approx (C_{ox}L + C_{ov}) \cdot \mathbf{W}$$

$$A_f \approx K_f / (C_{ox}L \cdot \mathbf{W})$$

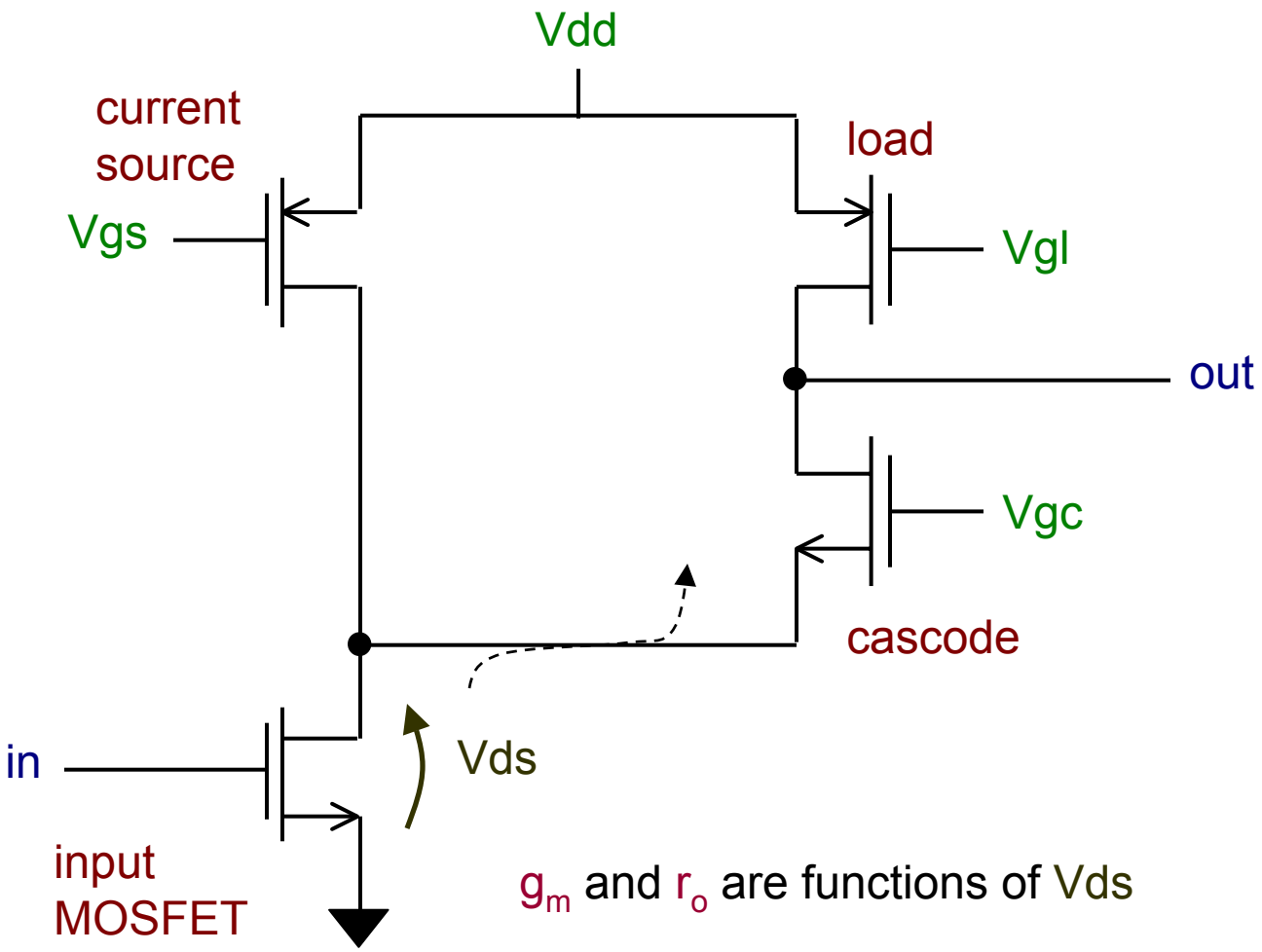
Input MOSFET optimization



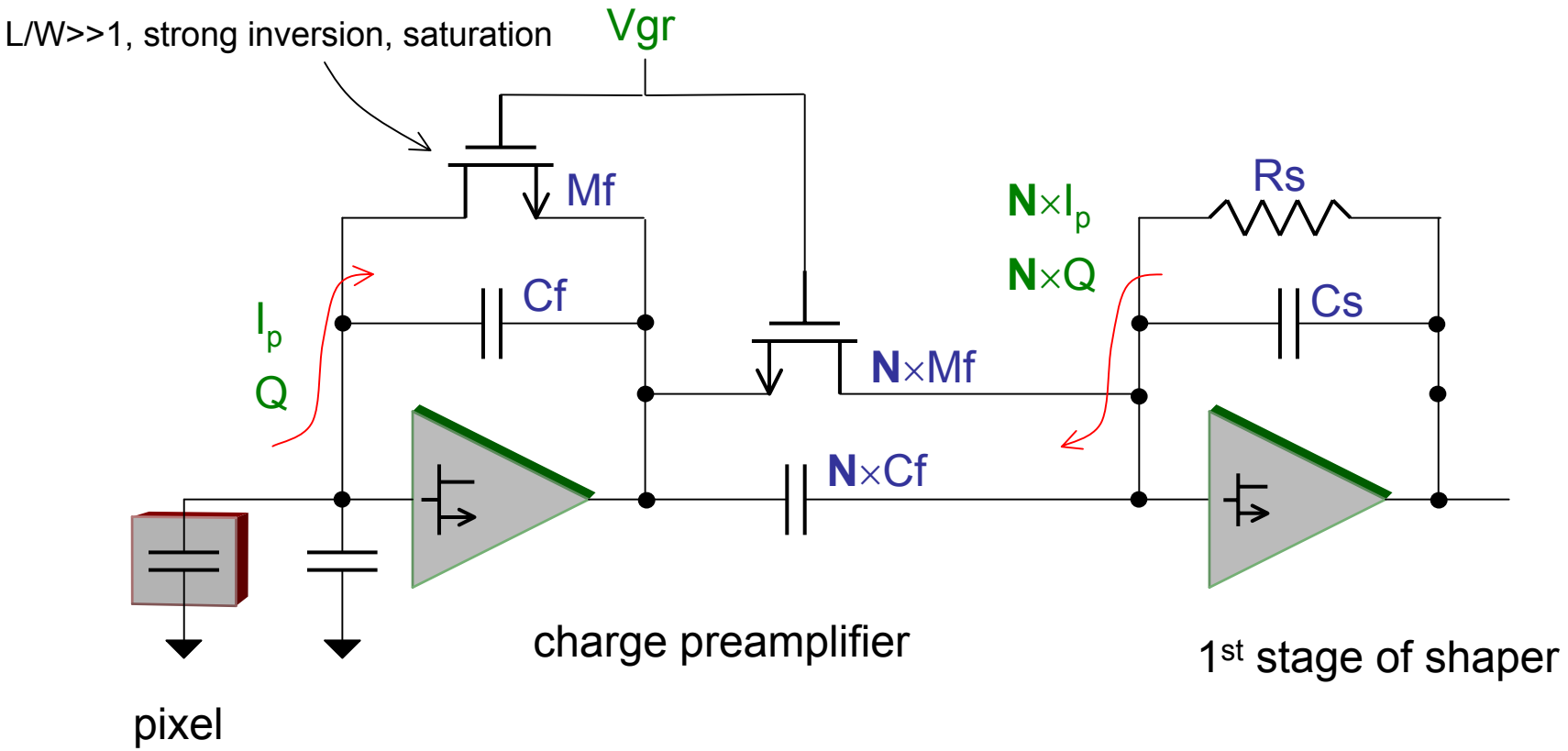
Input MOSFET optimization



Input MOSFET optimization



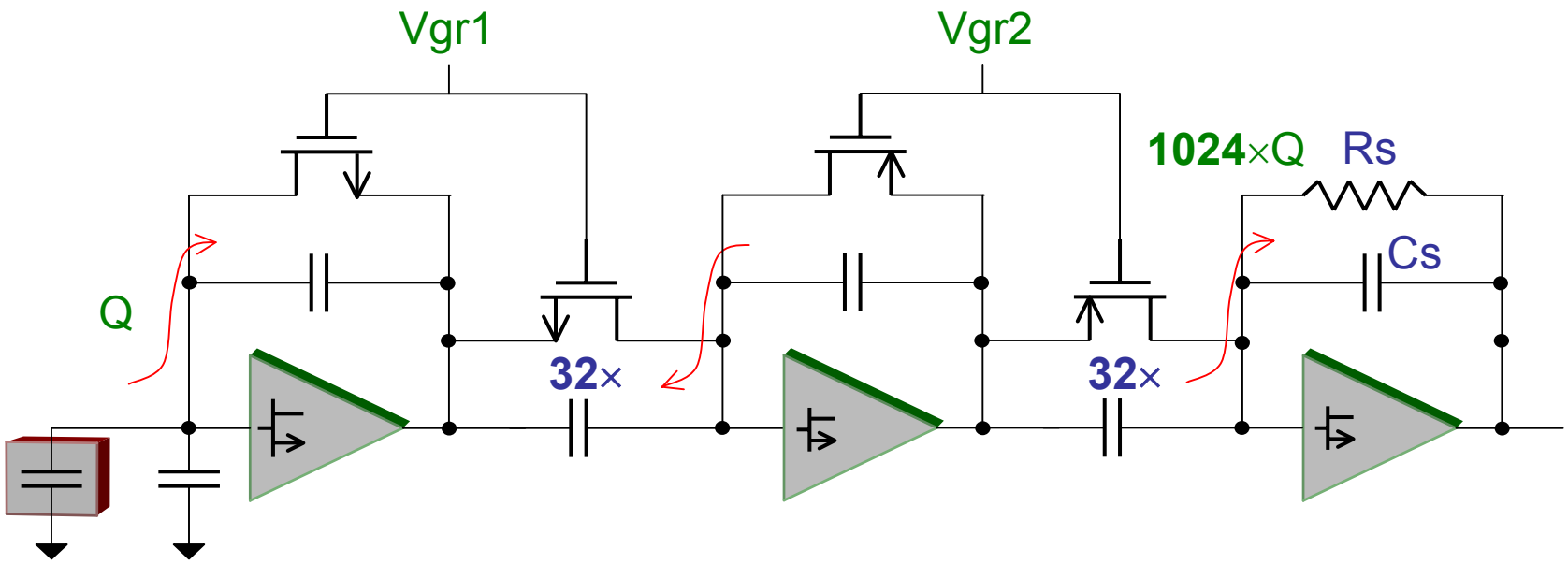
Continuous reset



- current gain equal to **N**
- fully linear
- **self-adapts** to leakage current
- minimum noise contribution

Continuous reset

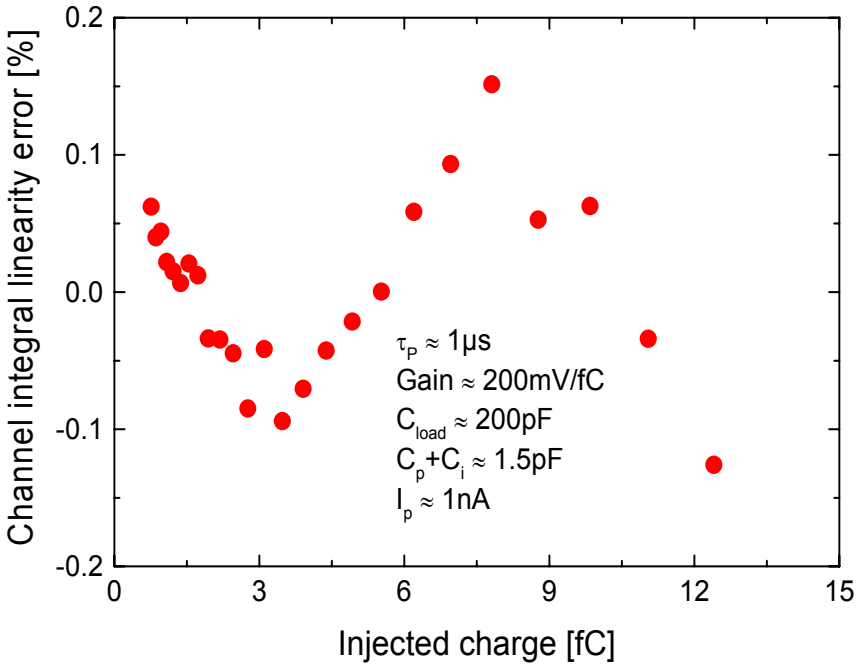
$$\frac{2kT}{Rs}\frac{1}{N^2} \equiv q \cdot I_{eq} \qquad Rs \approx 192k\Omega \rightarrow I_{eq} \approx 260pA$$



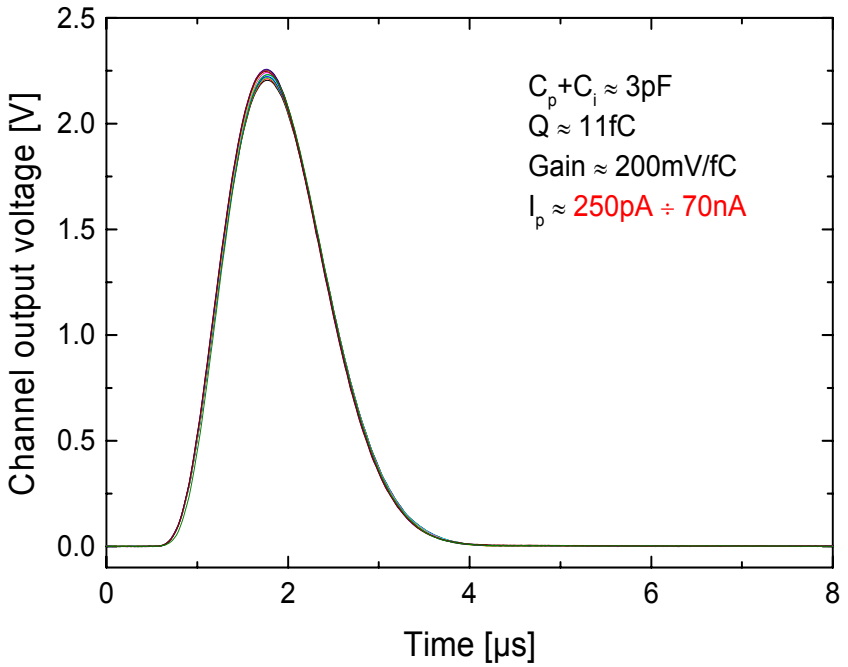
$$Rs \approx 192k\Omega \rightarrow I_{eq} \approx 260fA$$

Continuous reset

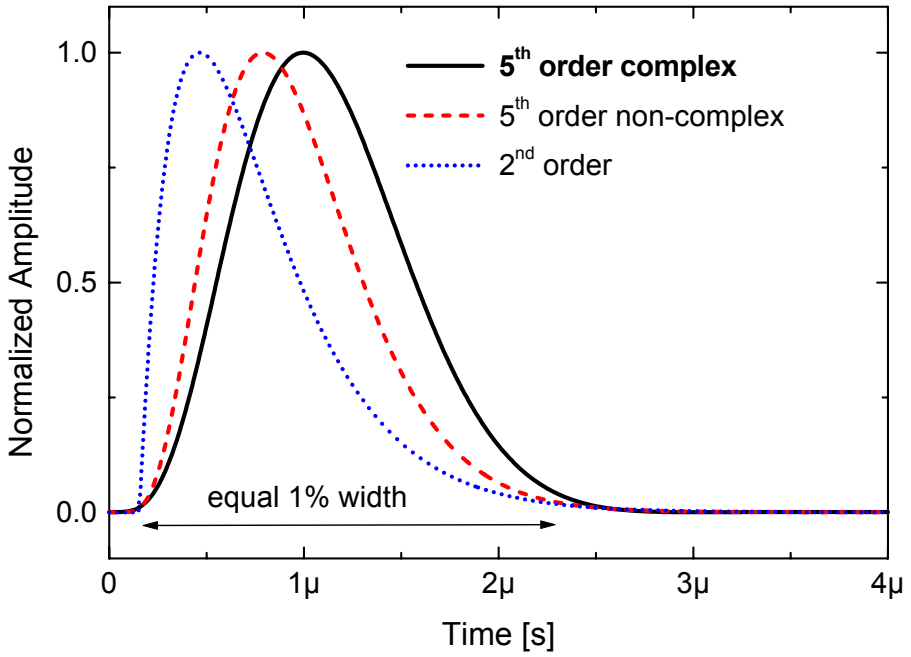
linearity



output vs pixel leakage current



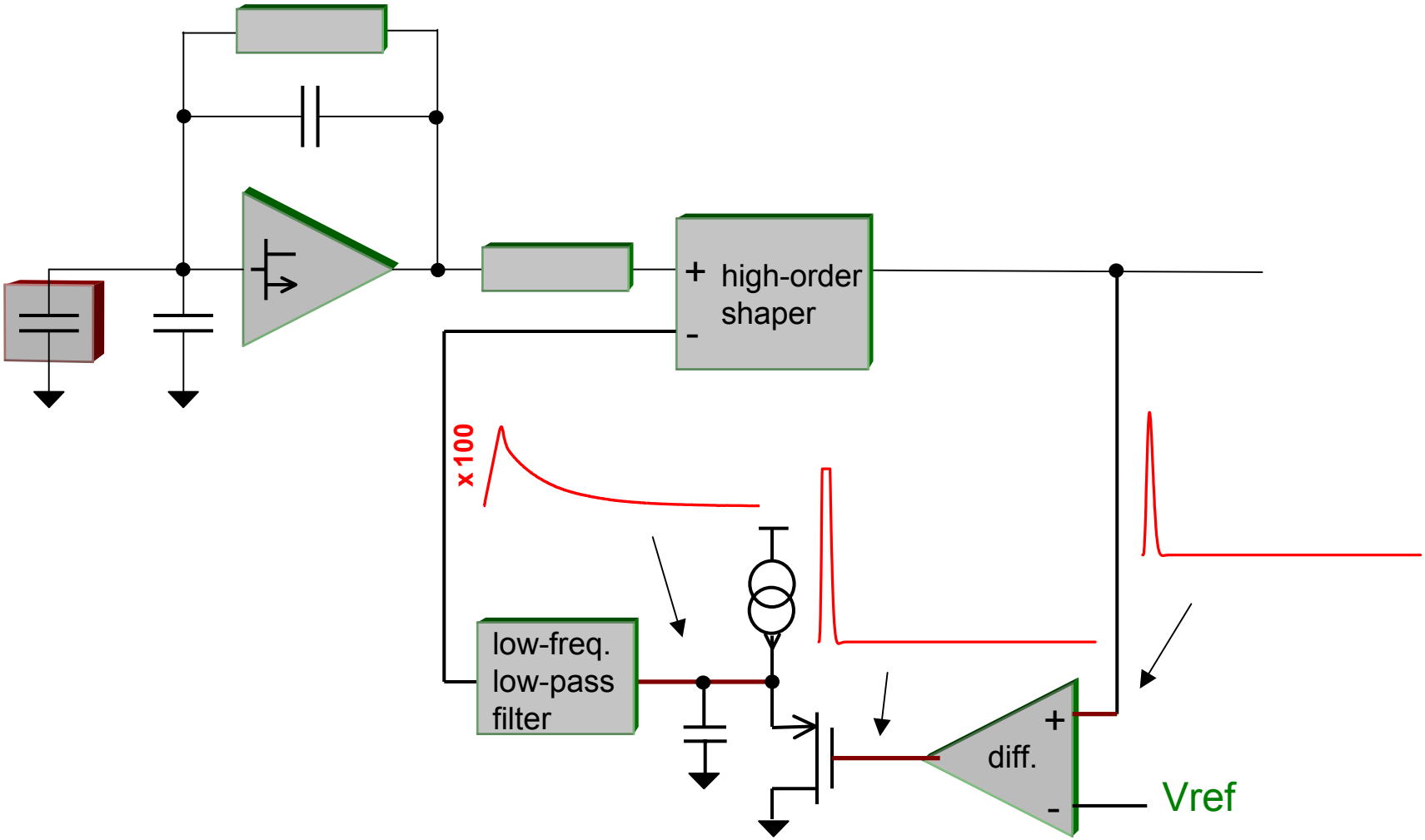
High order shaping



	A_1/τ_P
5th cpx	**1**
5th	1.24
2nd	2.64

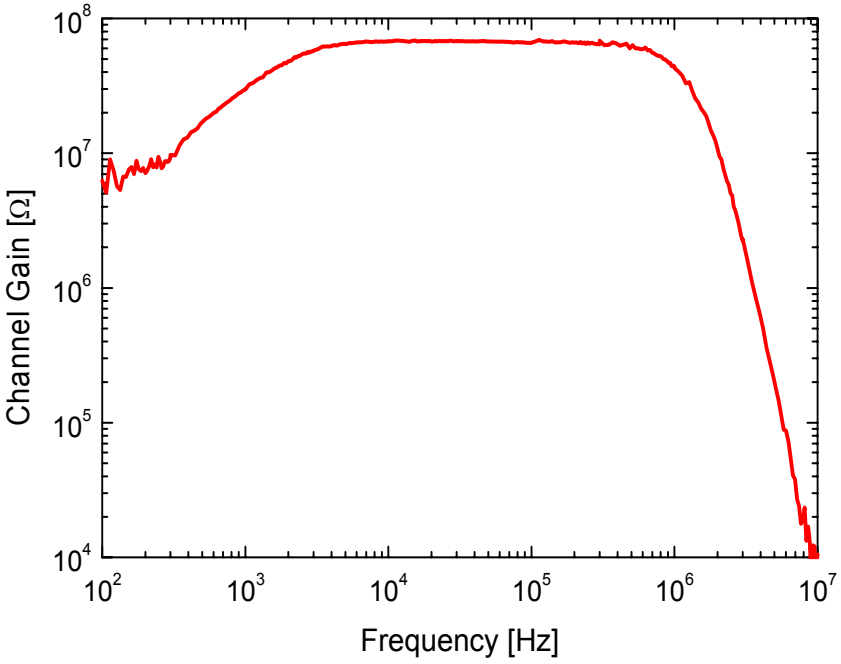
$$ENC^2 = \frac{A_1}{\tau_P} \frac{\left(C_p + C_i + C_g\right)^2}{g_m} + \ldots$$

Output baseline stabilizer

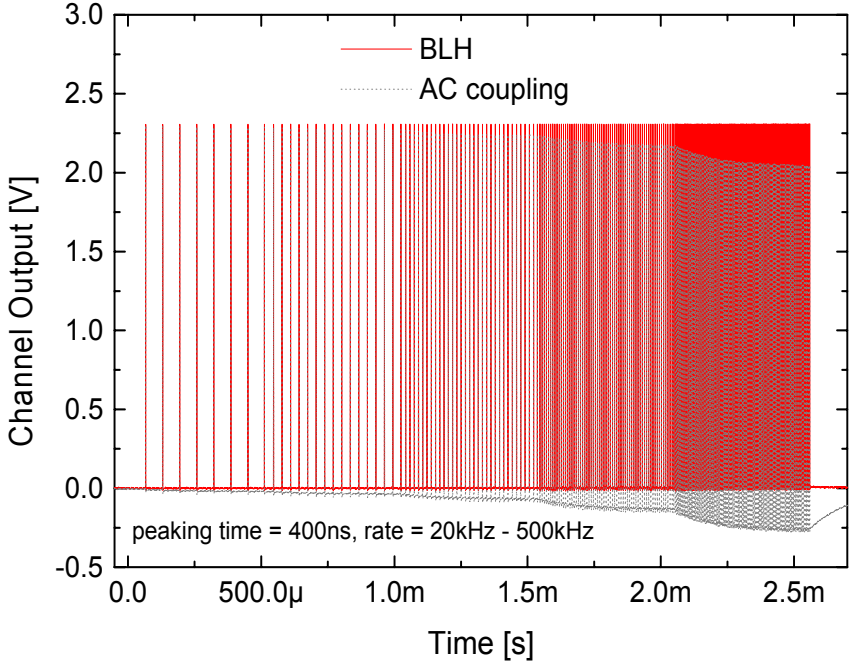


Output baseline stabilizer

transfer function



performance at high rate



Other ASIC features

- plug & play
- per-channel test capacitor
- programmable gain
- programmable peaking time
- high output drive capability
- high stability vs temperature →