BROOKHAVEN
NATIONAL LABORATORY

NSLS Annual Users' Meeting
May 20-22, 2002

The New Detector for EXAFS at NSLS

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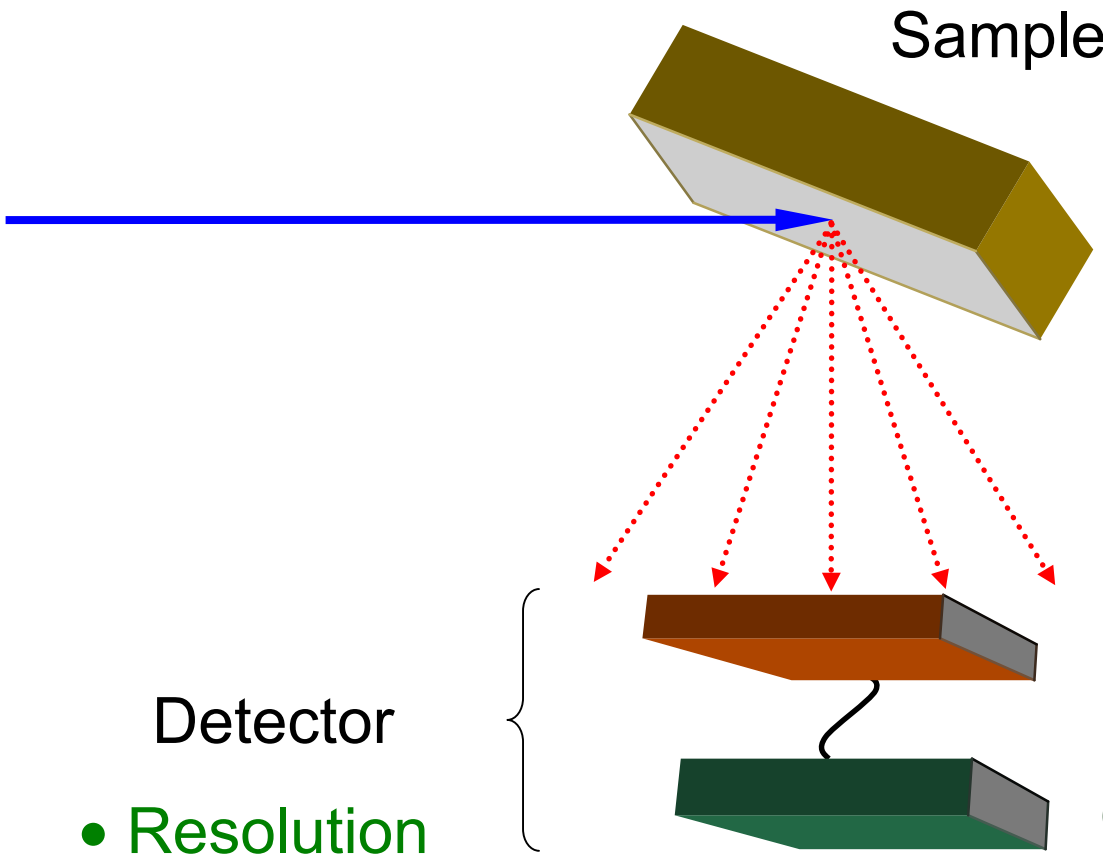
Si sensor, interconnect, front-end & processing electronics, readout electronics, assembly

Outline

- Si sensor
  - segmentation
- Interconnect
- Front-end & processing electronics (ASIC)
  - reset, shaping, stabilization, layout
- Readout electronics
- First experimental results

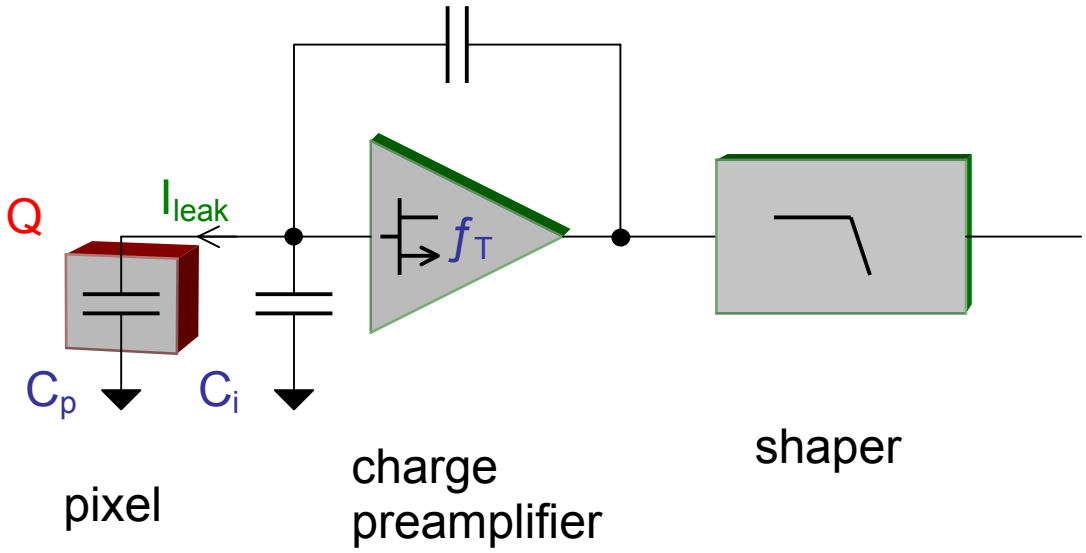
Typical fluorescence EXAFS measurement geometry



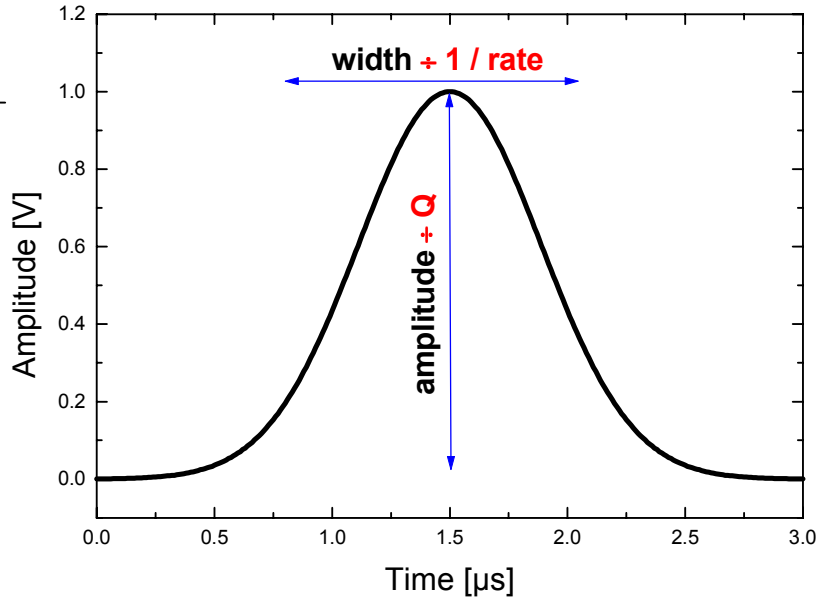
Detector

- Resolution
- Rate

Resolution vs Rate

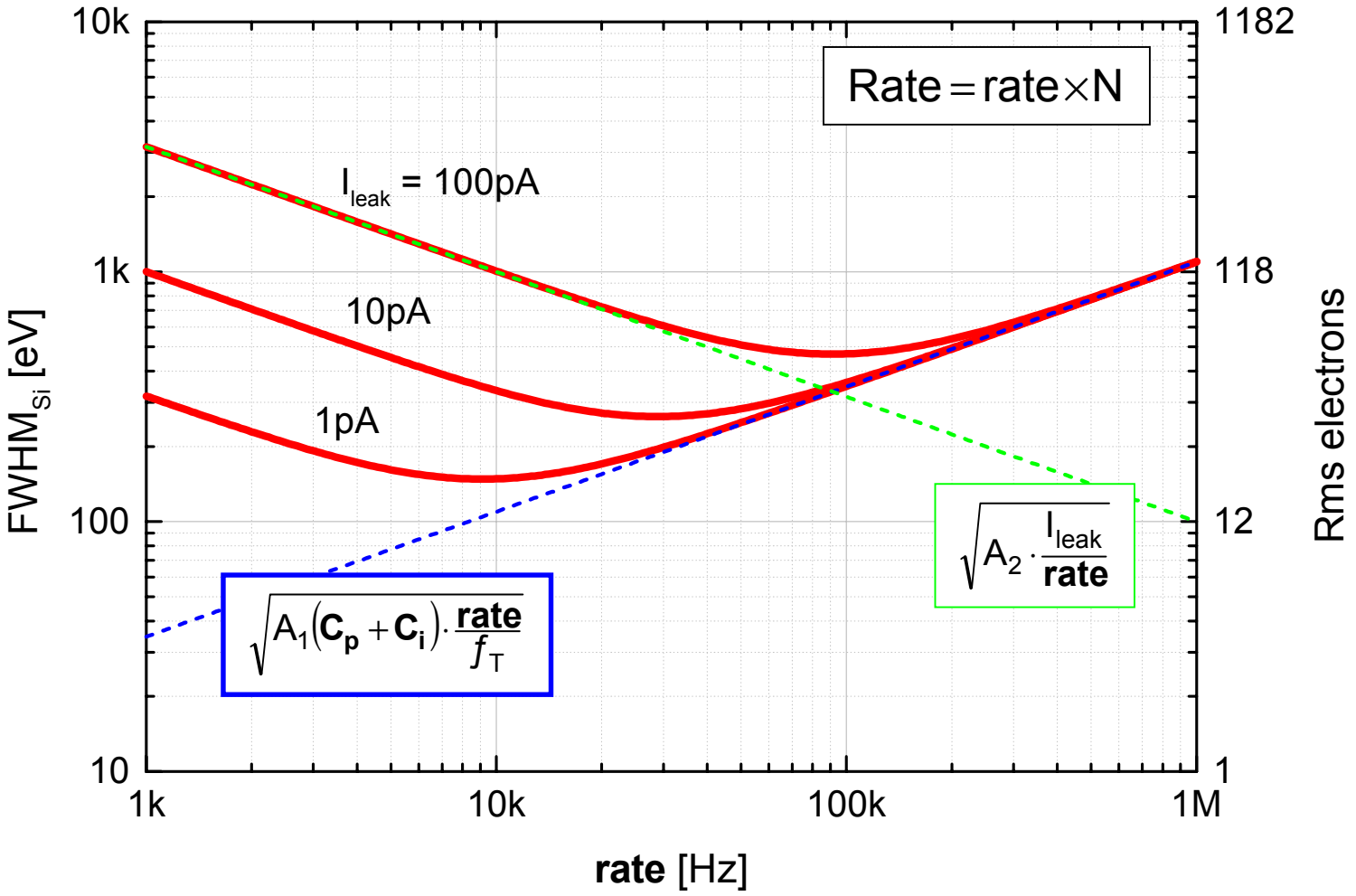


$$\text{rate} = \frac{\text{Rate}}{N} \quad (N = \text{number of pixels})$$

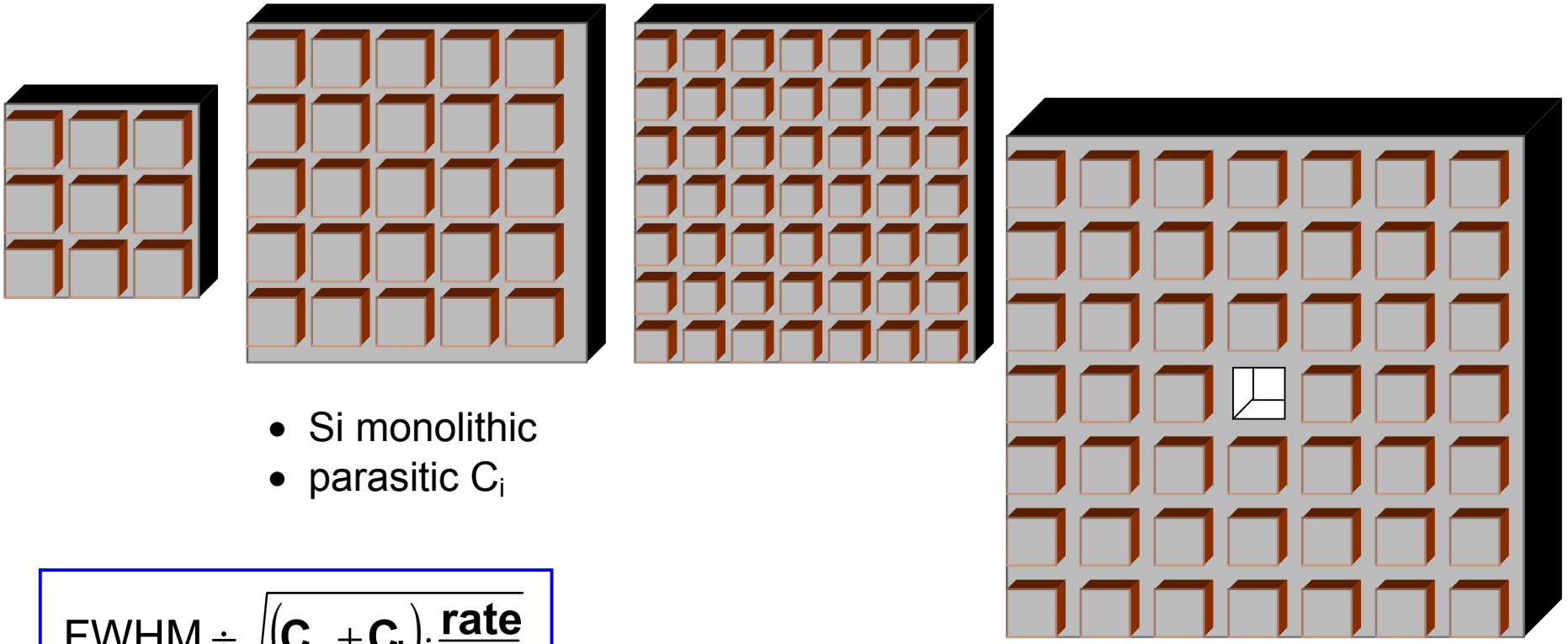


$$\text{FWHM} = \sqrt{A_1\left(\mathbf{C_p} + \mathbf{C_i}\right)\cdot\frac{\mathbf{rate}}{f_T} + A_2\cdot\frac{I_{leak}}{\mathbf{rate}}}$$

Resolution vs rate



Optimum segmentation



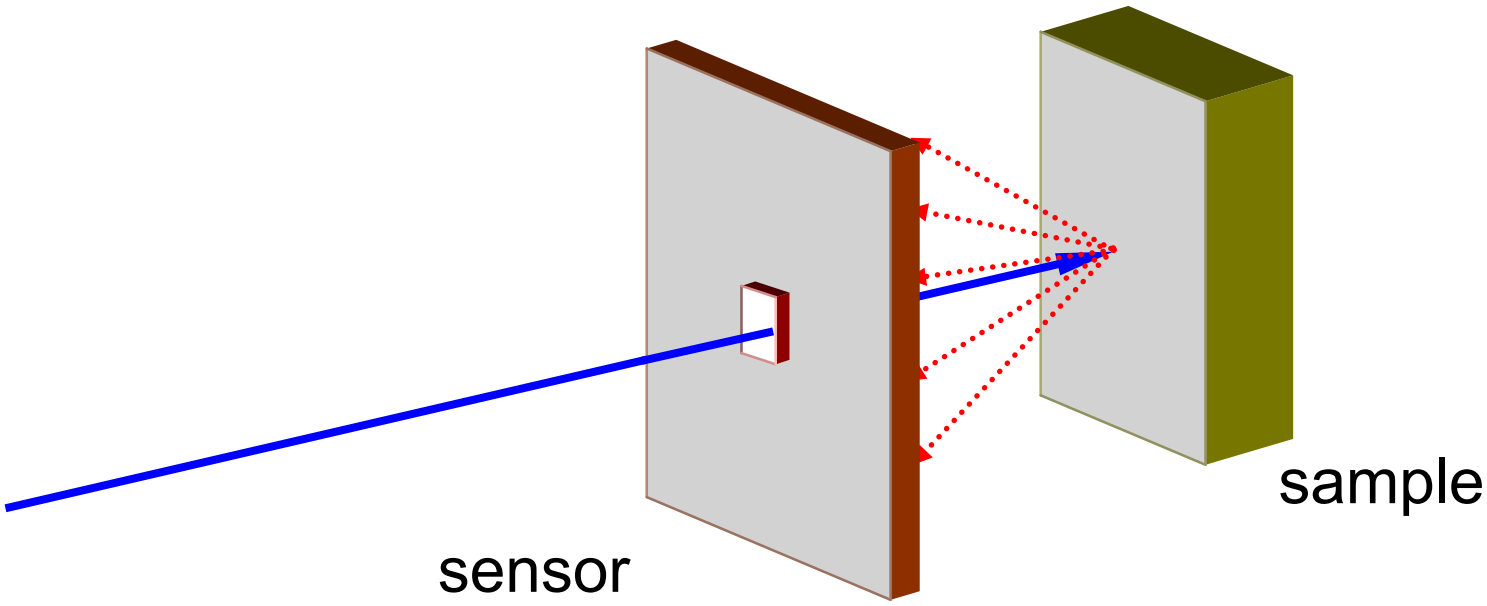
- Si monolithic
- parasitic C_i

$$\mathrm{FWHM} \div \sqrt{\left(C_p + C_i\right) \cdot \frac{\mathrm{rate}}{f_T}}$$

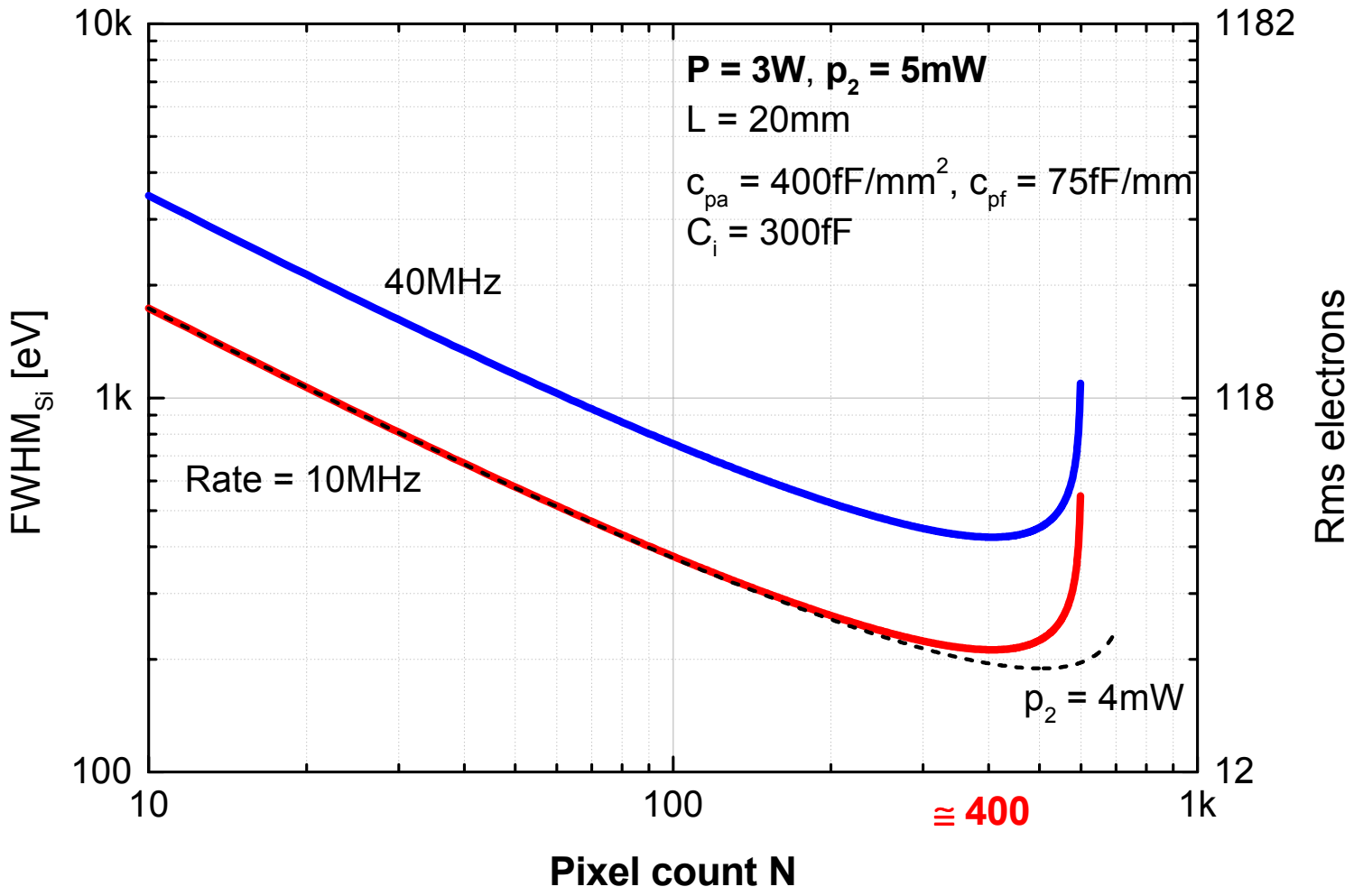
- front-end electronics (channel count, power)
- fringe capacitance (component of C_p)
- parasitic C_i
- charge sharing (≈20µm/side) and trapping (gap/side)

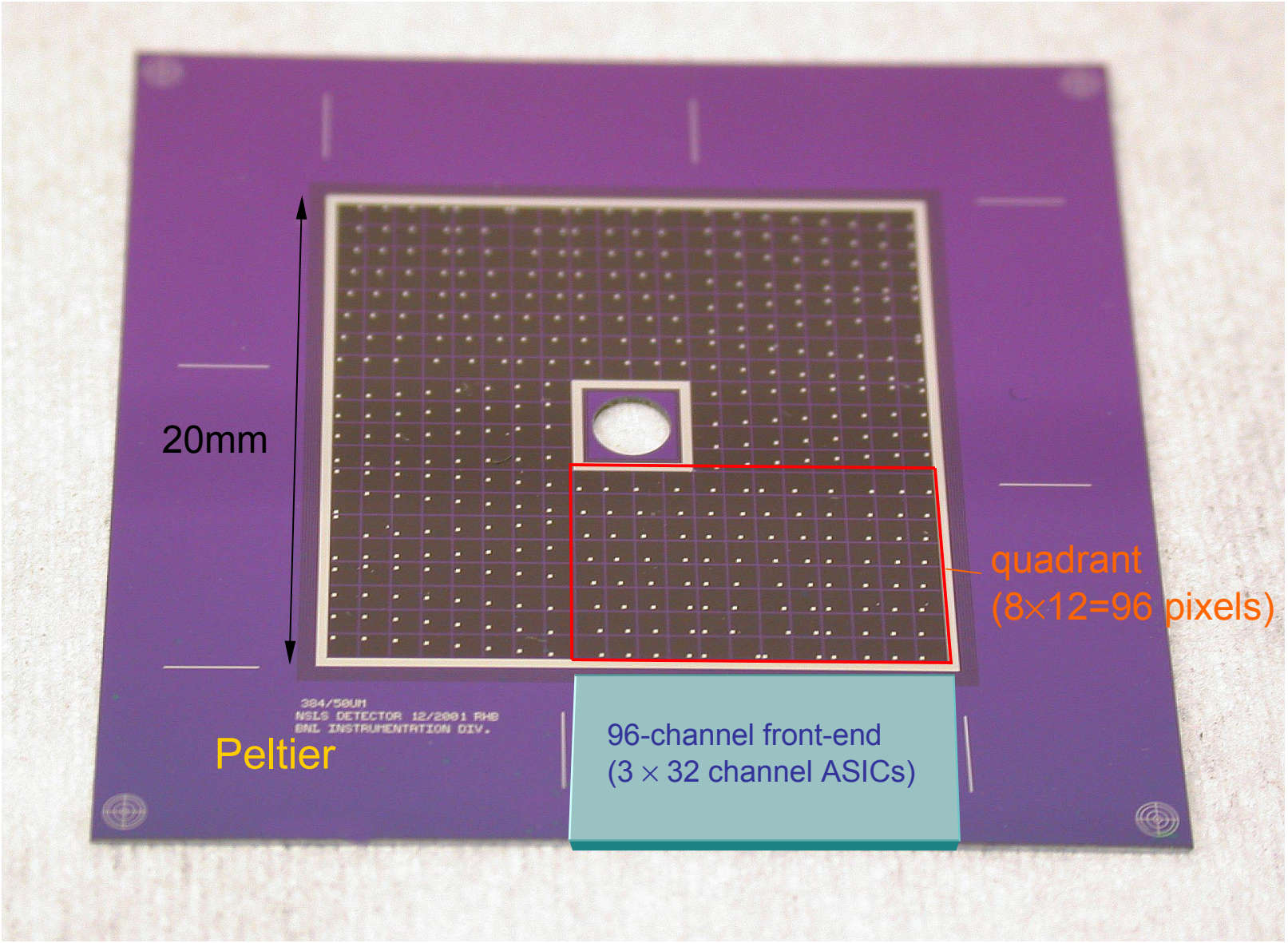
2^{nd} order,
empirical approach

Beam through



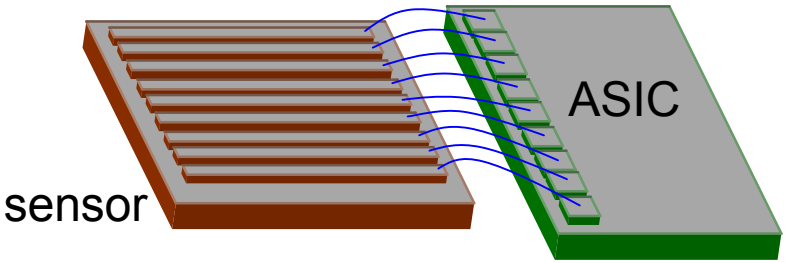
$$\mathrm{FWHM} \div \sqrt{\left[c_{pa}\left(\frac{L}{\sqrt{N}}\right)^2 + c_{pf}\frac{L}{\sqrt{N}} + C_i\right]\cdot\frac{\mathrm{Rate}}{N}\cdot\frac{1}{\sqrt{\frac{P}{N}-p_2}}}$$



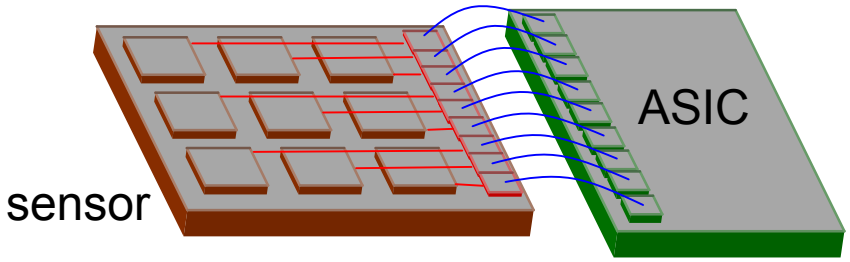


Si n-type high resistivity wafer 250μm thick,
N = 384 p^+ ≈1mm×1mm pixels,
gaps 10μm, 30μm, 50μm

Interconnecting pixel to front-end electronics



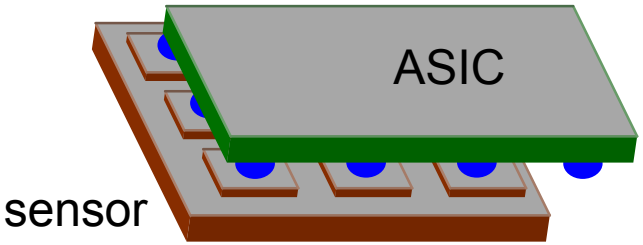
+ interconnect parasitic
+ bond length
- fringe capacitance
- charge sharing and trapping



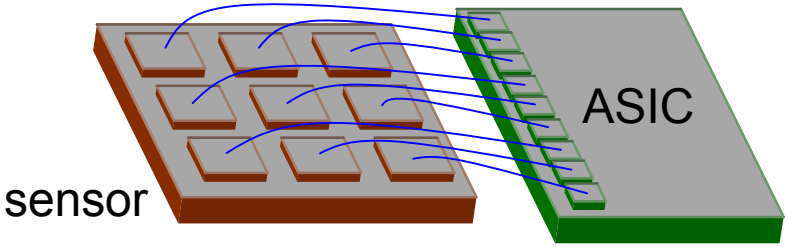
+ bond length
- interconnect parasitic
- dielectric losses

6mm×10µm, Si_3N_4 (ε_r=6.5,$tan(\delta)$=0.001), 3µm, $C_i \approx 1.2pF$

$$\delta FWHM_{loss} = 8.5/q \cdot \sqrt{2kT\,C_p\,tan(\delta)} \approx 170eV$$

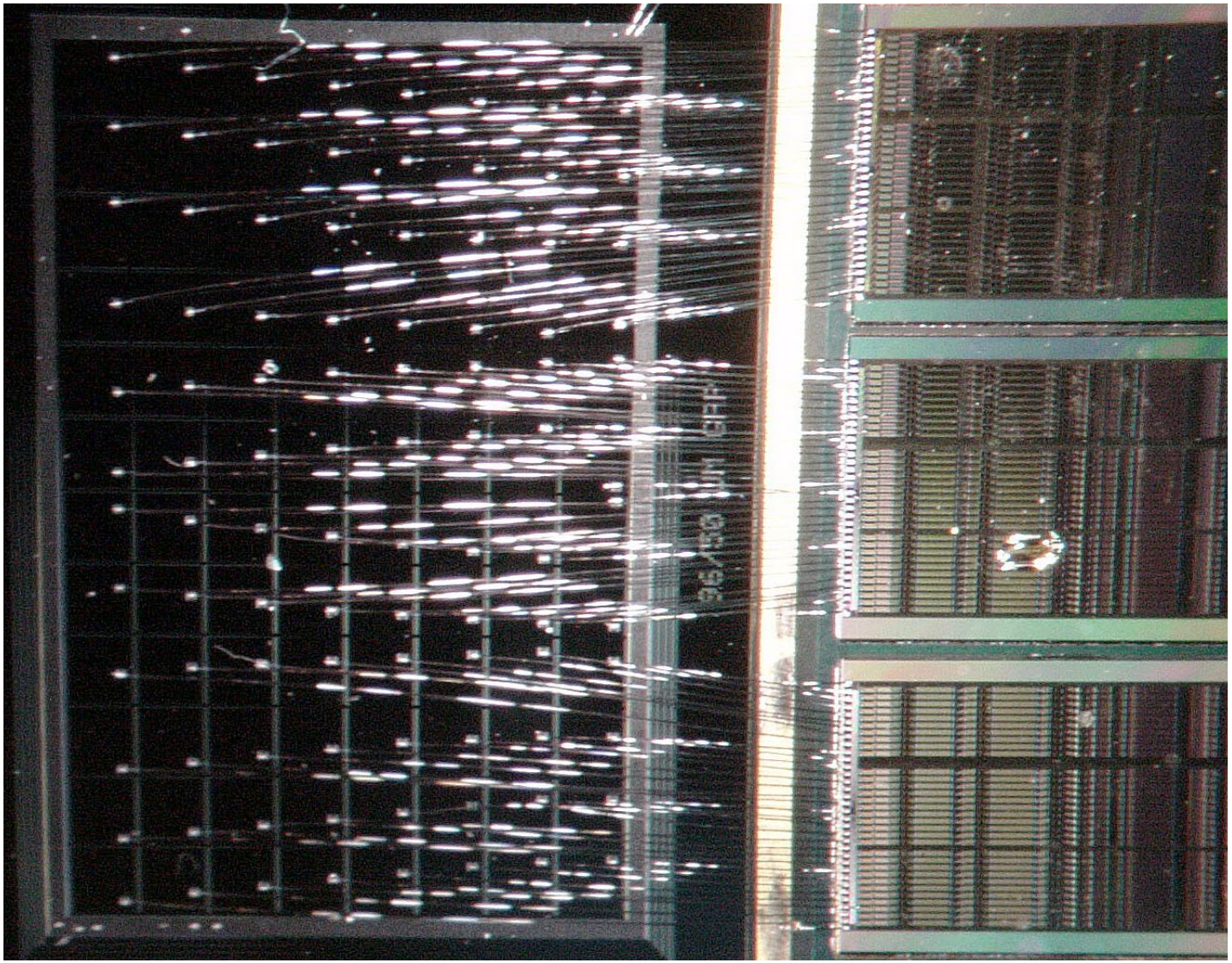


+ interconnect parasitic
- constraint on ASIC area and layout
- fluorescence from Pb (Sn/Pb/Ag)
- illumination from segmented side



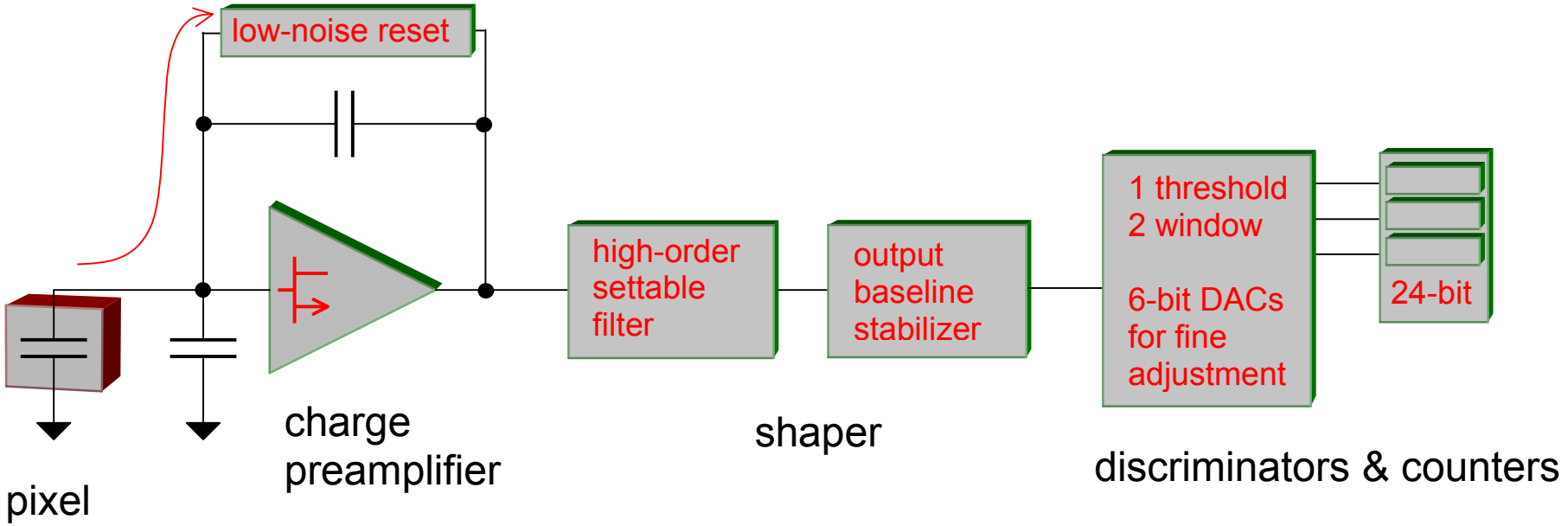
+ dielectric losses
± interconnect parasitic
- bond length

Detector-ASIC photo



quadrant

Front-end channel overview



≈ 3 mW

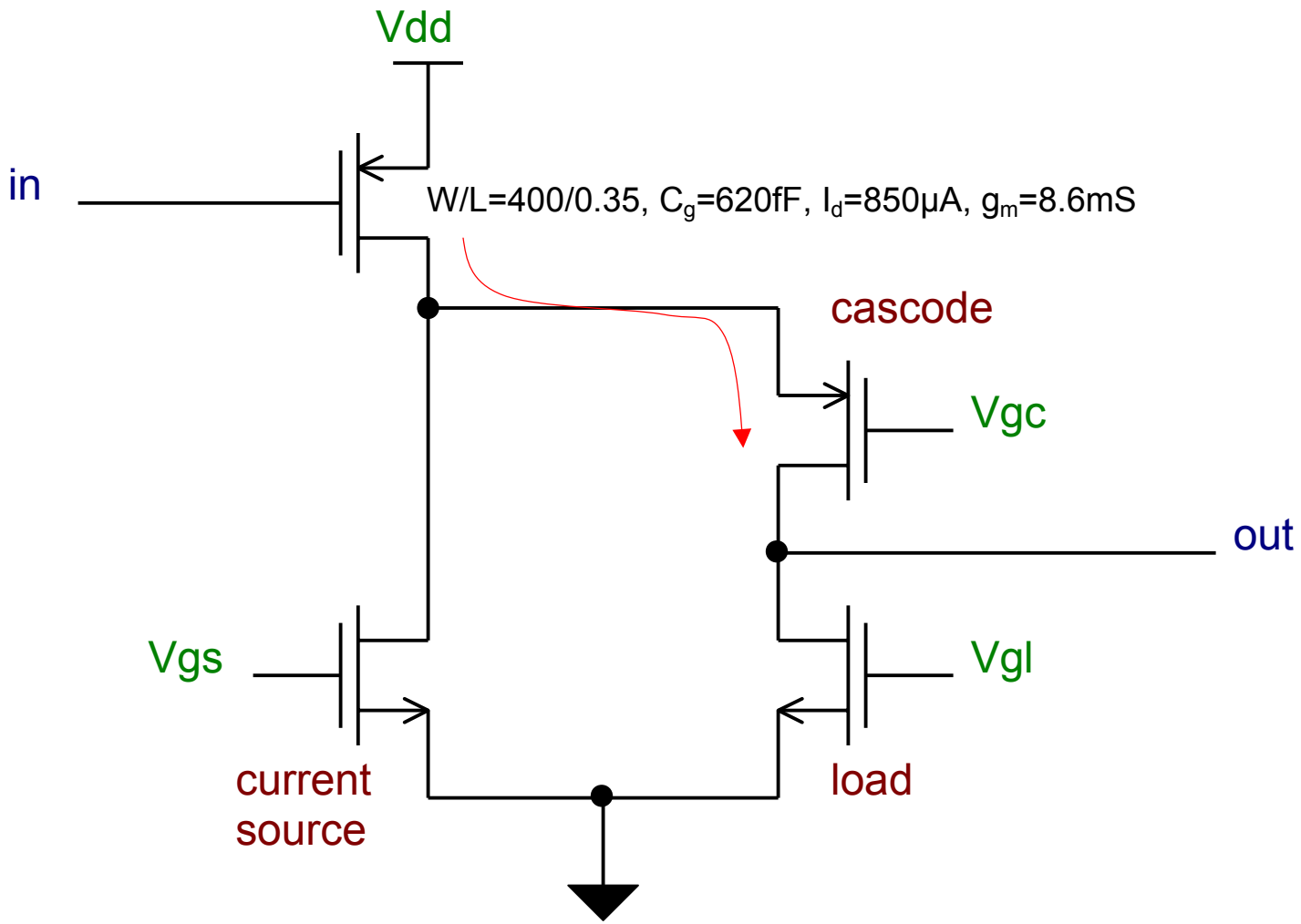
≈ 5 mW

SPI

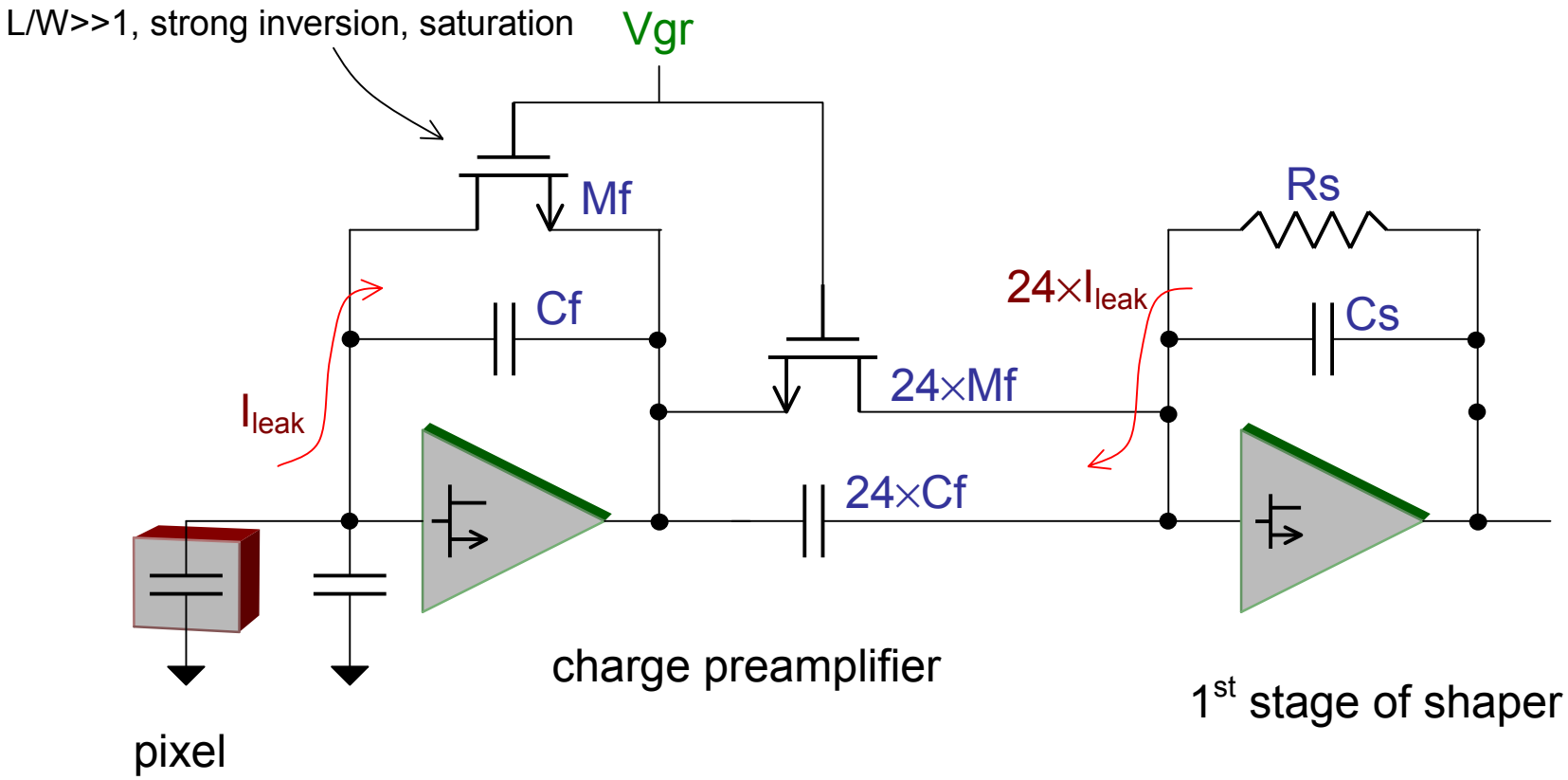
readout

Technology CMOS 0.35µm 3.3V 2P4M

Charge preamplifier



Continuous reset

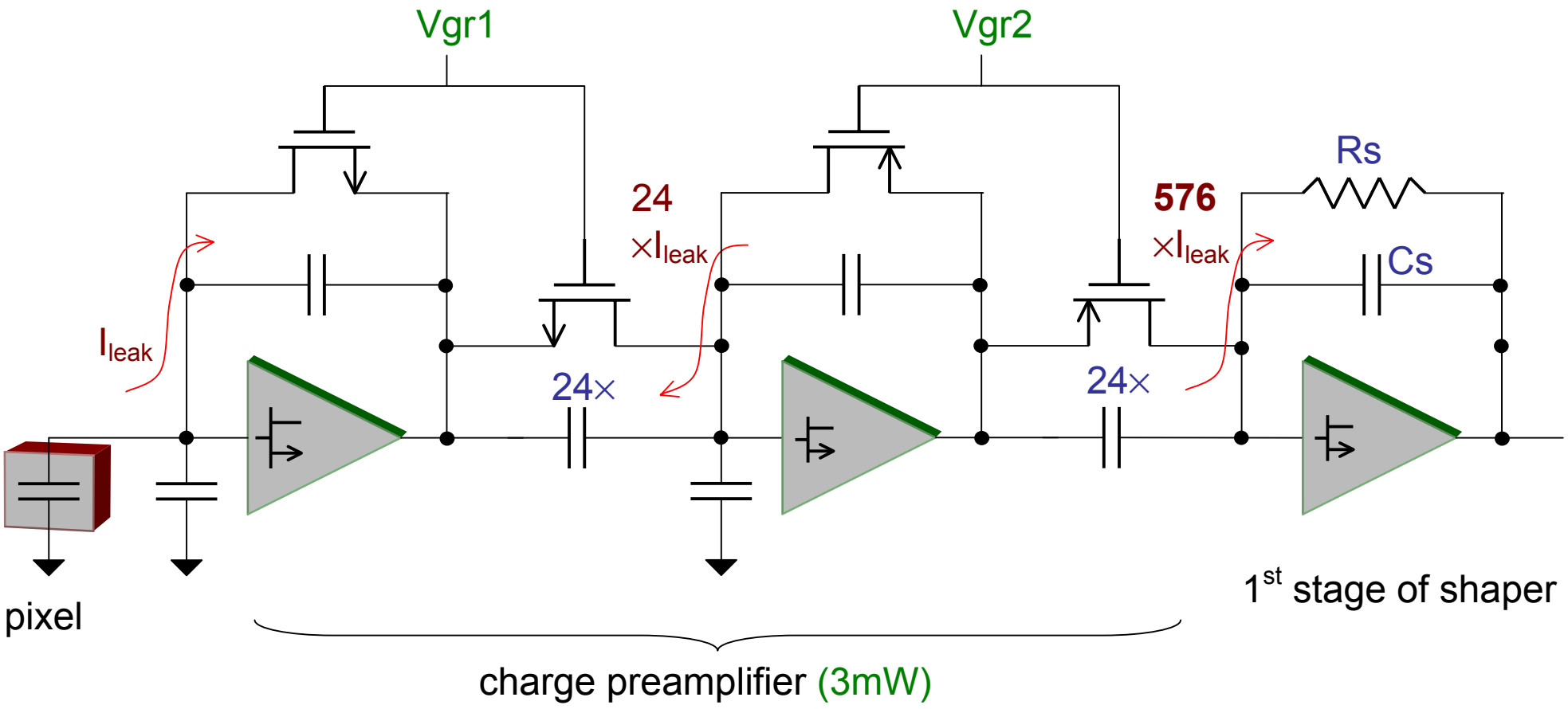


- current gain of 24
- fully linear
- self-adapts to leakage current
- minimum noise contribution

Continuous reset – dual stage

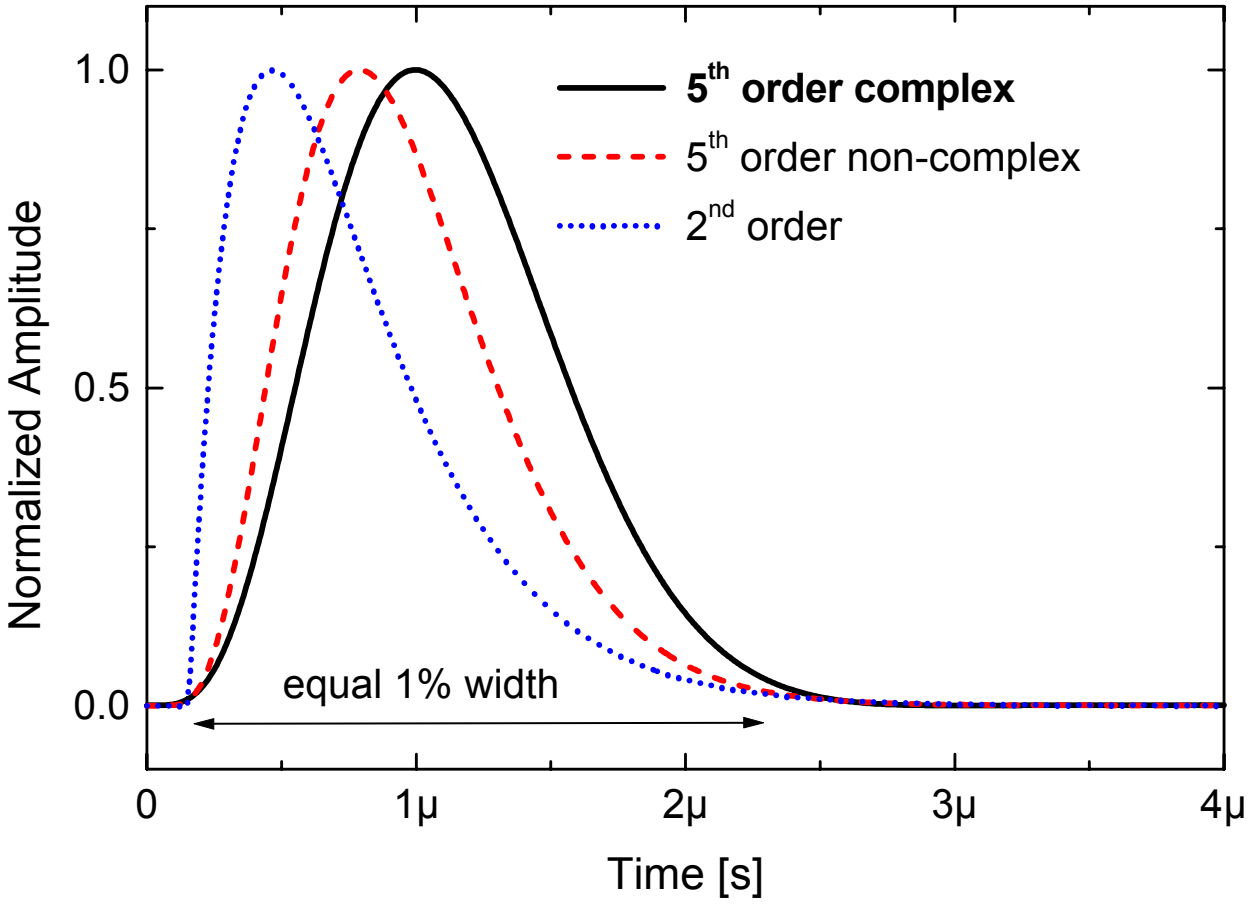
$$\frac{2kT}{Rs}\frac{1}{24^2} \equiv q \cdot I_{eq}$$

$$Rs \approx 200k\Omega \rightarrow I_{eq} \approx 500pA$$



$$Rs \approx 200k\Omega \rightarrow I_{eq} \approx 0.75pA$$

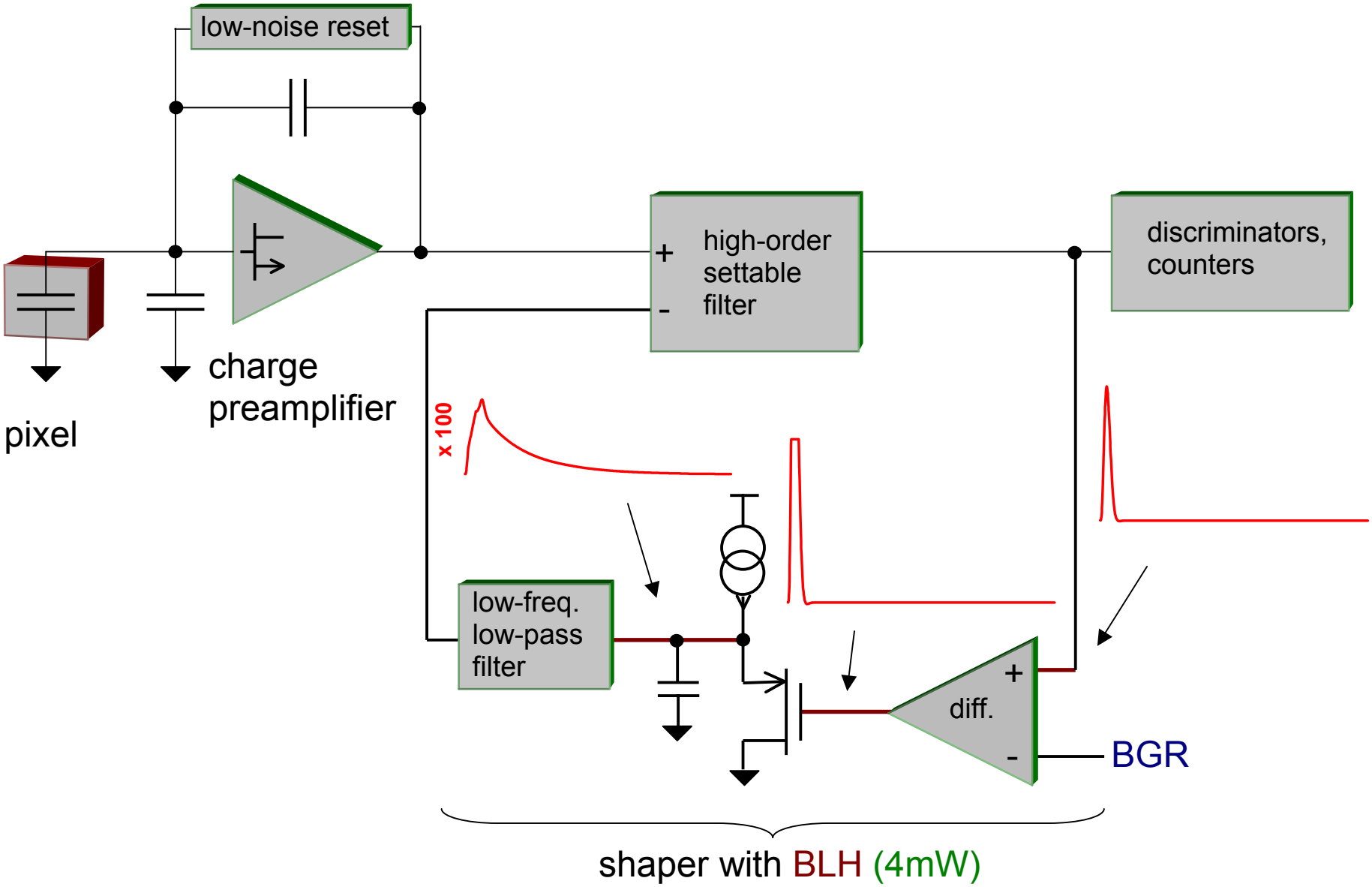
Shaping



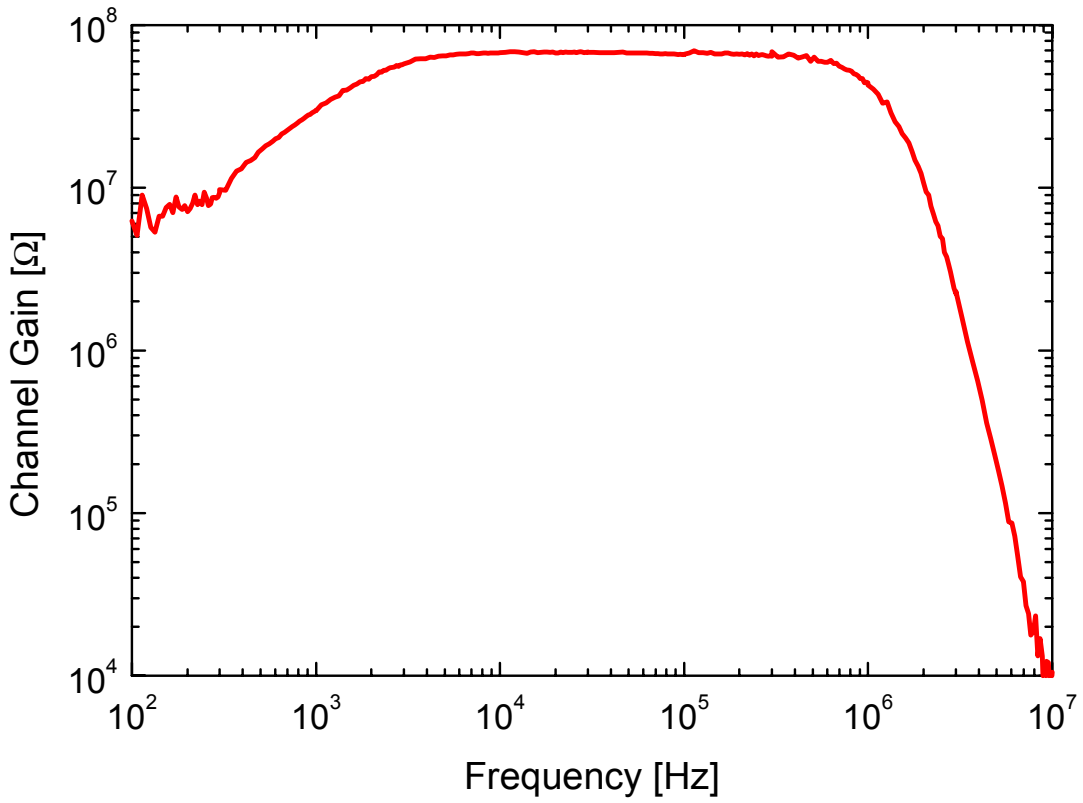
$$FWHM=\sqrt{\alpha \cdot A_1\left(C_p+C_i\right)\cdot\frac{rate}{f_T}}$$

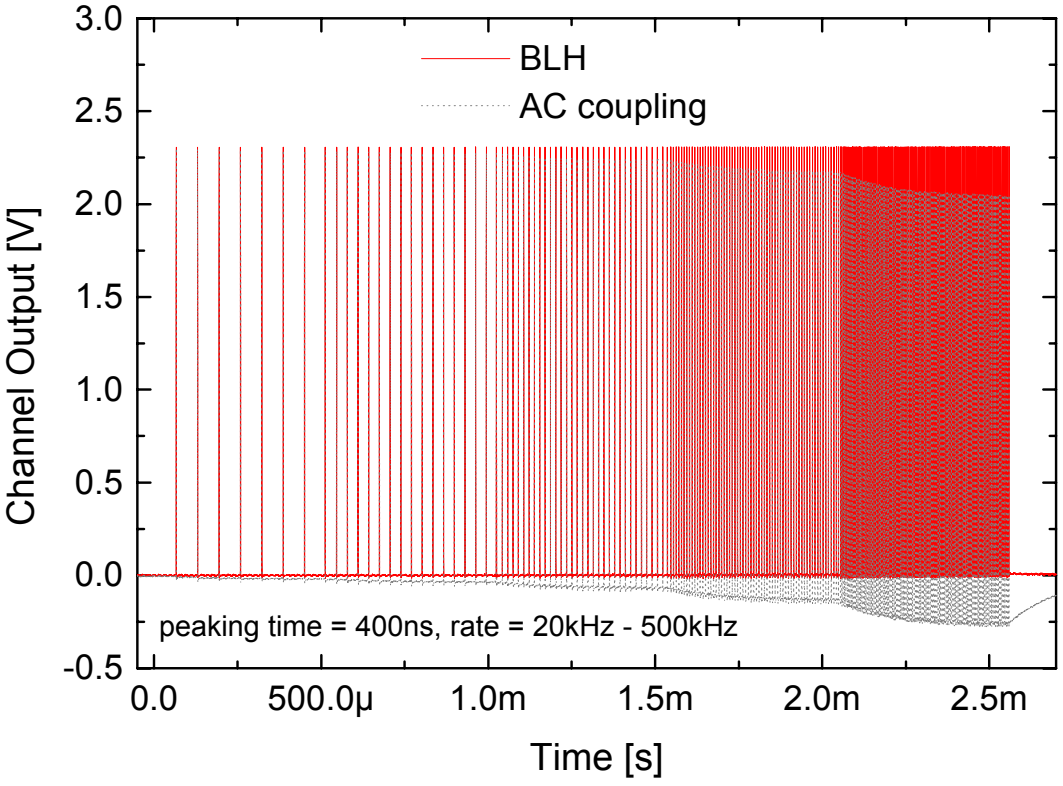
	α
5th cpx	**5.5**
5th	6.8
2nd	14.5

Baseline stabilization

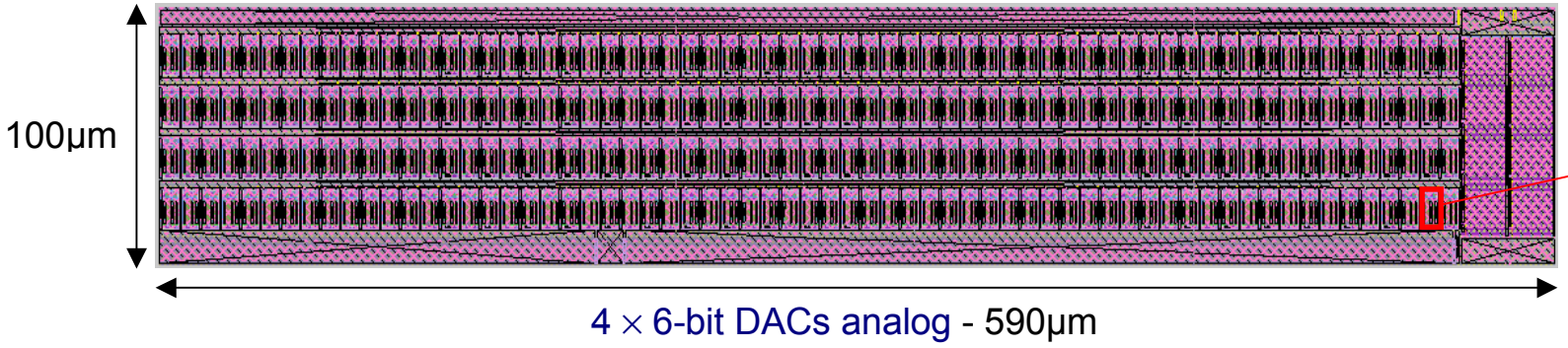


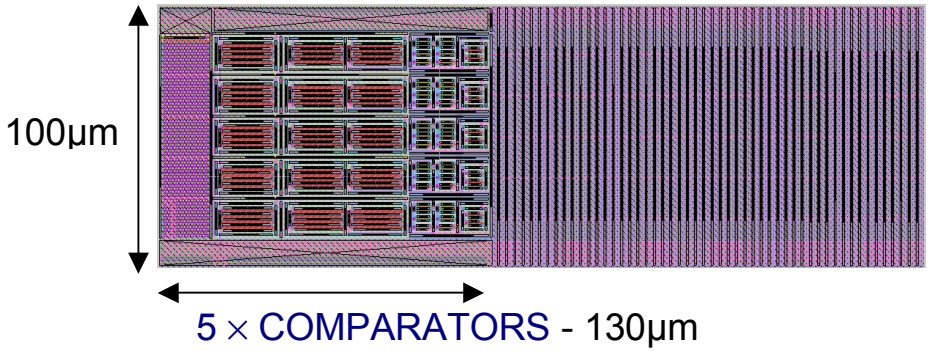
Baseline stabilization (BLH)

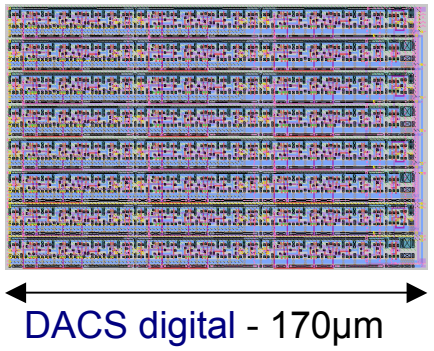


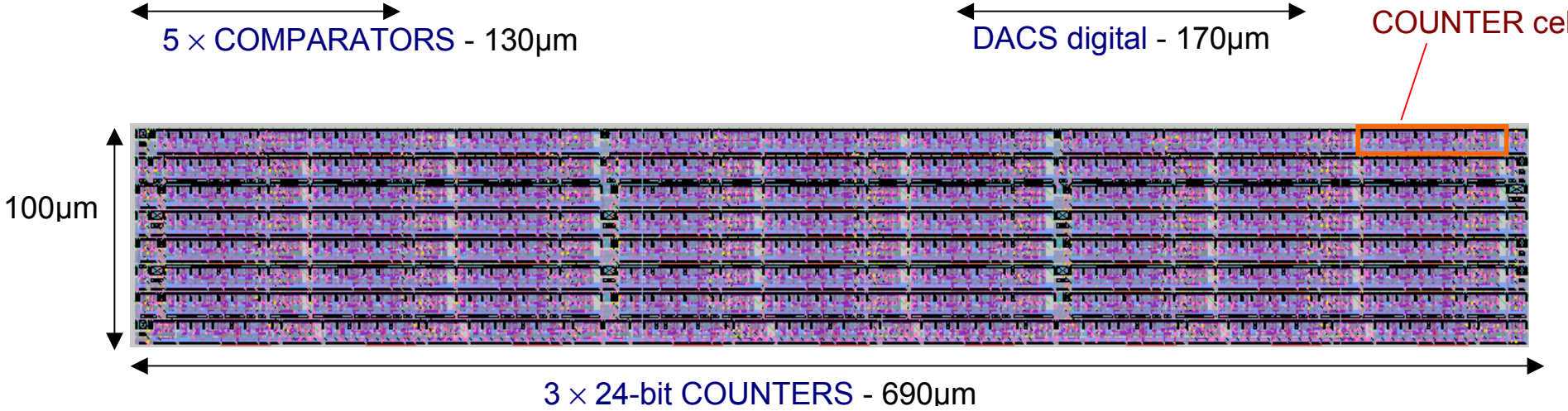


Layout (CMOS 3.3V 2P4M 0.35µm)







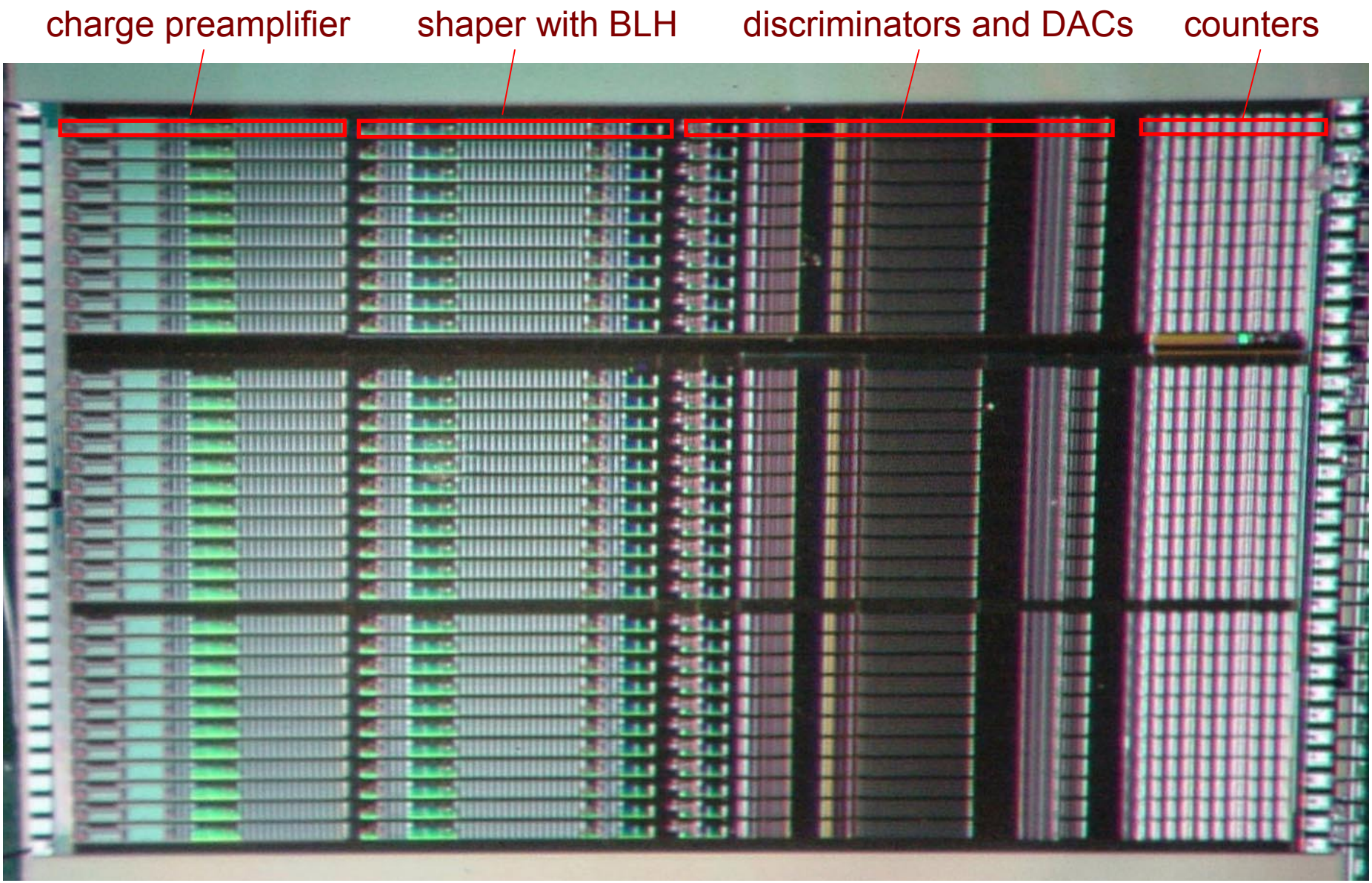


ASIC overview

CMOS 0.35µm 3.3V 2P4M
180,000 MOSFETs, size 3.6×6.3 mm^2
8mW / channel

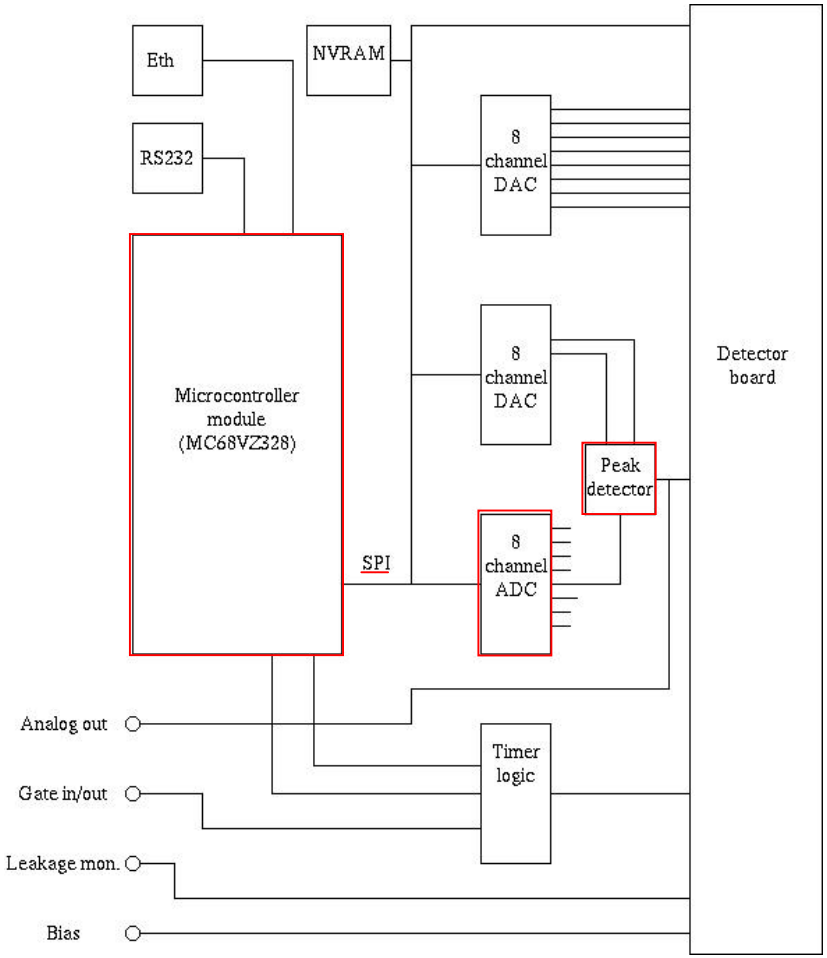
- 32 readout channels
  - self adaptable continuous reset
  - high order shaper
    - settable peaking time (0.5µs, 1µs, 2µs, 4µs)
    - settable gain (750mV/fC, 1500mV/fC)
    - band-gap referenced output baseline
    - output baseline stabilization (BLH)
  - 1 threshold and 2 window discriminators
  - 4× 6-bit DACs for fine window adjustments
  - 3× 24-bit counters
  - test mode
  - analog output monitor
  - pixel leakage current monitor
- Serial Peripheral Interface (SPI)
  - global settings
  - monitors enabling
  - test enabling
  - channels masking
  - DACs setting
  - counters readout

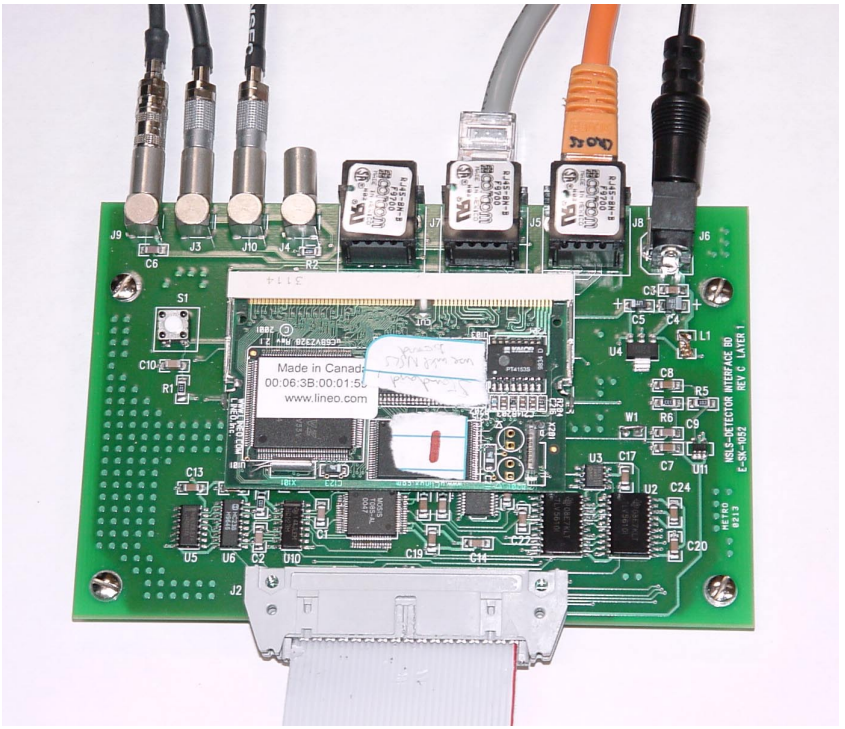
ASIC photo



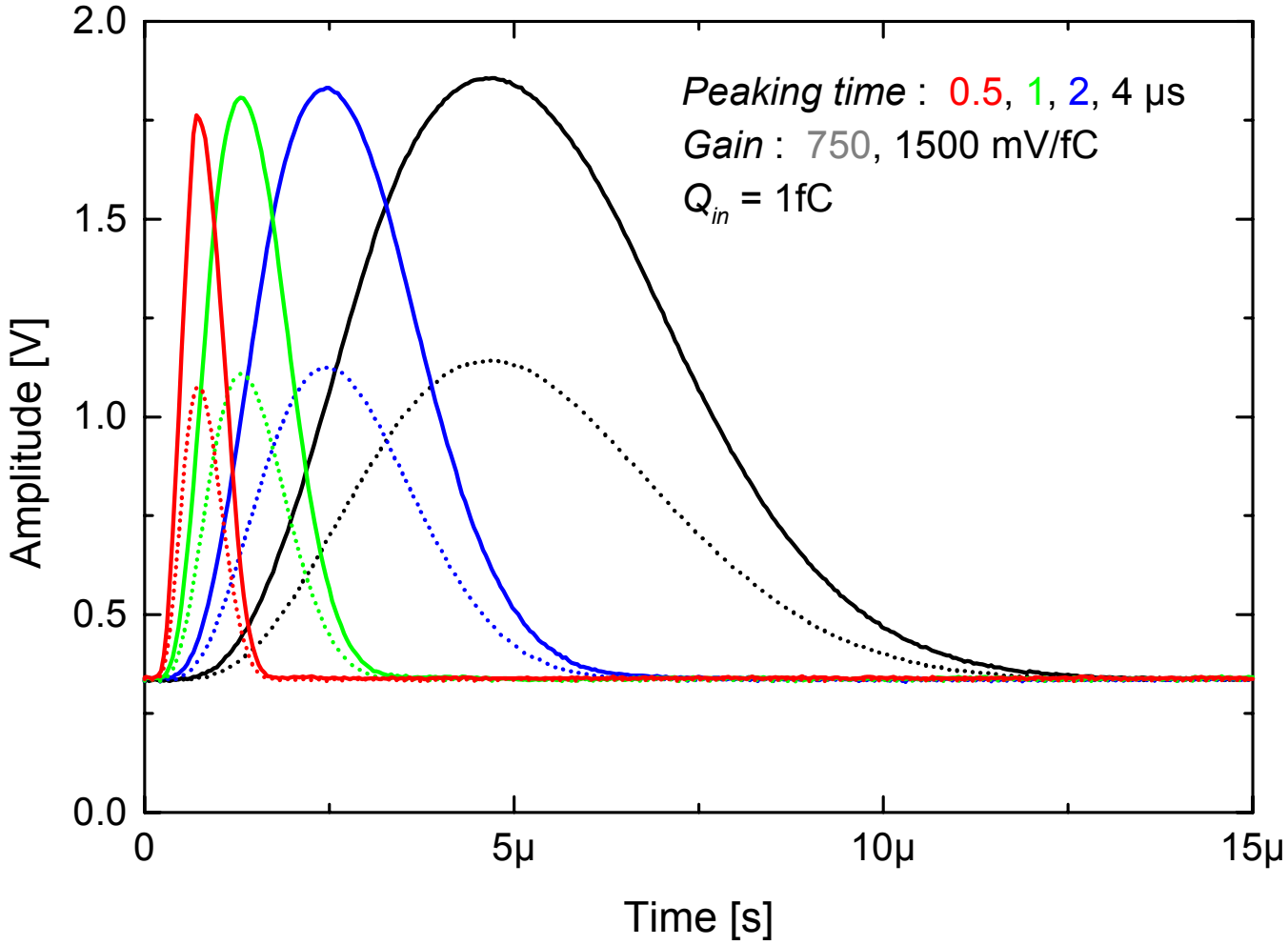
32 channels, 3.6 × 6.3 mm²

Readout

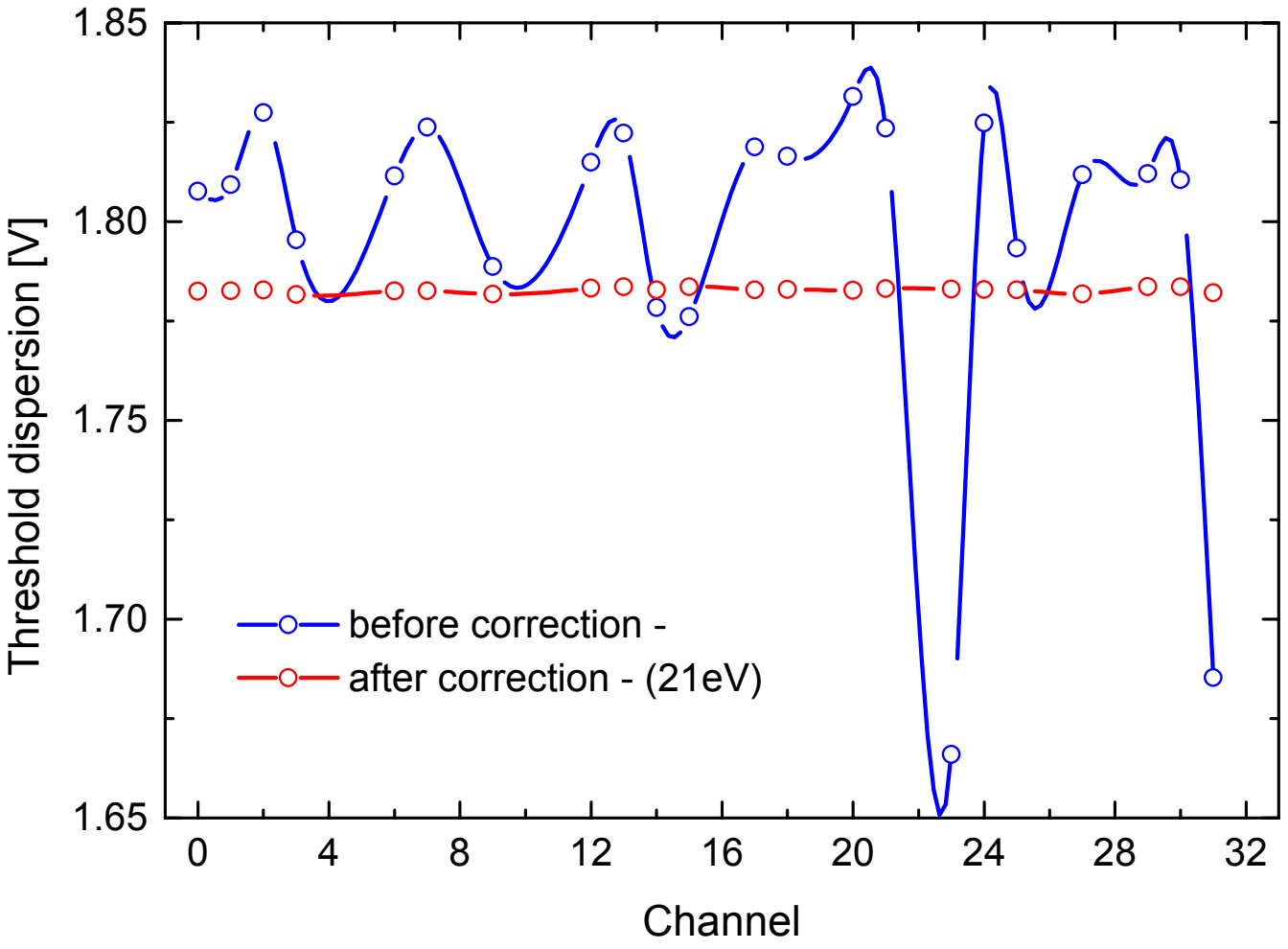

Eth
NVRAM
RS232
8 channel DAC
8 channel DAC
Microcontroller module (MC68VZ328)
Peak detector
Detector board
SPI
8 channel ADC
Analog out
Timer logic
Gate in/out
Leakage mon.
Bias



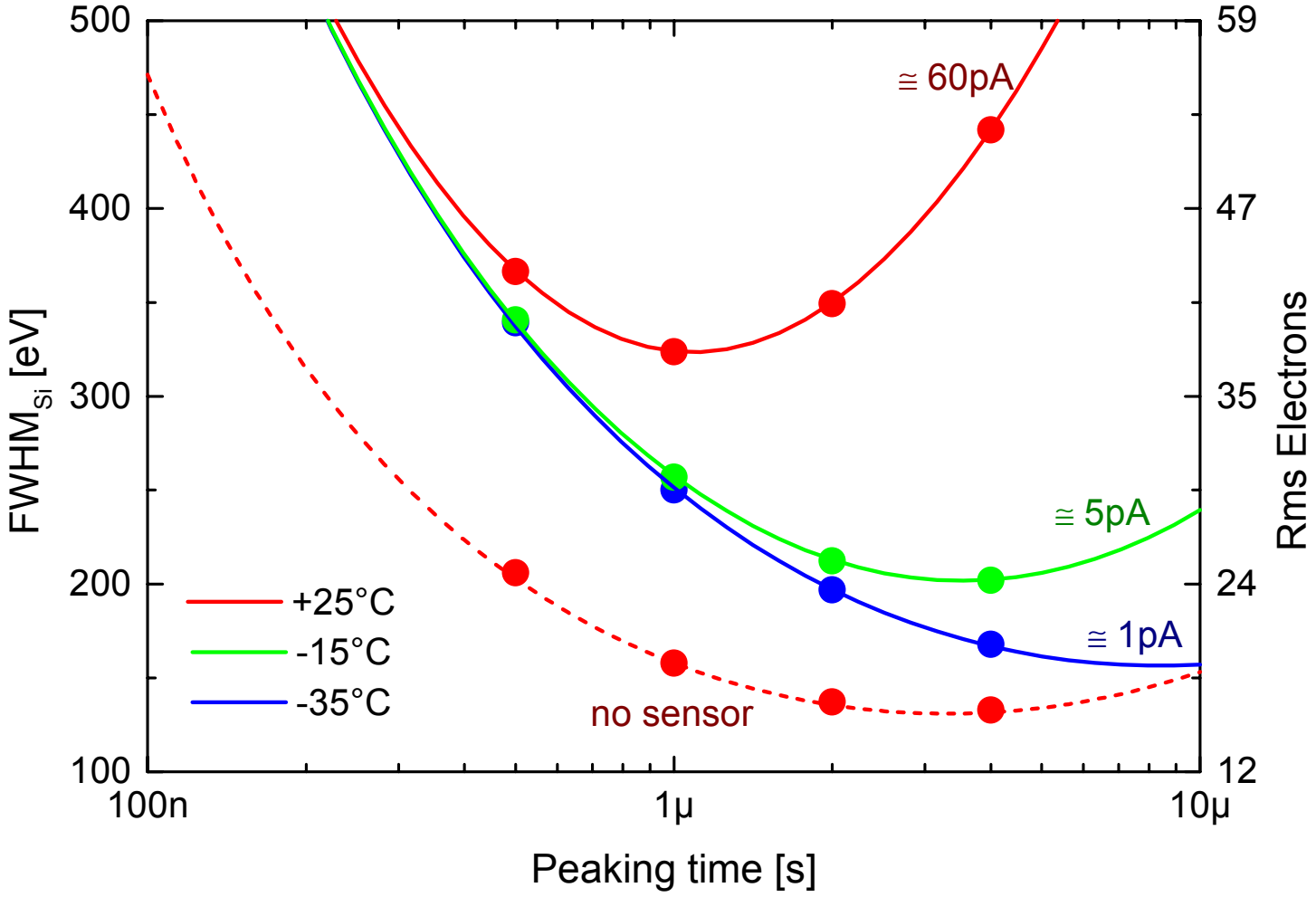
Experimental



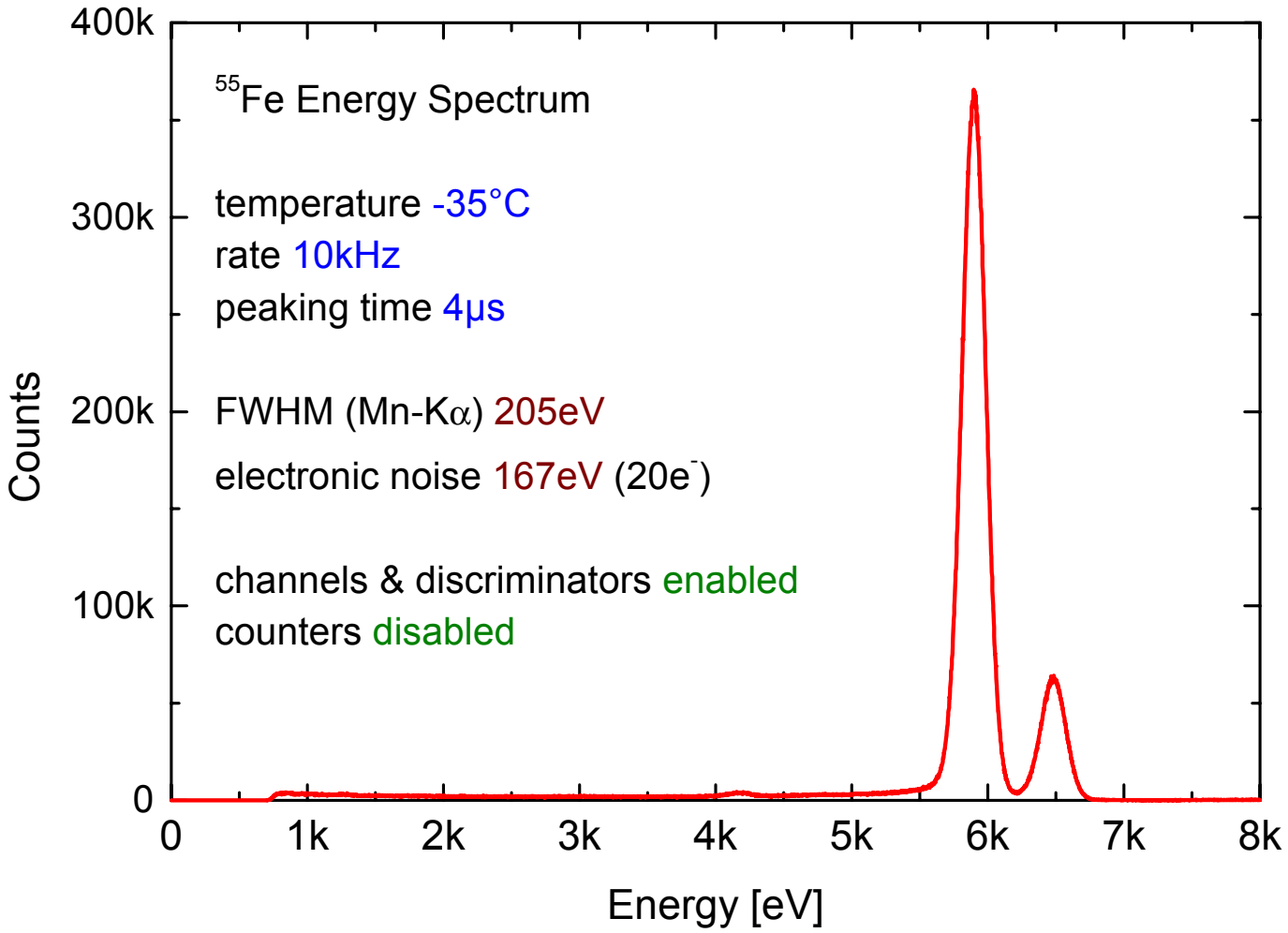
Experimental



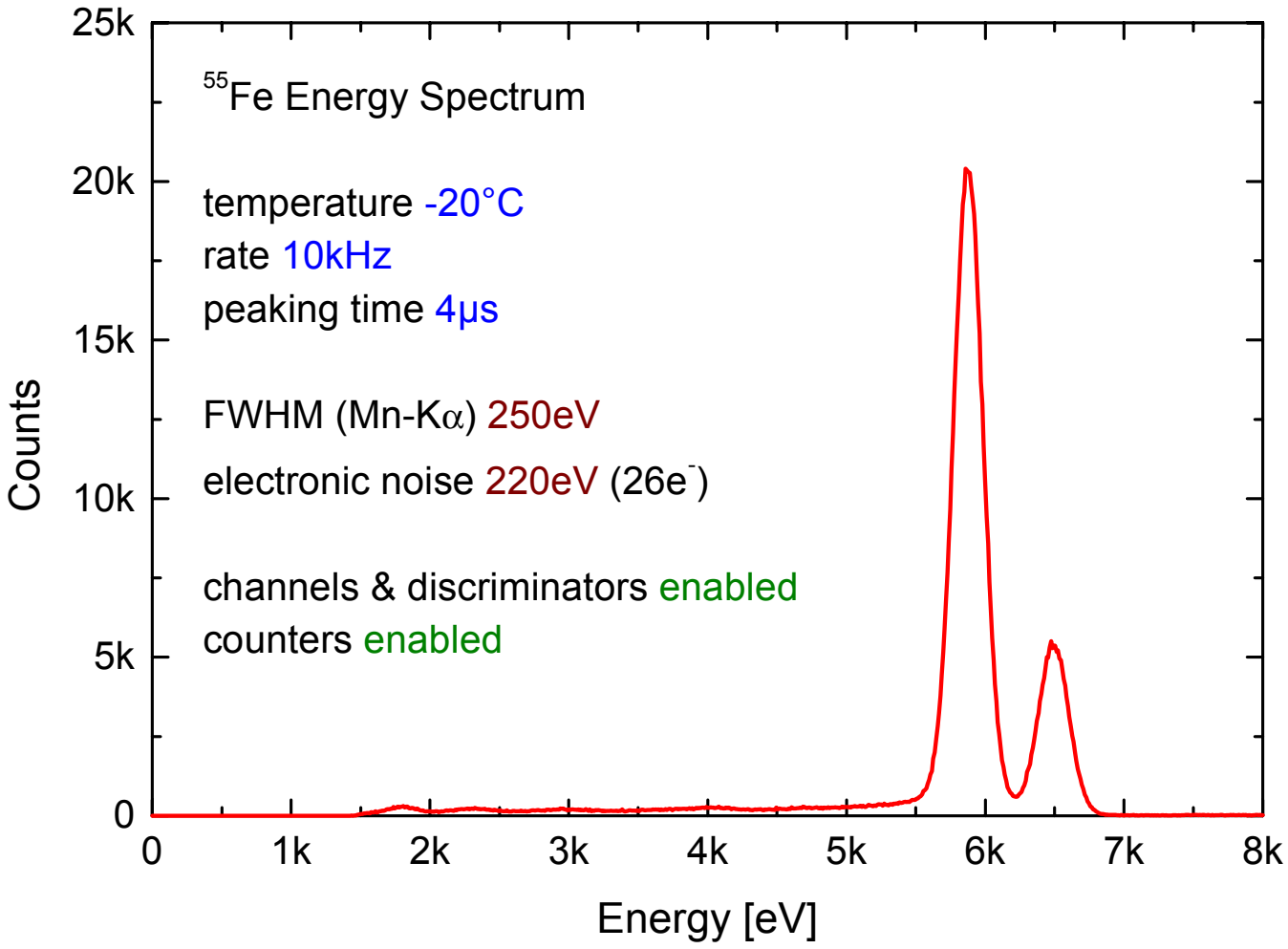
Experimental



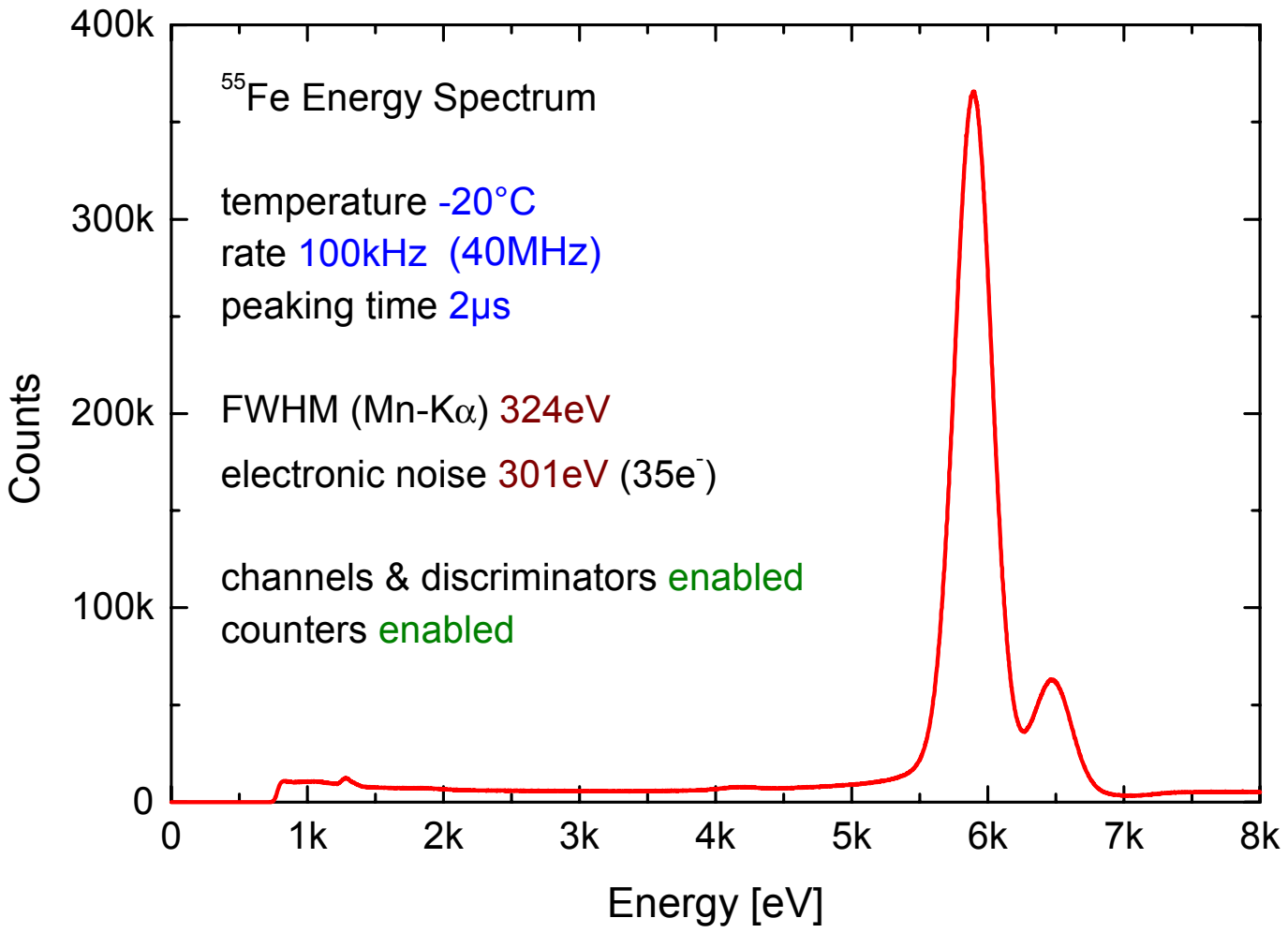
Experimental



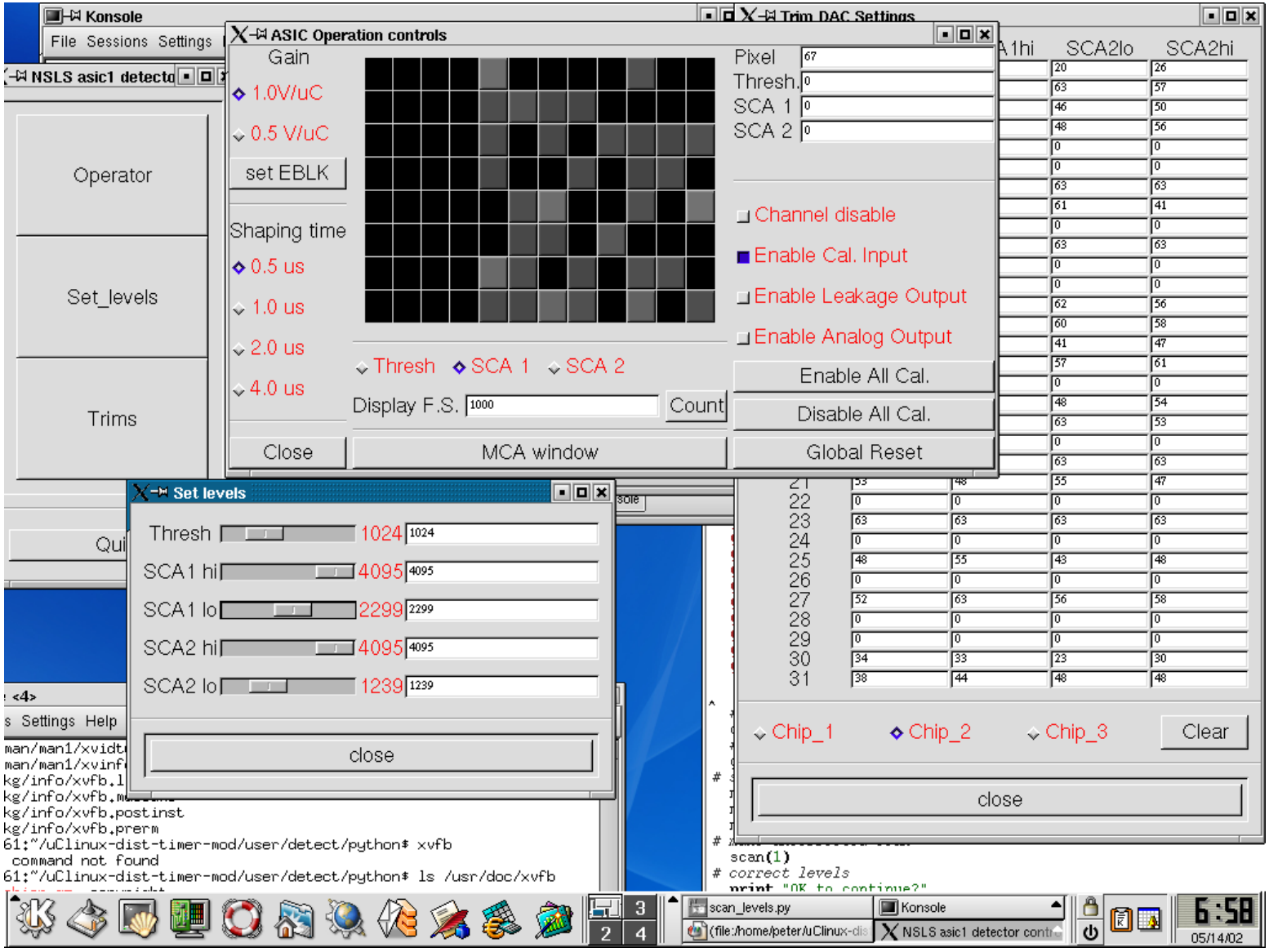
Experimental



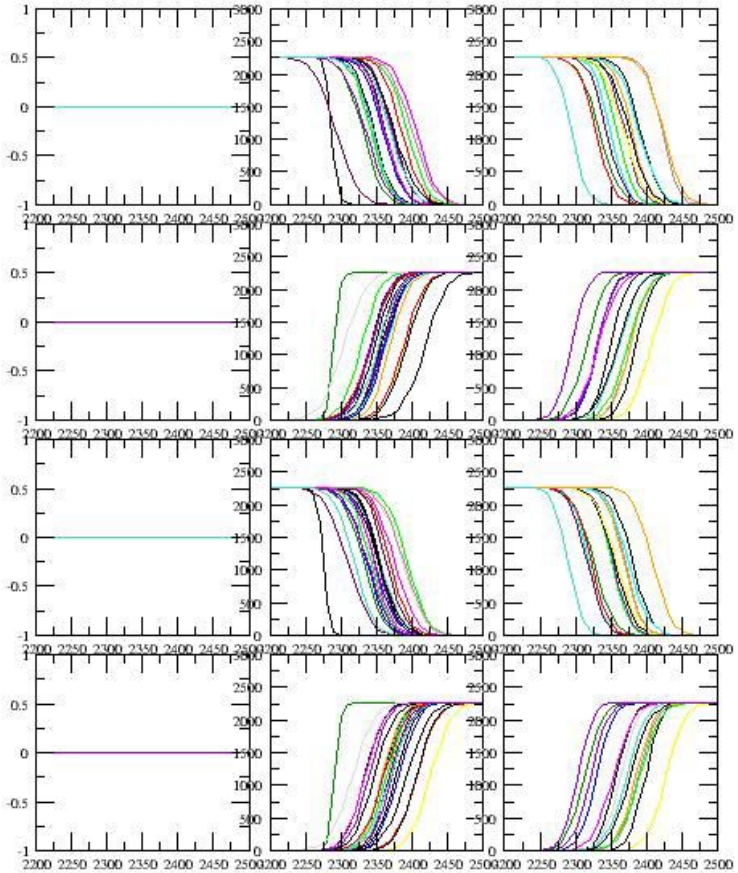
Experimental



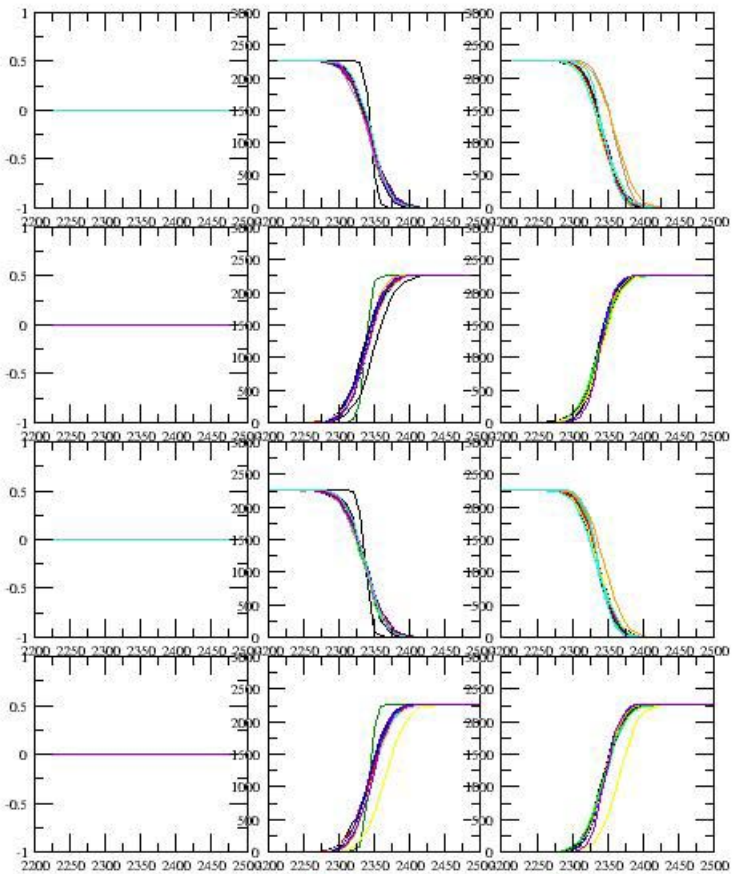
Readout interface



Automatic threshold equalization



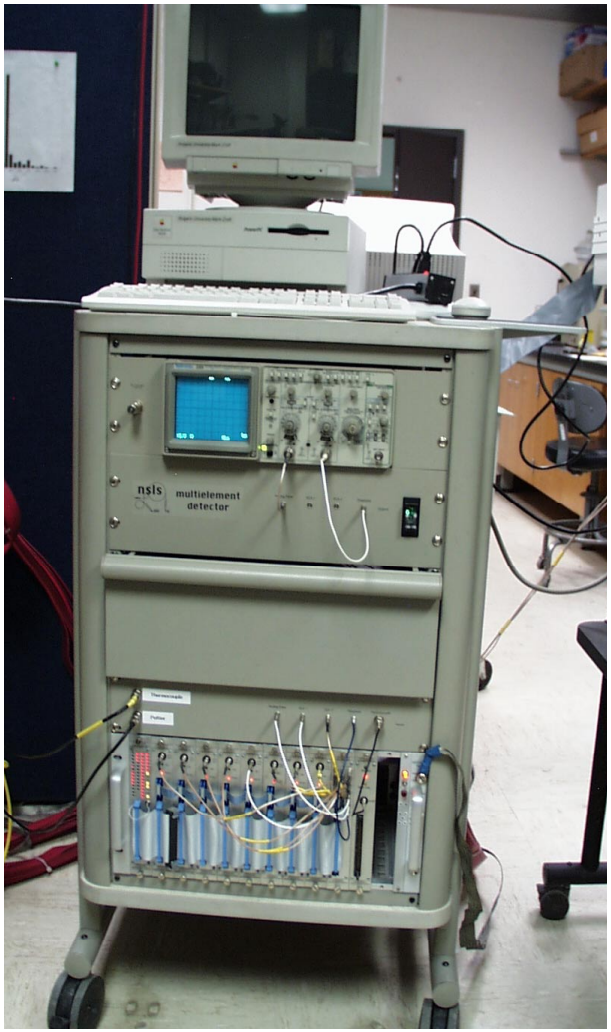
before correction



after correction

Current detector

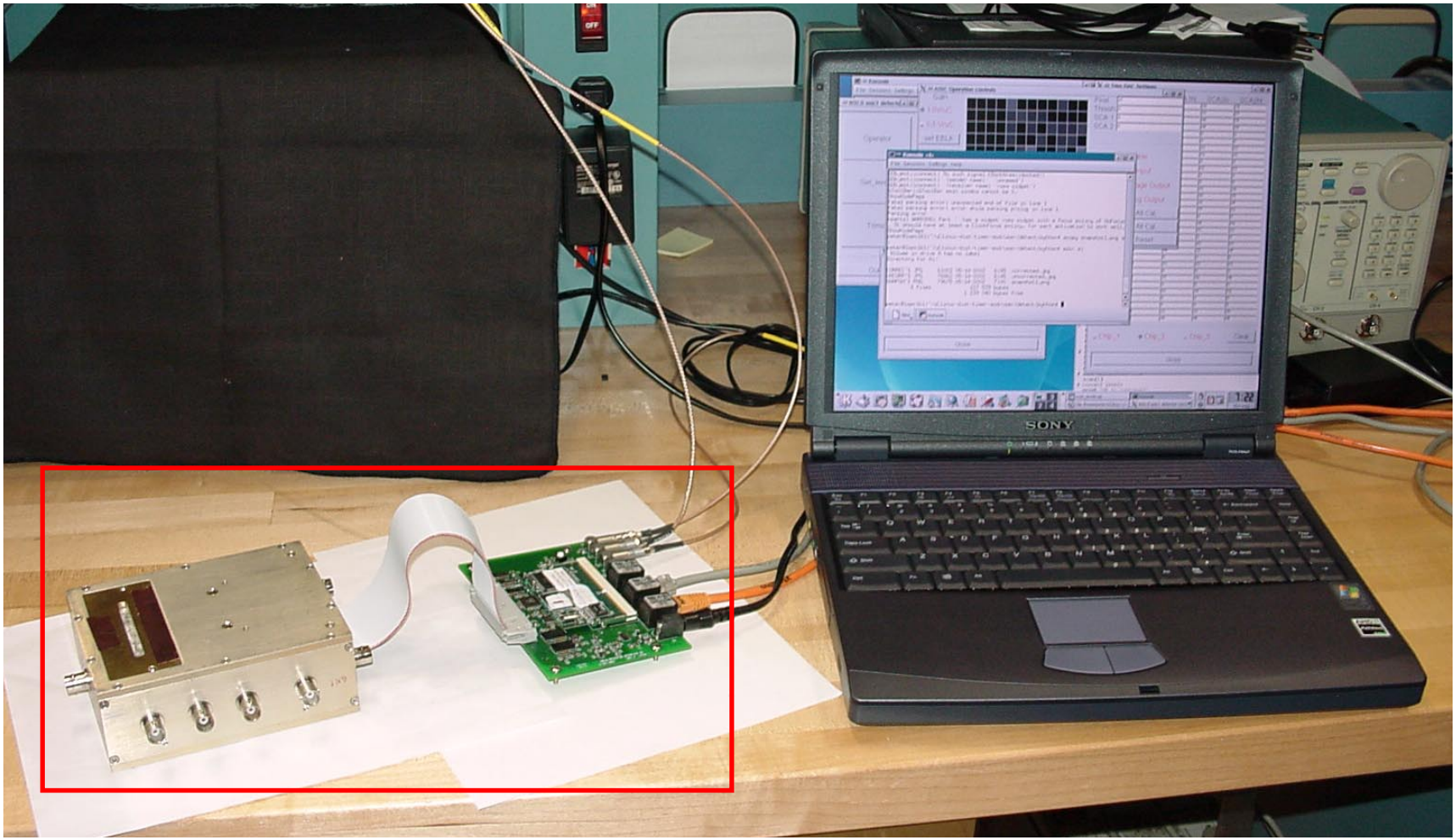
head - preamplifiers



rack – shapers …

≈ 100 channels, > 350 eV, < 1 MHz

New detector



≈ 400 channels, < 300 eV, > 10MHz

Next steps

- Test at high rate (in excess of 50kHz / pixel)
- Gap selection (10μm, 30μm, 50μm)
- ASIC optimization
- Test of four-quadrant version
- Peltier cooler implementation

Acknowledgment

DOE (support)
Veljko Radeka, Pavel Rehak, Graham Smith (discussion)
John Triolo (technical)