



NSLS Annual Users' Meeting  
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# The New Detector for EXAFS at NSLS

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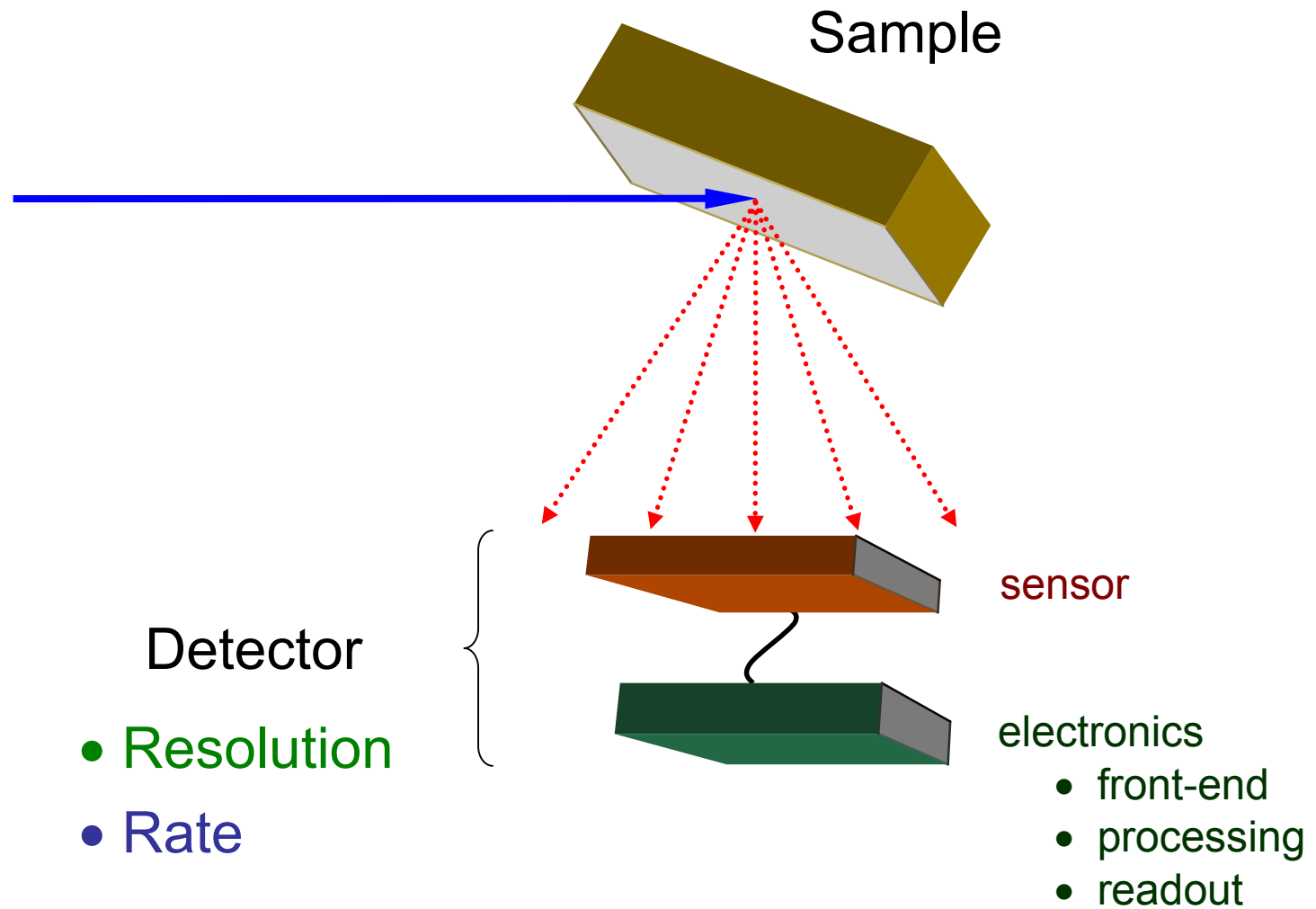
**Gianluigi De Geronimo, Paul O'Connor** - *Microelectronics, Instrum. Div.*, BNL

*Si sensor, interconnect, front-end & processing electronics, readout electronics, assembly*

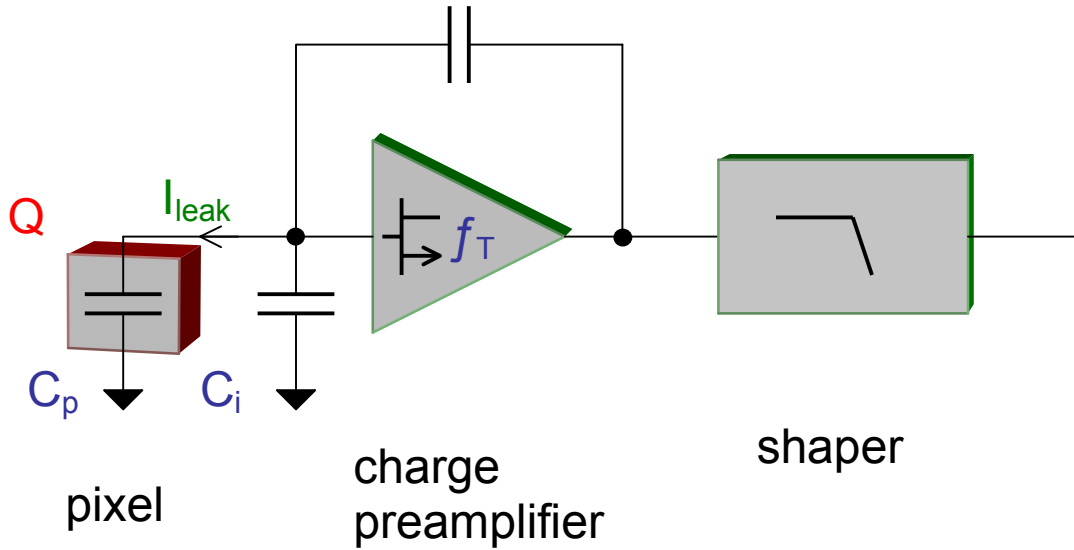
# Outline

- Si sensor
  - segmentation
- Interconnect
- Front-end & processing electronics (ASIC)
  - reset, shaping, stabilization, layout
- Readout electronics
- First experimental results

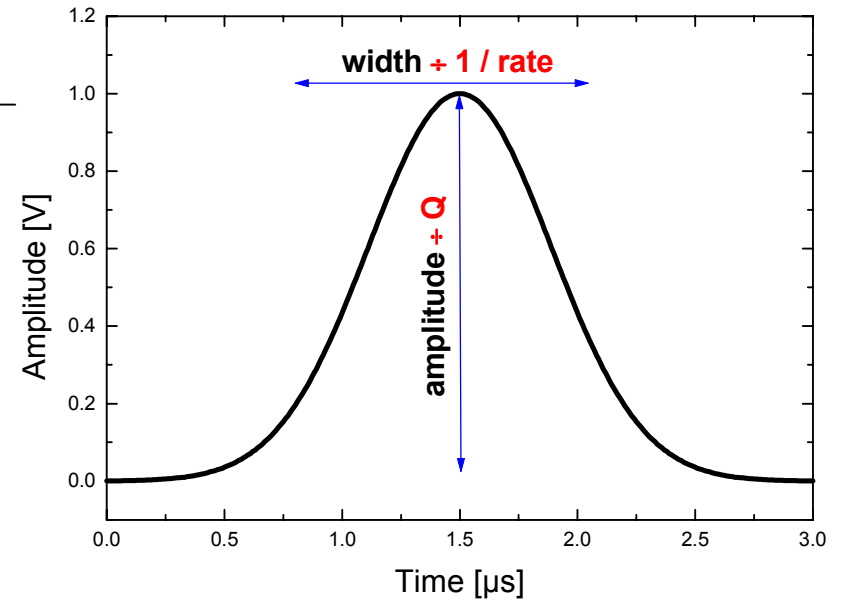
# Typical fluorescence EXAFS measurement geometry



# Resolution vs Rate

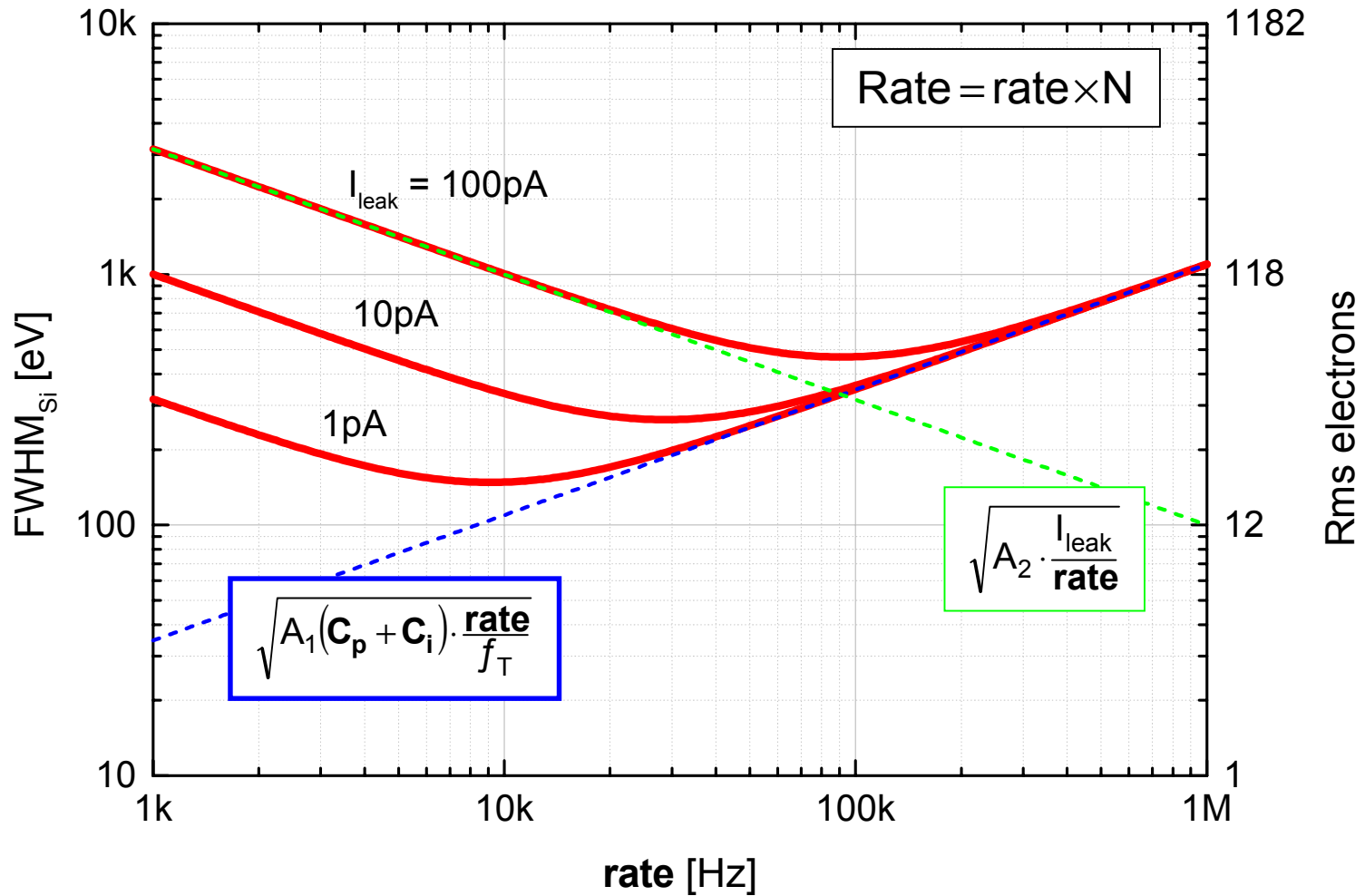


$$\text{rate} = \frac{\text{Rate}}{N} \quad (N = \text{number of pixels})$$

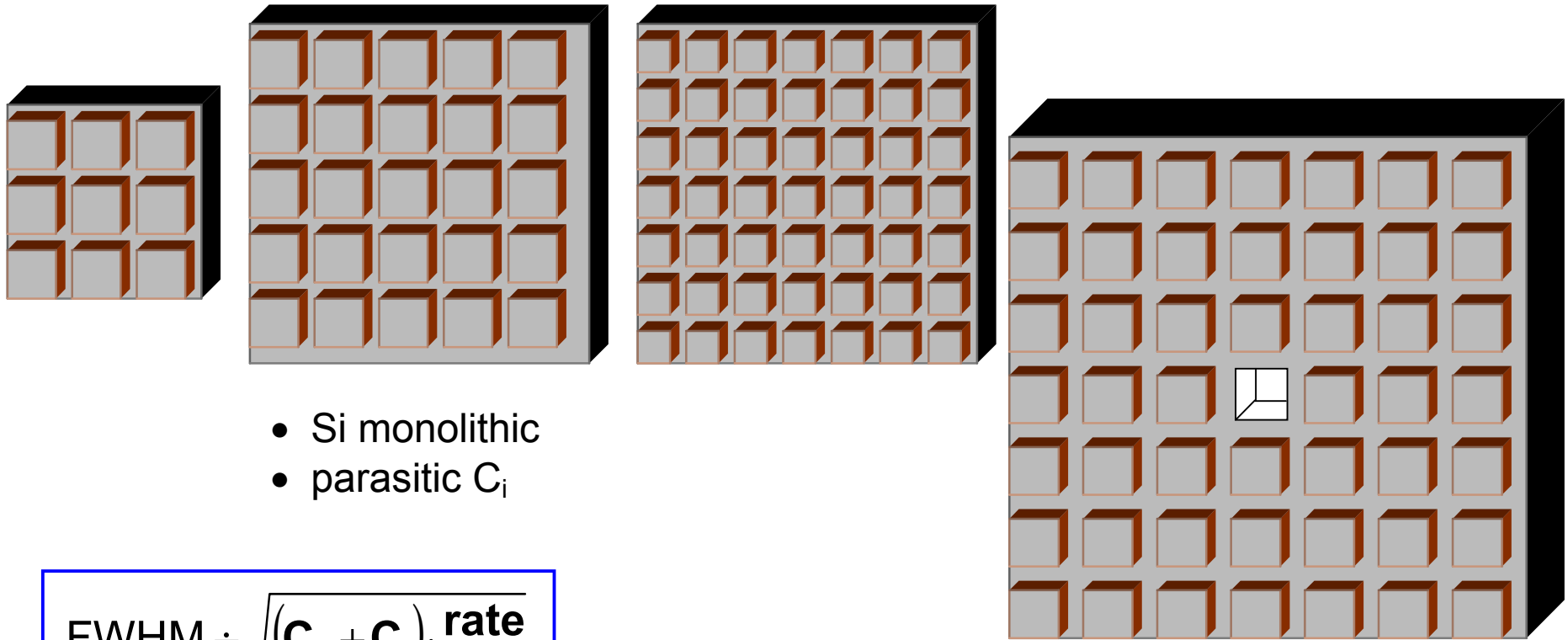


$$\text{FWHM} = \sqrt{A_1(C_p + C_i) \cdot \frac{\text{rate}}{f_T} + A_2 \cdot \frac{I_{leak}}{\text{rate}}}$$

# Resolution vs rate



# Optimum segmentation



- Si monolithic
- parasitic  $C_i$

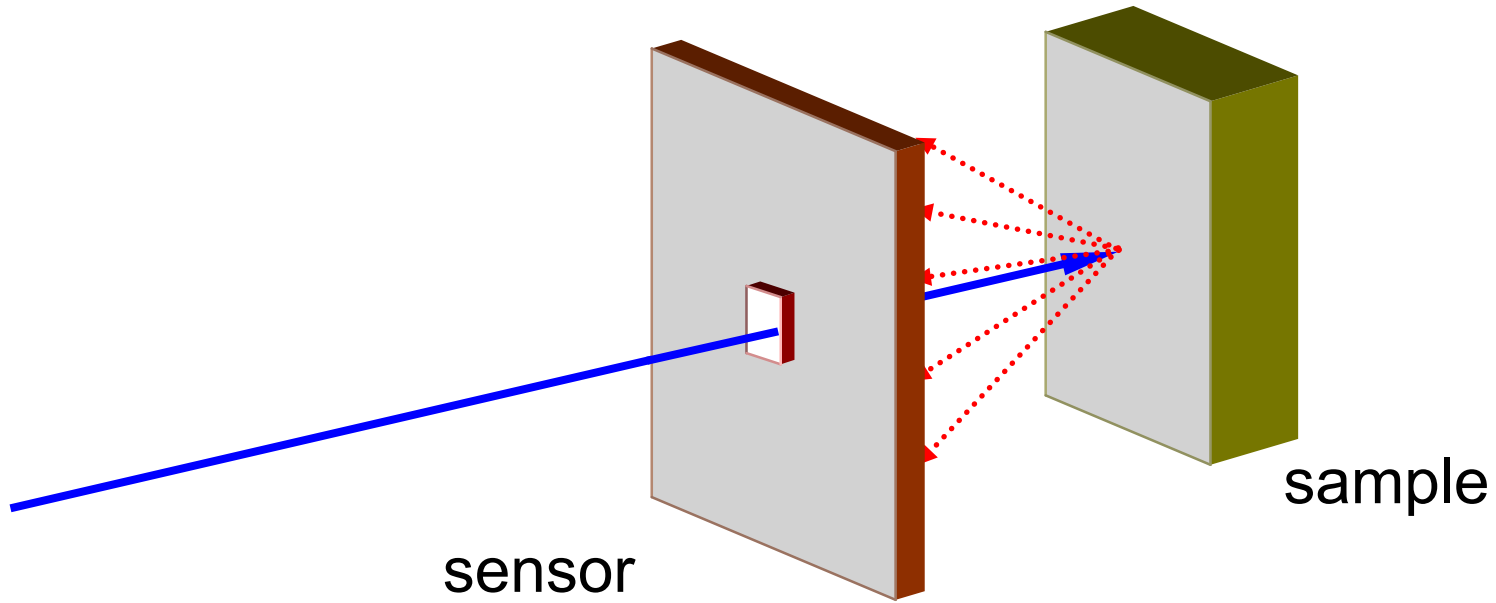
$$\text{FWHM} \div \sqrt{(C_p + C_i) \cdot \frac{\text{rate}}{f_T}}$$

- front-end electronics (channel count, power)
- fringe capacitance (component of  $C_p$ )
- parasitic  $C_i$
- charge sharing ( $\approx 20\mu\text{m}/\text{side}$ ) and trapping (gap/side)

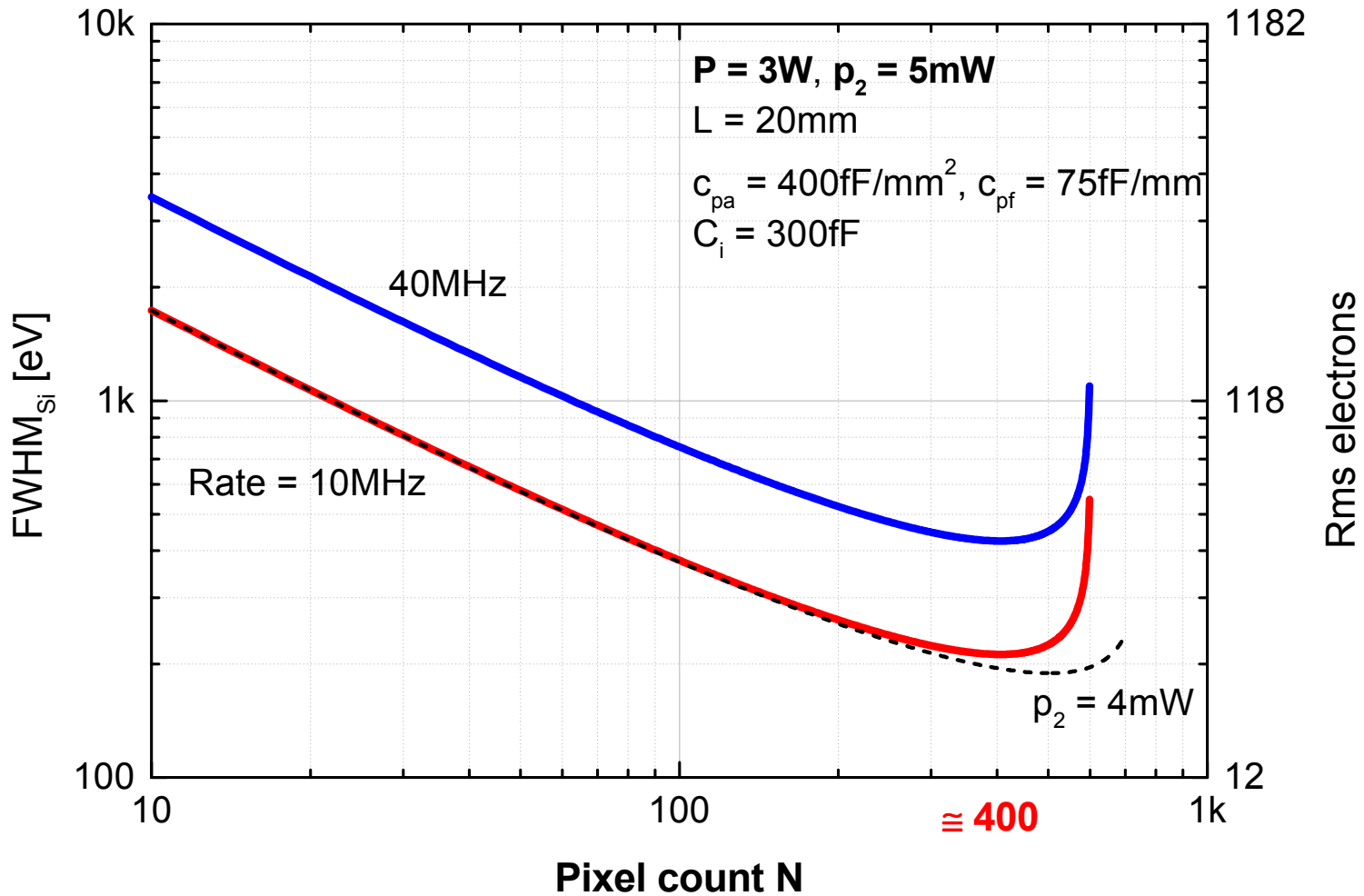
2<sup>nd</sup> order,  
empirical approach



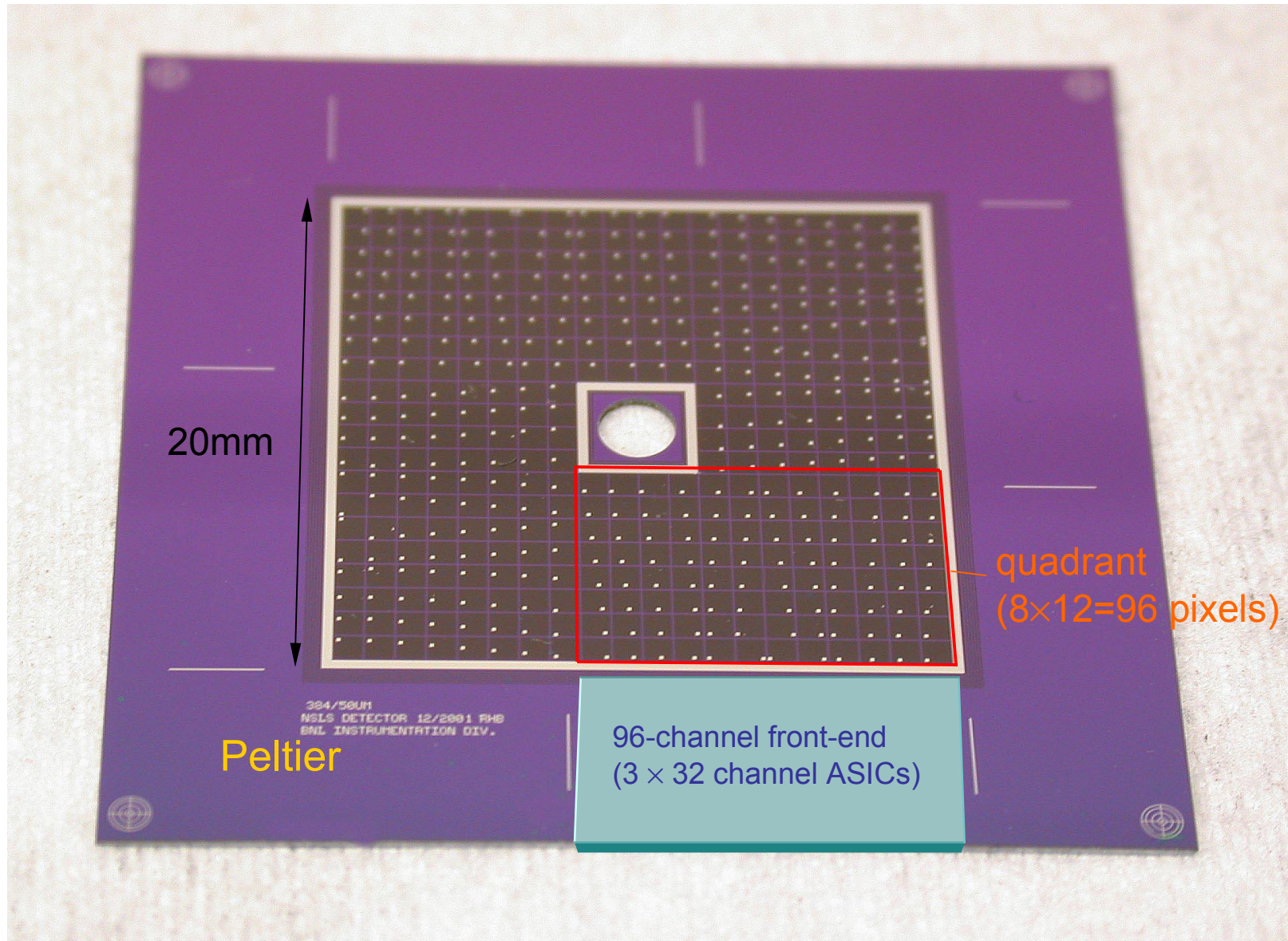
# Beam through



$$\text{FWHM} \div \sqrt{\left[ c_{\text{pa}} \left( \frac{L}{\sqrt{N}} \right)^2 + c_{\text{pf}} \frac{L}{\sqrt{N}} + C_i \right]} \cdot \frac{\text{Rate}}{N} \cdot \frac{1}{\sqrt{\frac{P}{N} - p_2}}$$

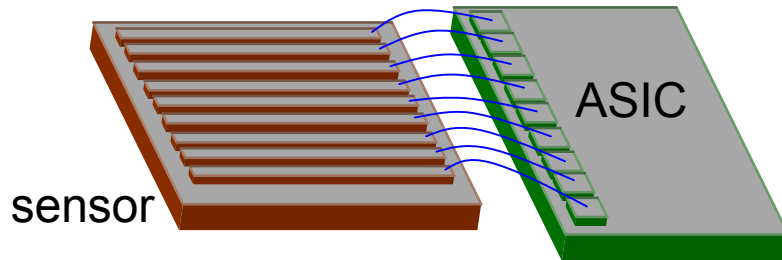




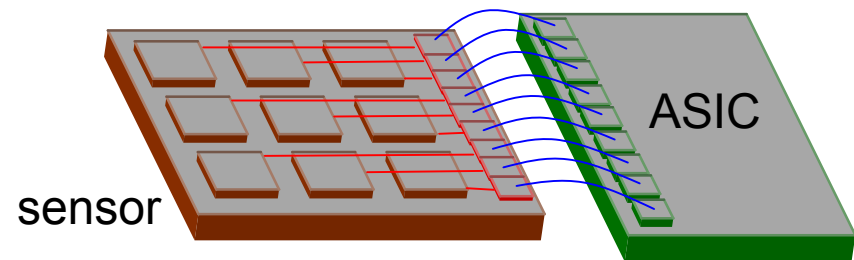


Si n-type high resistivity wafer 250 $\mu$ m thick,  
N = 384 p<sup>+</sup>  $\approx$ 1mm $\times$ 1mm pixels,  
gaps 10 $\mu$ m, 30 $\mu$ m, 50 $\mu$ m

# Interconnecting pixel to front-end electronics



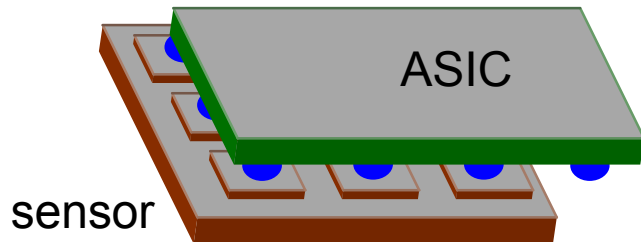
- + interconnect parasitic
- + bond length
- fringe capacitance
- charge sharing and trapping



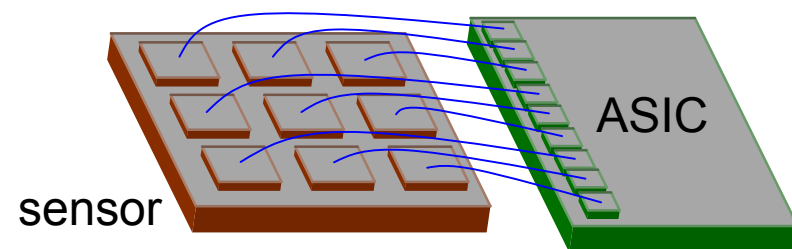
- + bond length
- interconnect parasitic
- dielectric losses

6mm×10μm, Si<sub>3</sub>N<sub>4</sub> ( $\epsilon_r=6.5, \tan(\delta)=0.001$ ), 3μm,  $C_i \approx 1.2\text{pF}$

$$\delta\text{FWHM}_{\text{loss}} = 8.5/q \cdot \sqrt{2kT C_p \tan(\delta)} \approx 170\text{eV}$$

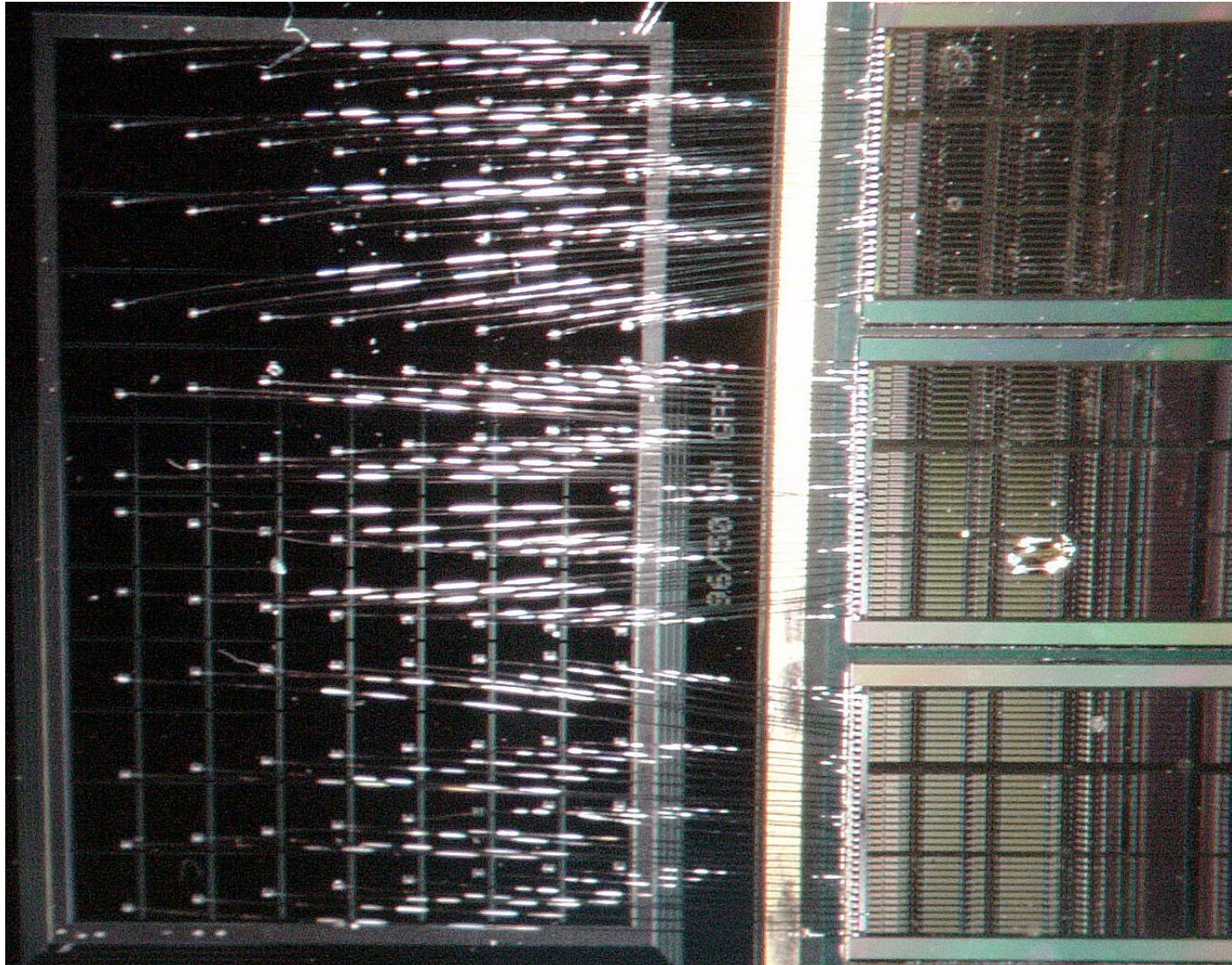


- + interconnect parasitic
- constraint on ASIC area and layout
- fluorescence from Pb (Sn/Pb/Ag)
- illumination from segmented side



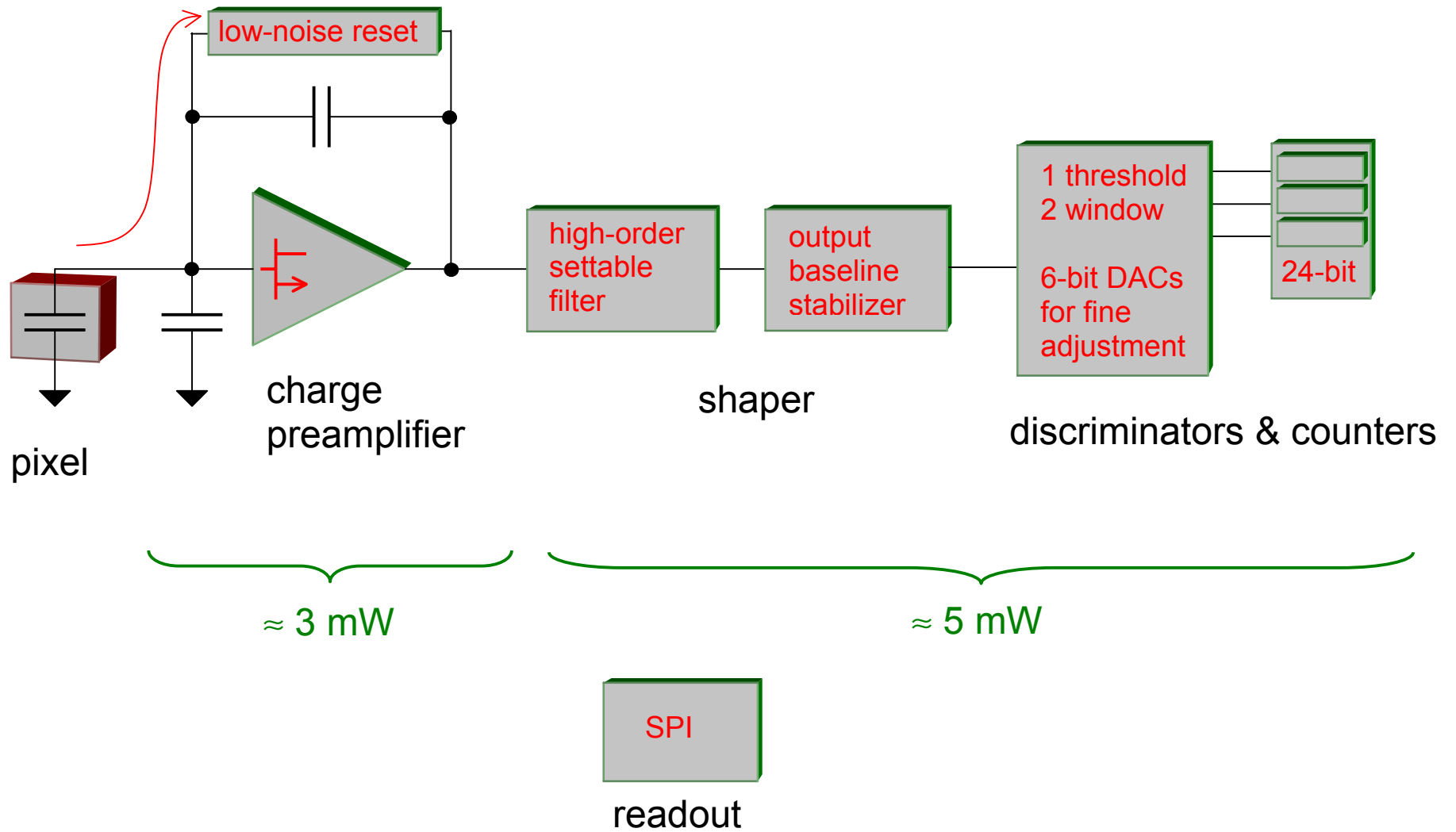
- + dielectric losses
- ± interconnect parasitic
- bond length

# Detector-ASIC photo



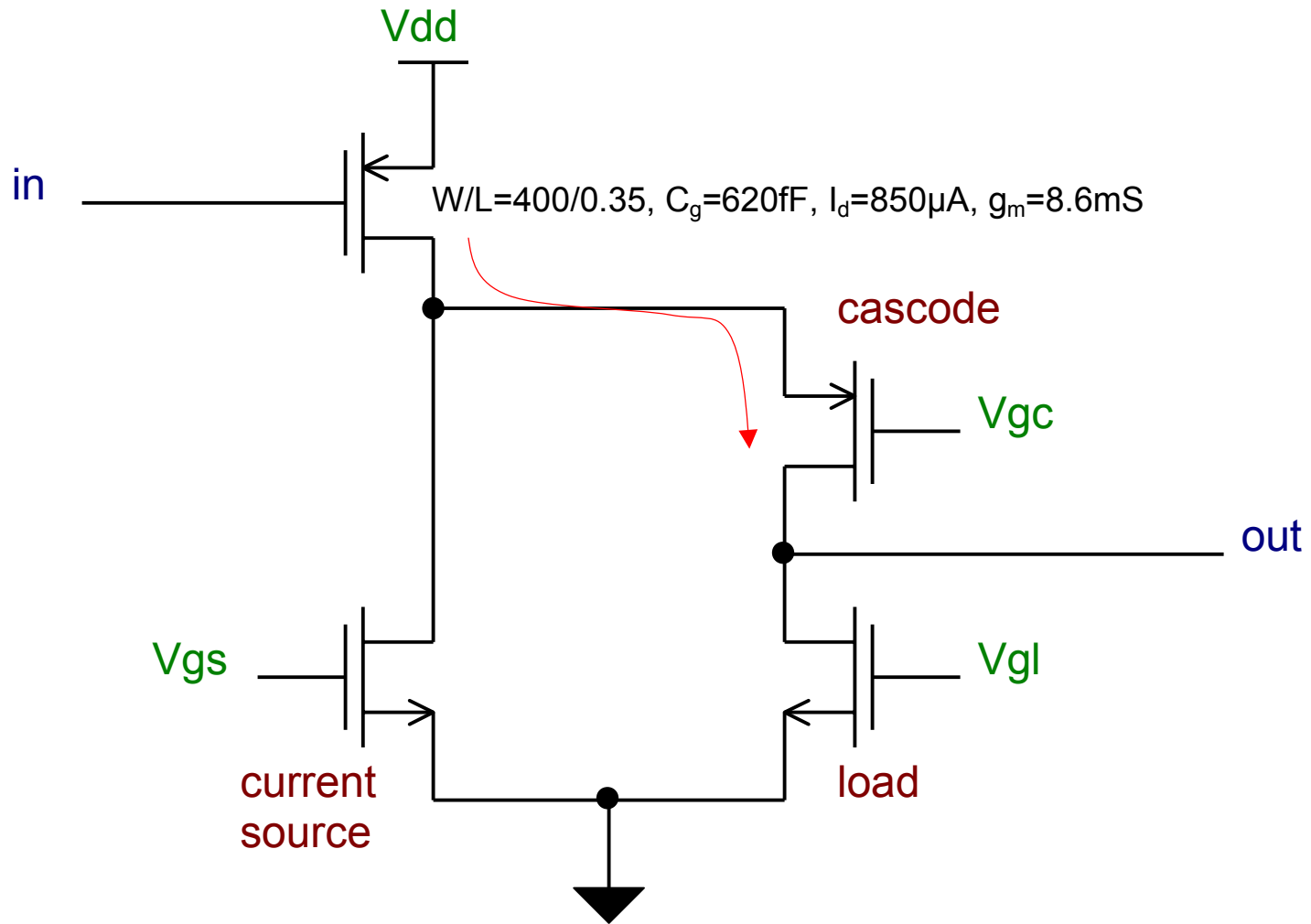
*quadrant*

# Front-end channel overview



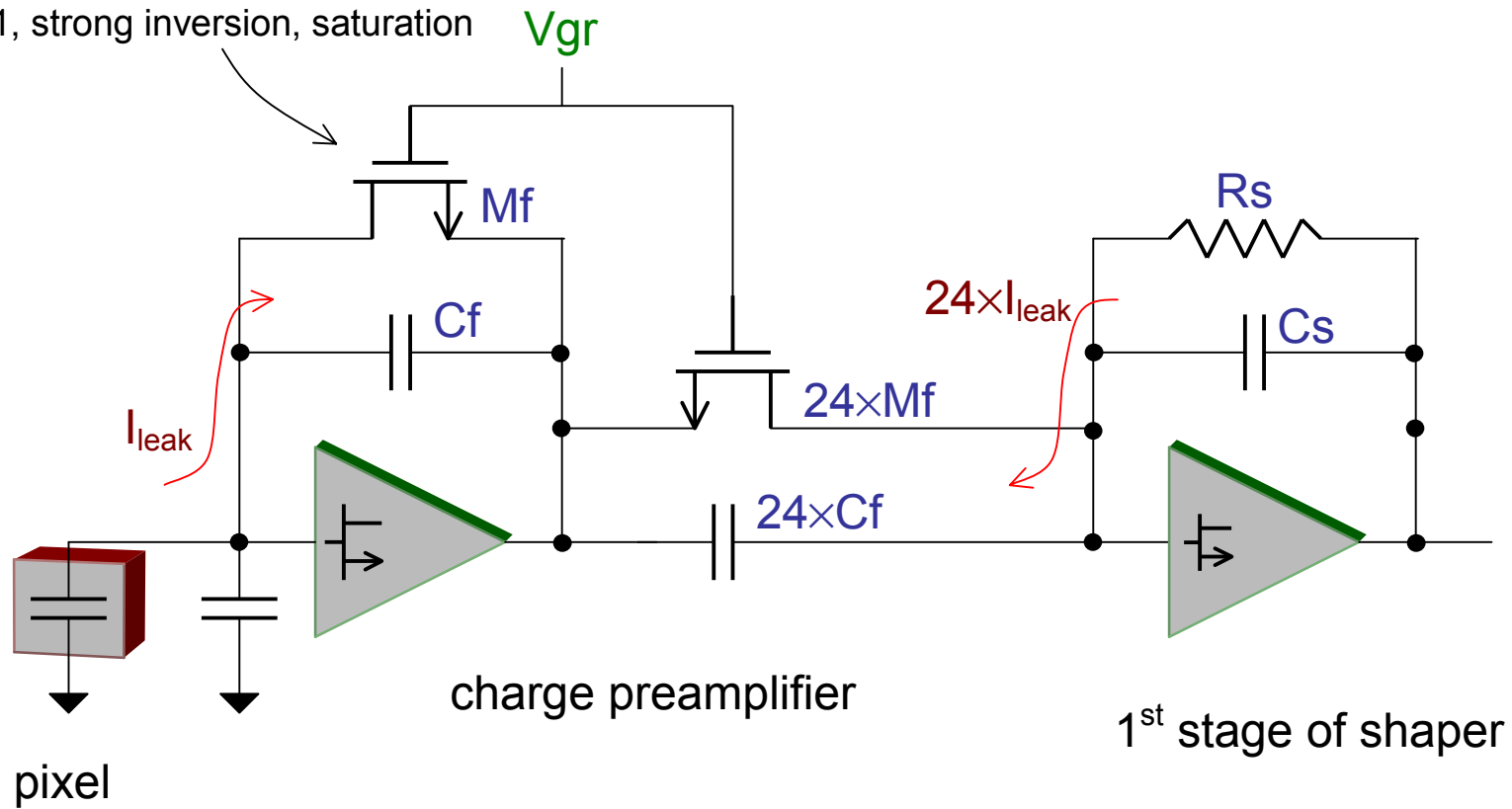
Technology CMOS 0.35 $\mu\text{m}$  3.3V 2P4M

# Charge preamplifier



# Continuous reset

$L/W \gg 1$ , strong inversion, saturation

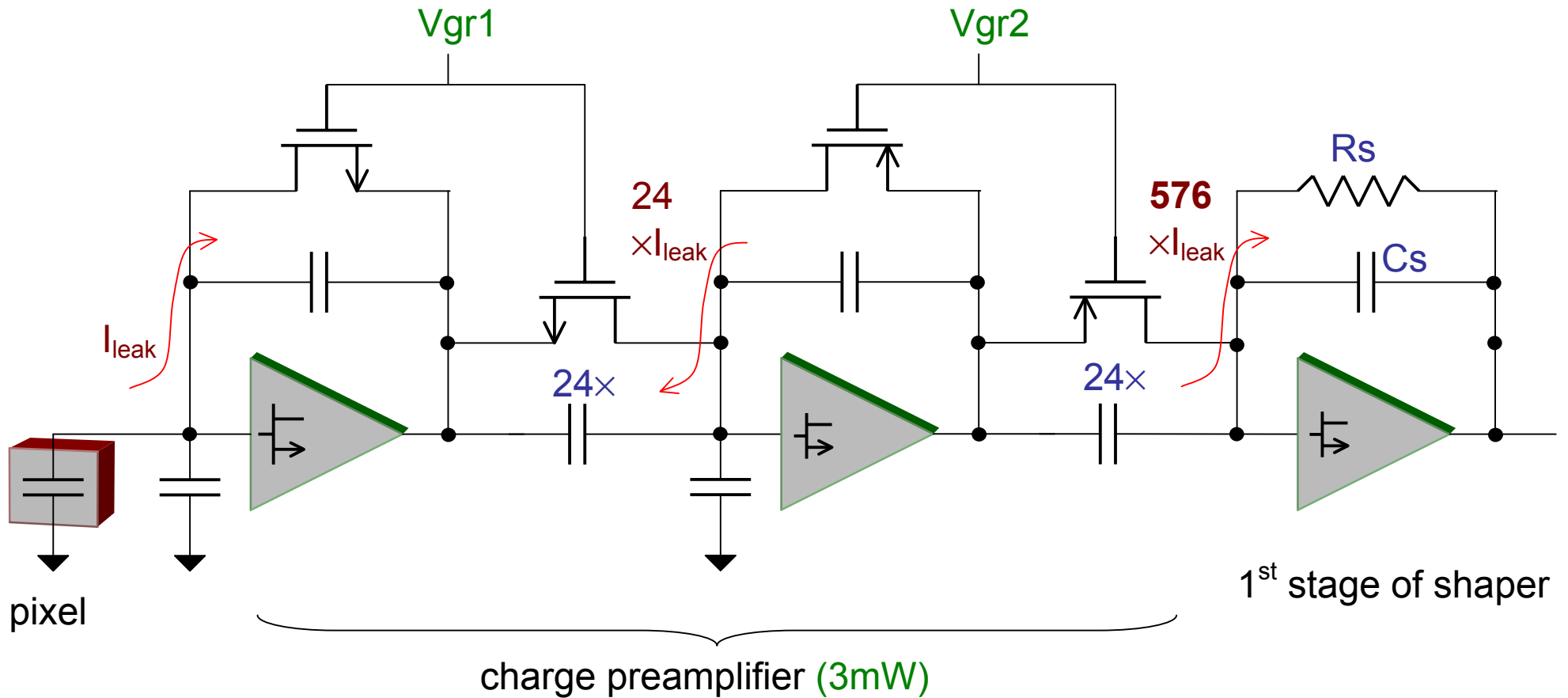


- current gain of 24
- fully linear
- self-adapts to leakage current
- minimum noise contribution

# Continuous reset – dual stage

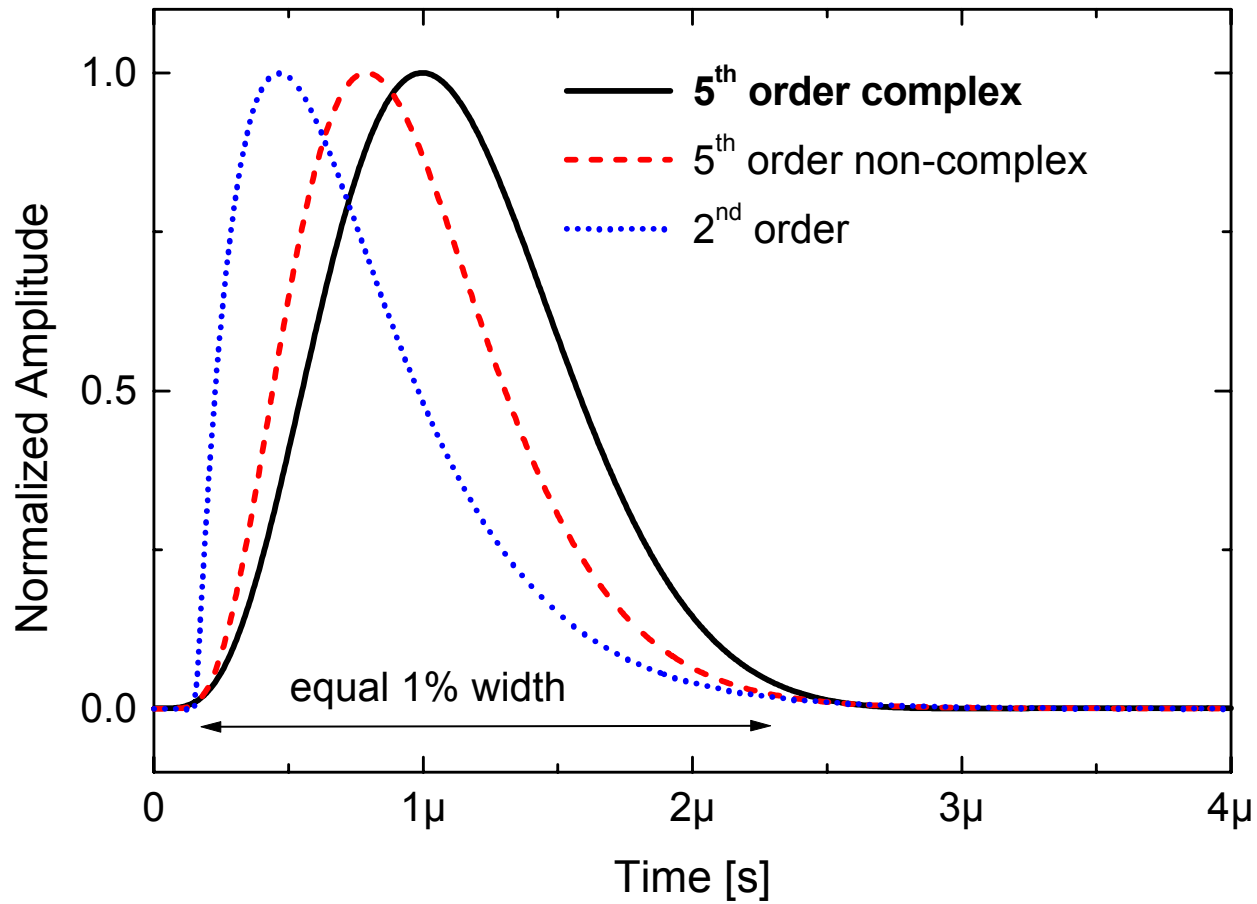
$$\frac{2kT}{R_s} \frac{1}{24^2} \equiv q \cdot I_{eq}$$

$$R_s \approx 200k\Omega \rightarrow I_{eq} \approx 500pA$$



$$R_s \approx 200k\Omega \rightarrow I_{eq} \approx 0.75pA$$

# Shaping

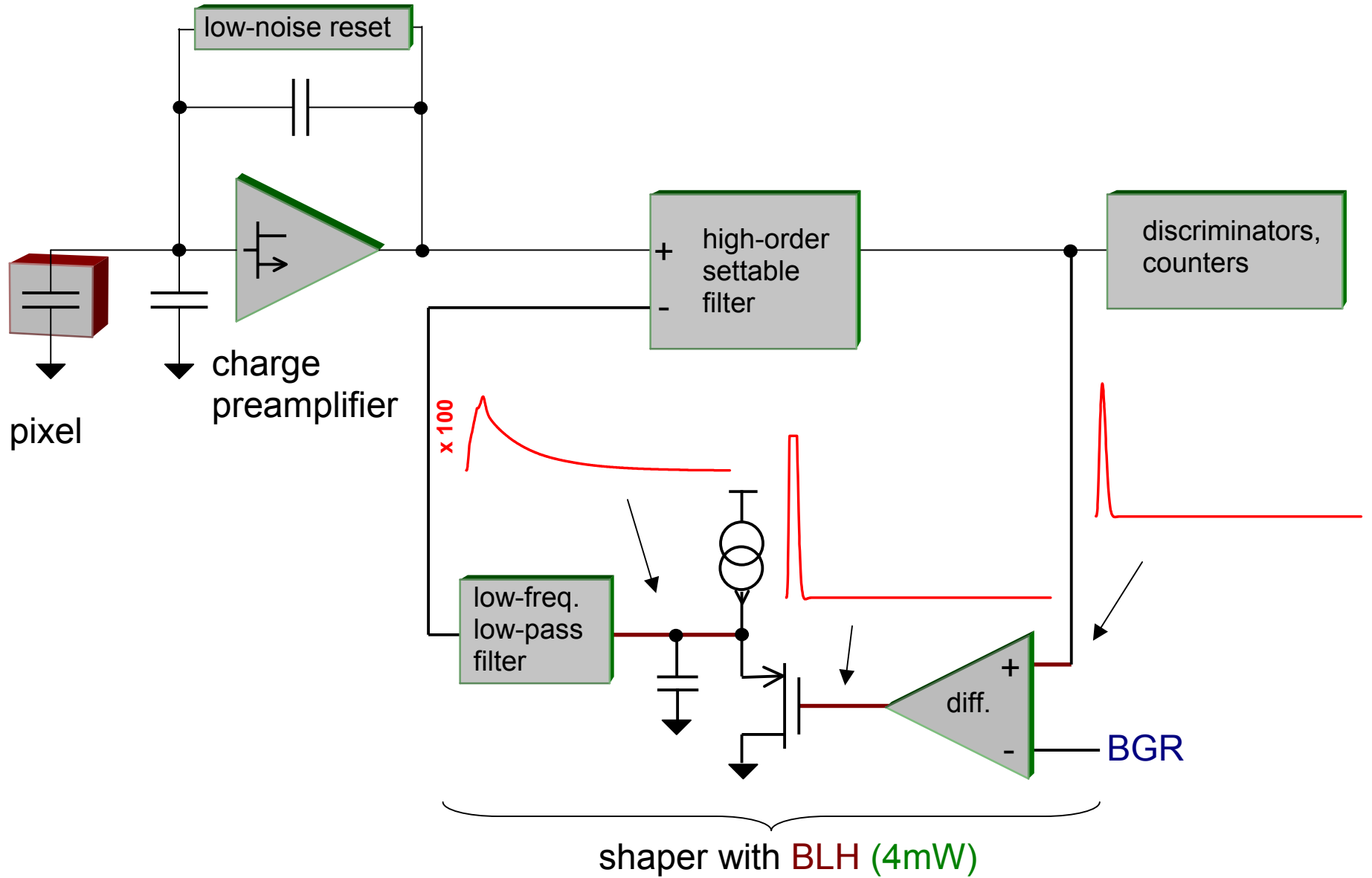


$$\text{FWHM} = \sqrt{\alpha \cdot A_1 (C_p + C_i) \cdot \frac{\text{rate}}{f_T}}$$

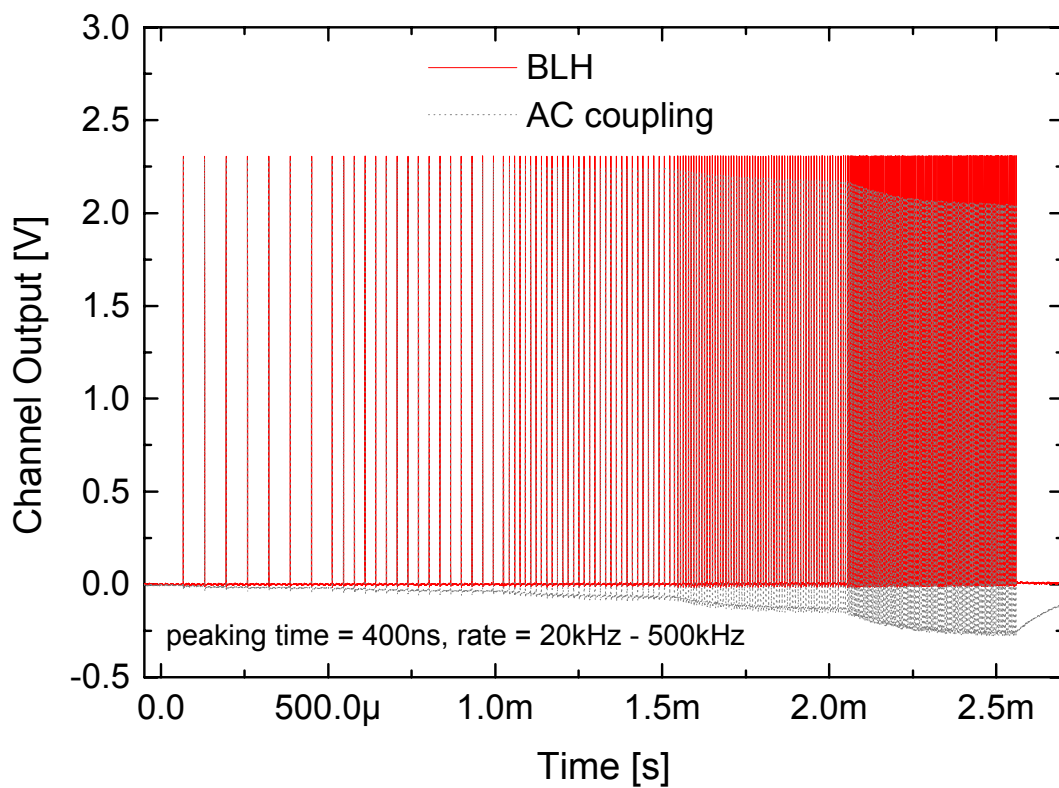
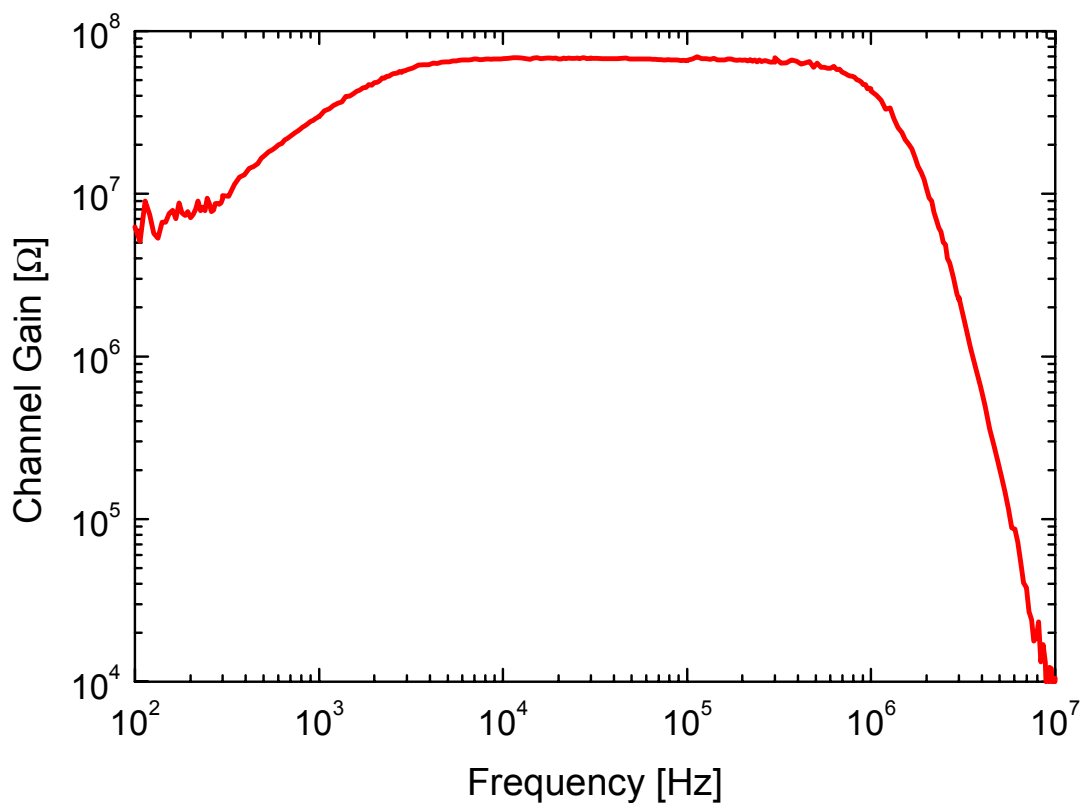
	$\alpha$
5 <sup>th</sup> cpx	5.5
5 <sup>th</sup>	6.8
2 <sup>nd</sup>	14.5



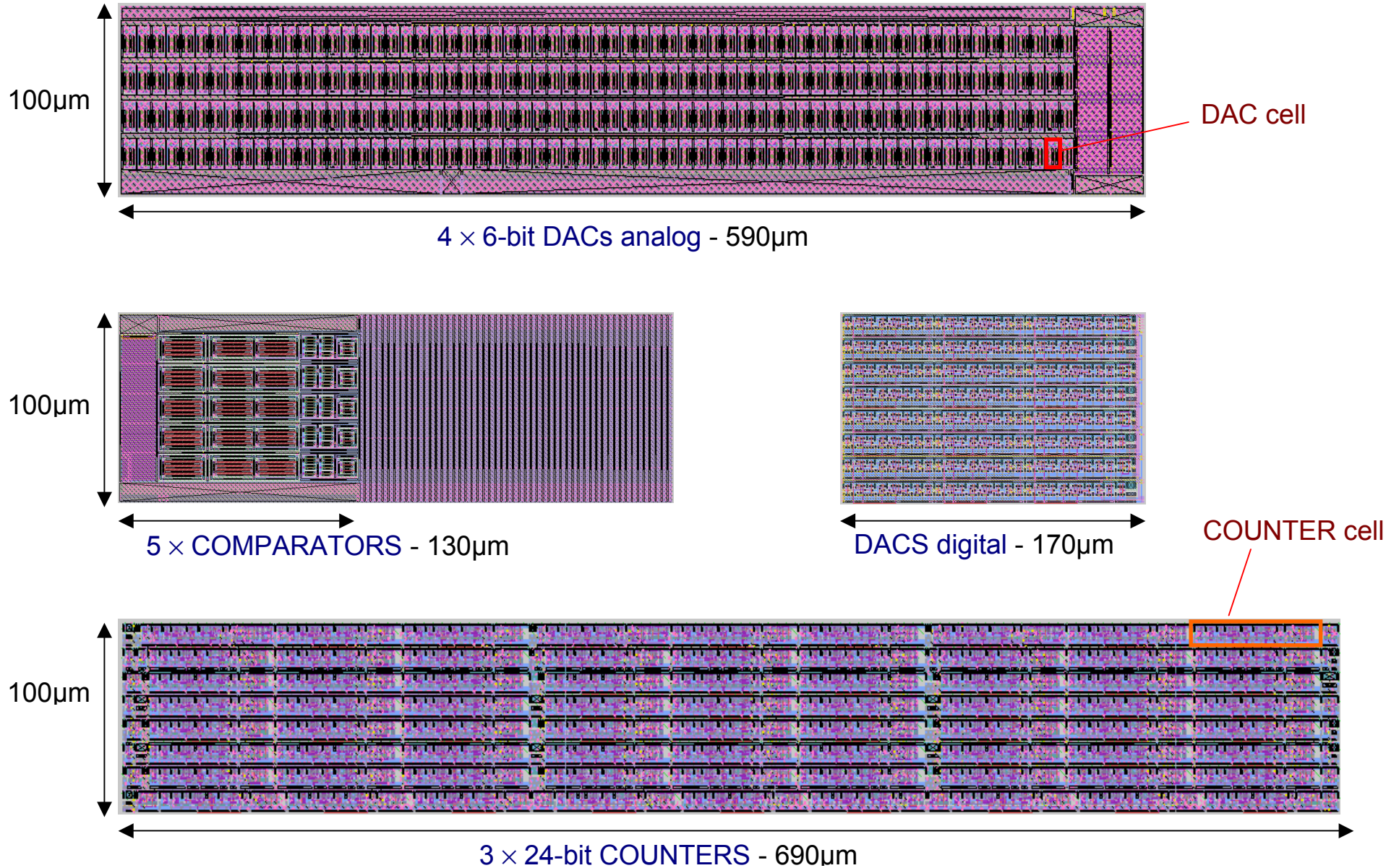
# Baseline stabilization



# Baseline stabilization (BLH)



# Layout (CMOS 3.3V 2P4M 0.35 $\mu$ m)



# ASIC overview

CMOS 0.35 $\mu$ m 3.3V 2P4M  
180,000 MOSFETs, size 3.6  $\times$  6.3 mm<sup>2</sup>  
8mW / channel

- 32 readout channels
  - self adaptable continuous **reset**
  - high order **shaper**
    - settable peaking time (0.5 $\mu$ s, 1 $\mu$ s, 2 $\mu$ s, 4 $\mu$ s)
    - settable gain (750mV/fC, 1500mV/fC)
    - band-gap referenced output baseline
    - output baseline stabilization (BLH)
  - 1 threshold and 2 window **discriminators**
  - 4 $\times$  6-bit **DACs** for fine window adjustments
  - 3 $\times$  24-bit **counters**
  - test mode
  - analog output monitor
  - pixel leakage current monitor
- Serial Peripheral Interface (**SPI**)
  - global settings
  - monitors enabling
  - test enabling
  - channels masking
  - DACs setting
  - counters readout

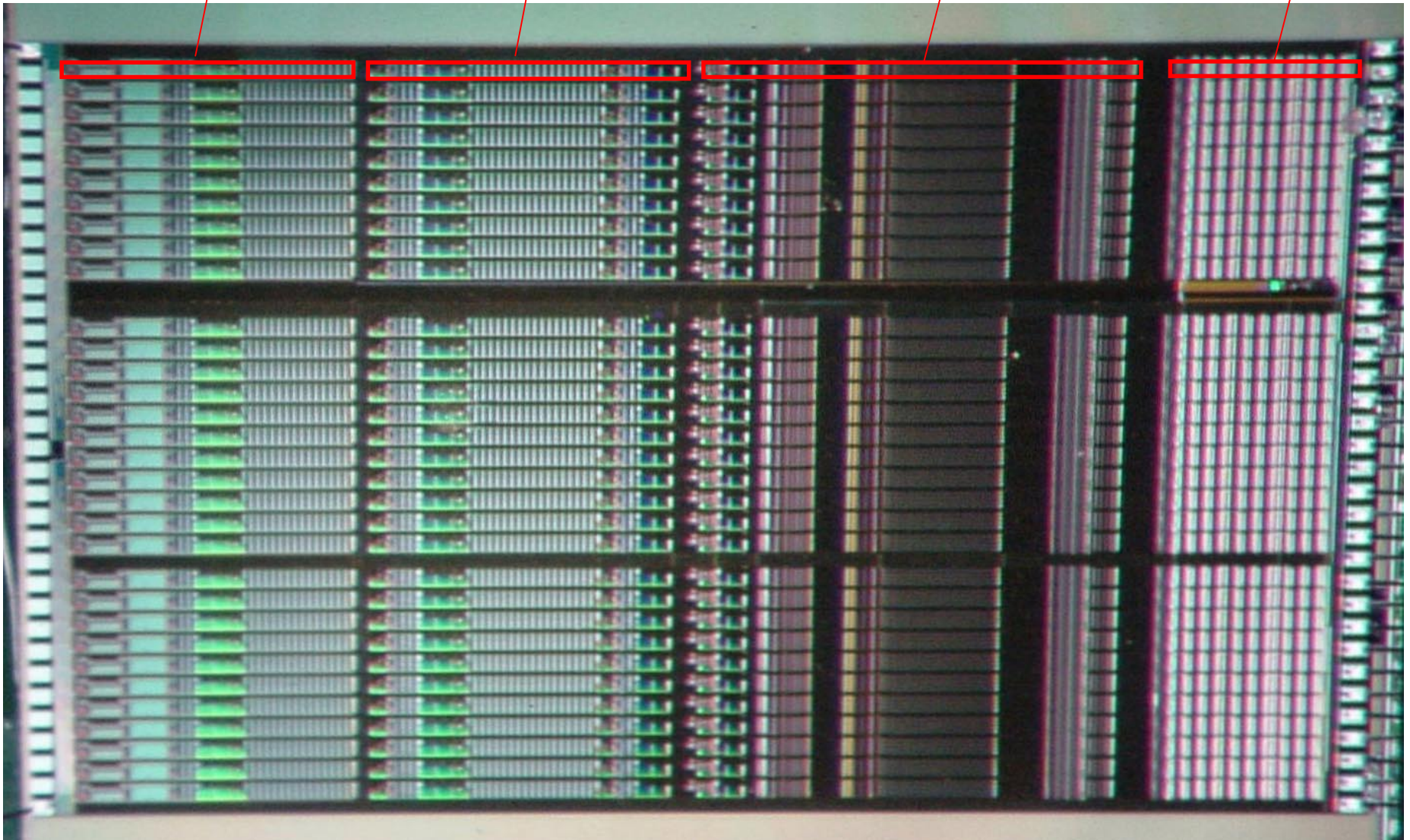
# ASIC photo

charge preamplifier

shaper with BLH

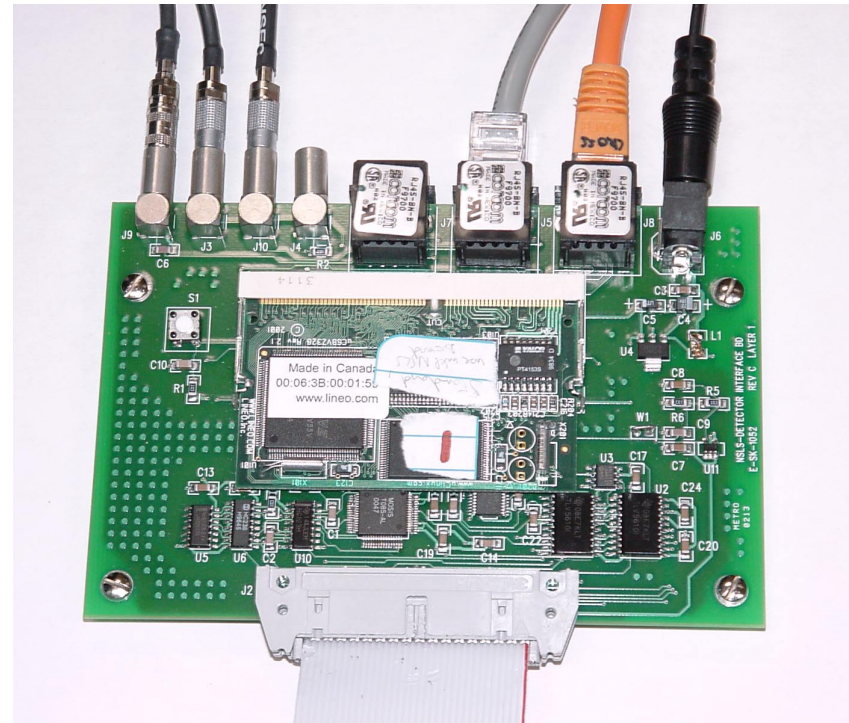
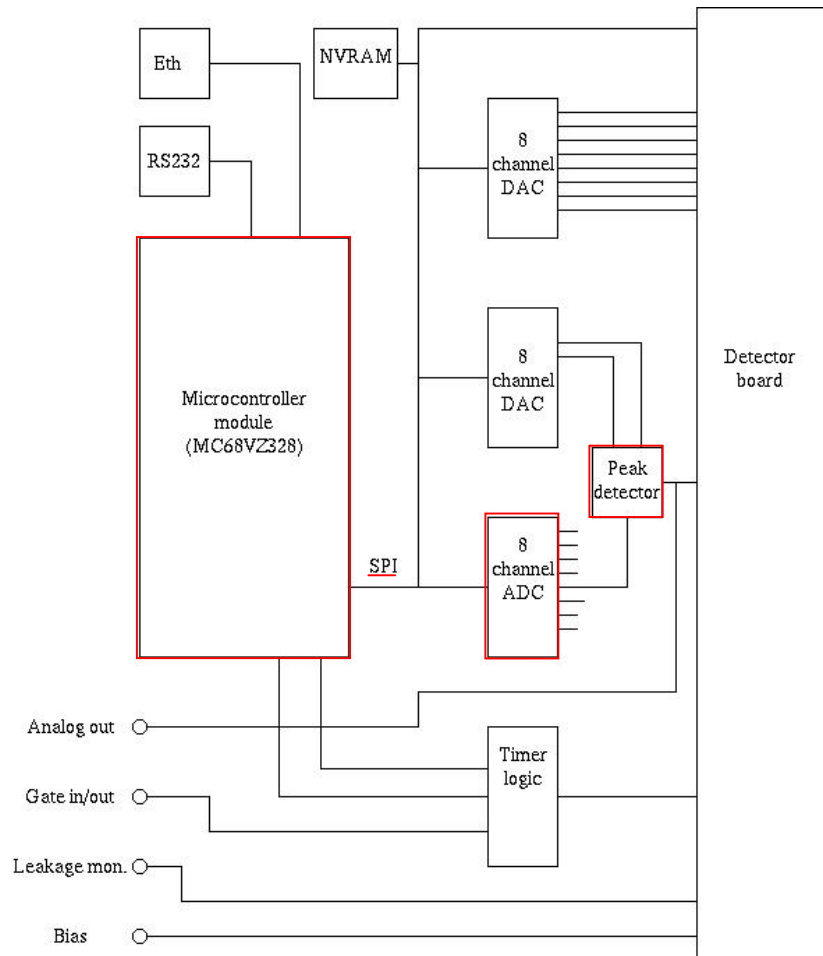
discriminators and DACs

counters

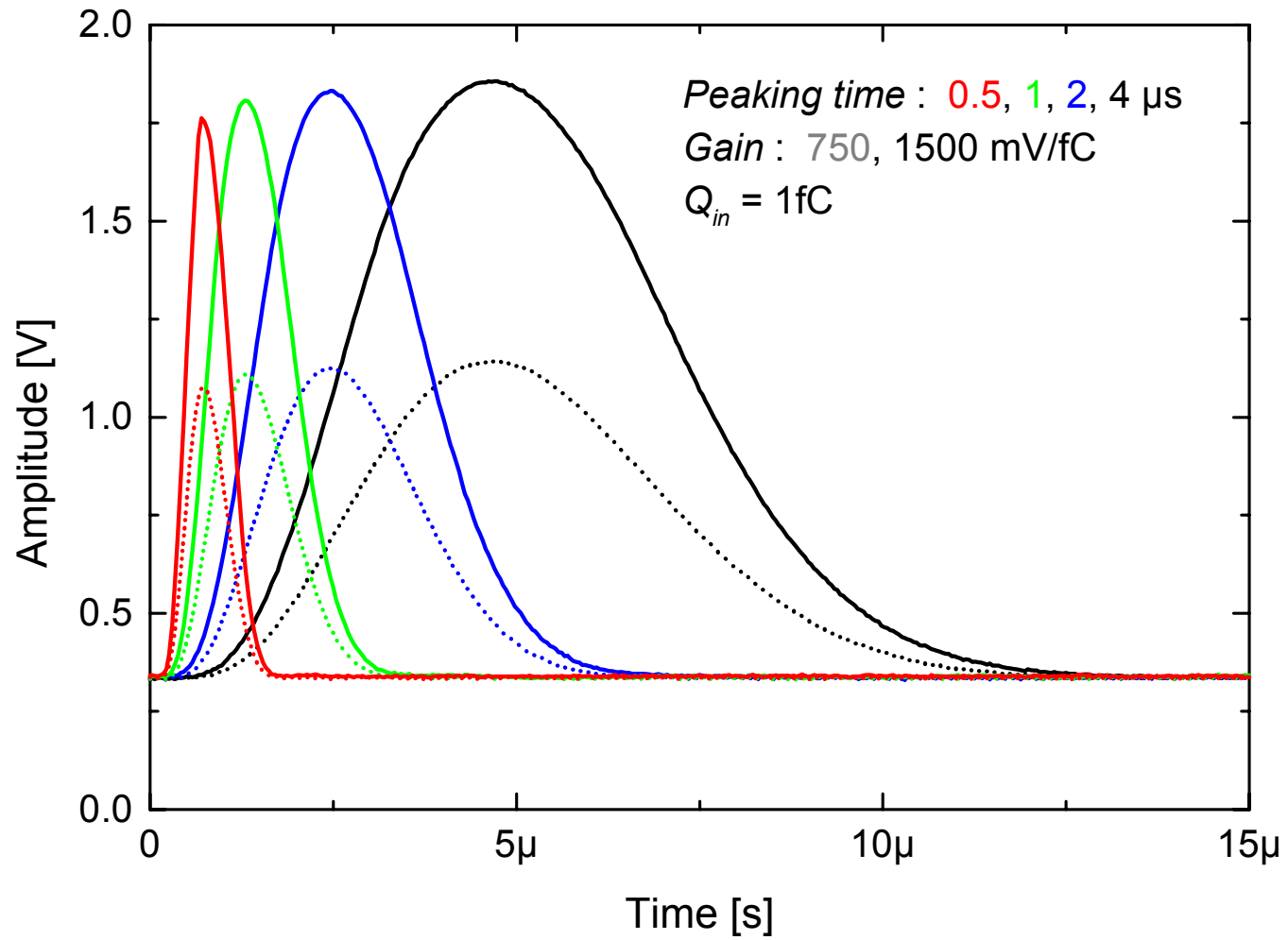


*32 channels,  $3.6 \times 6.3 \text{ mm}^2$*

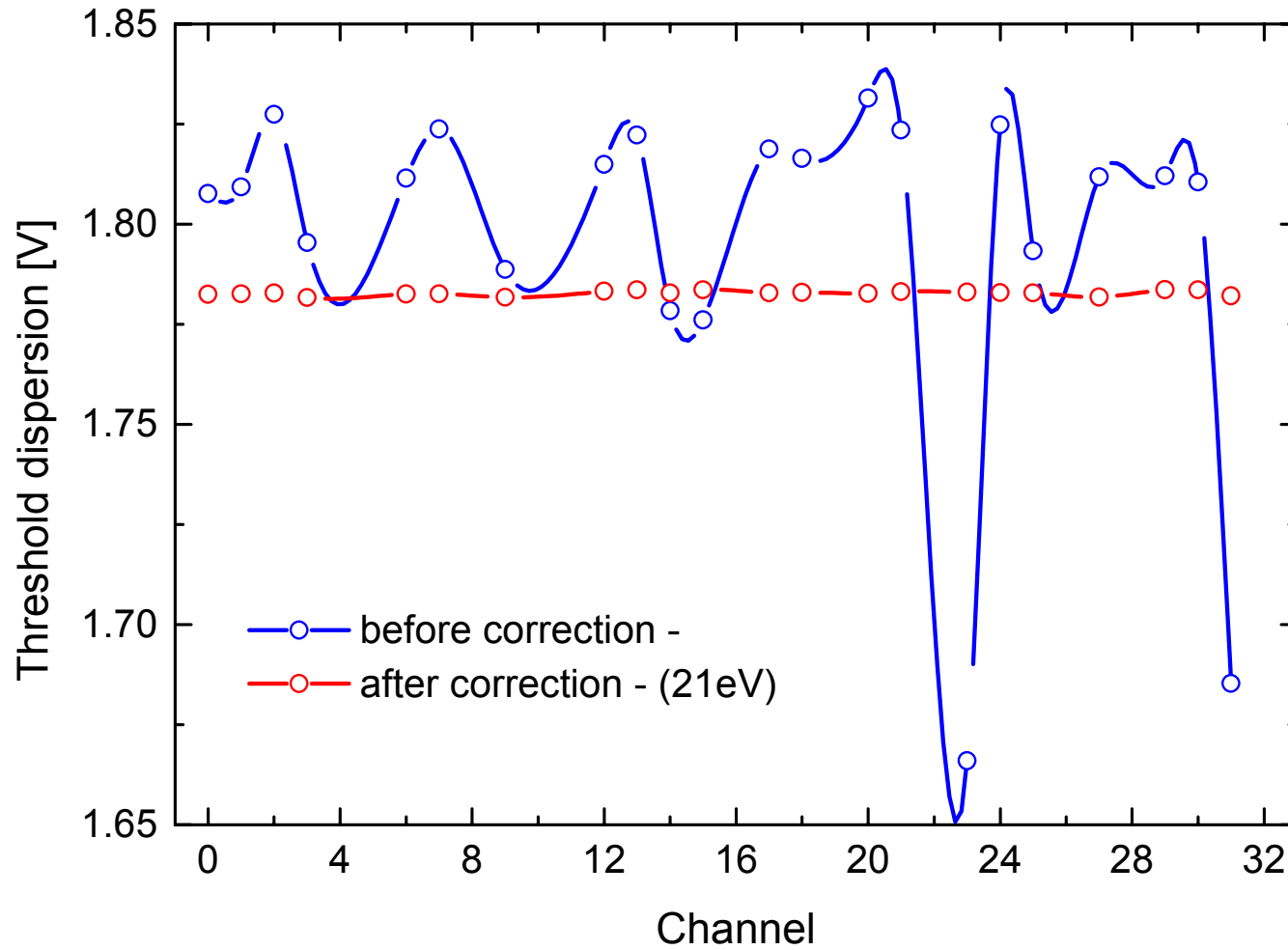
# Readout



# Experimental

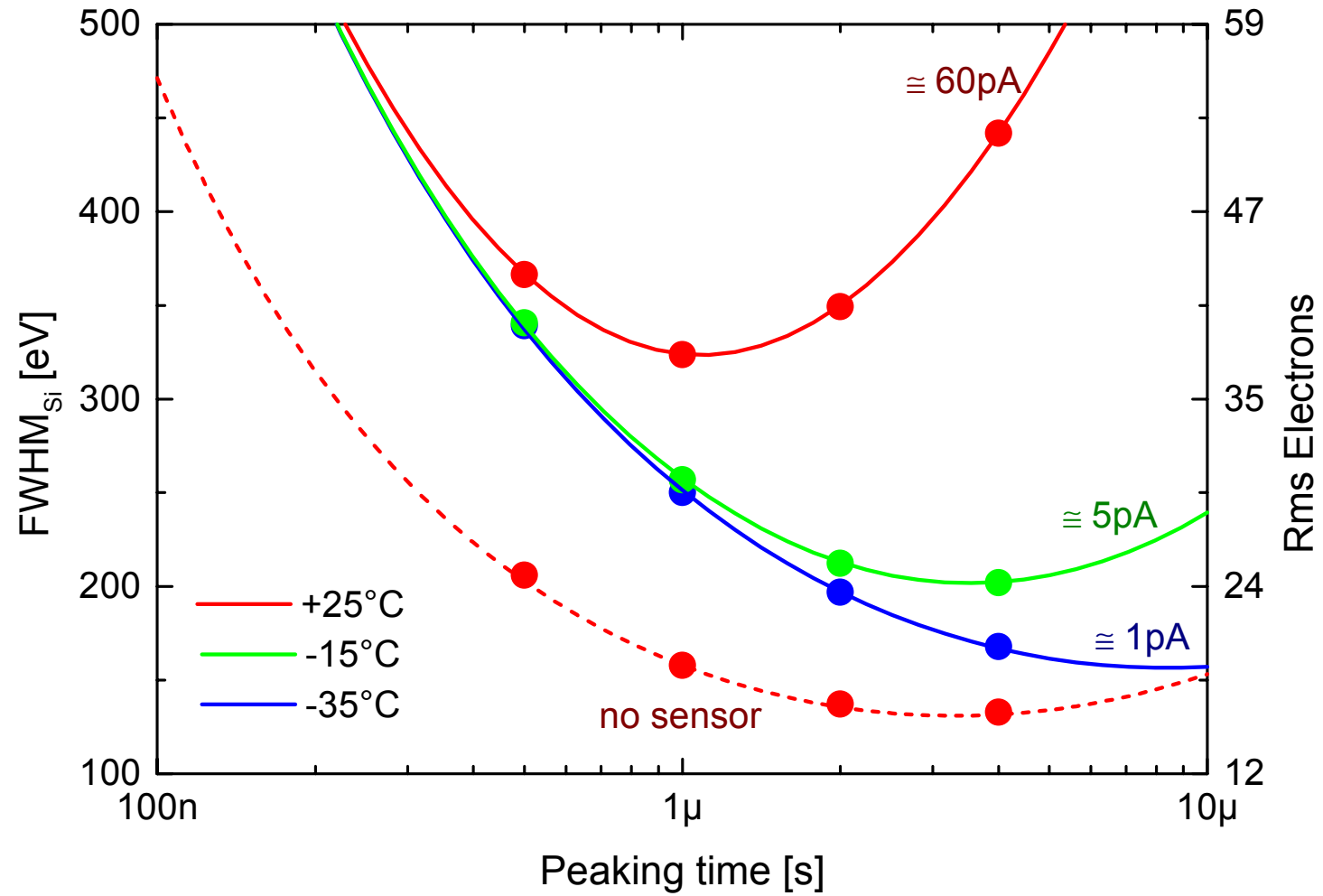


# Experimental

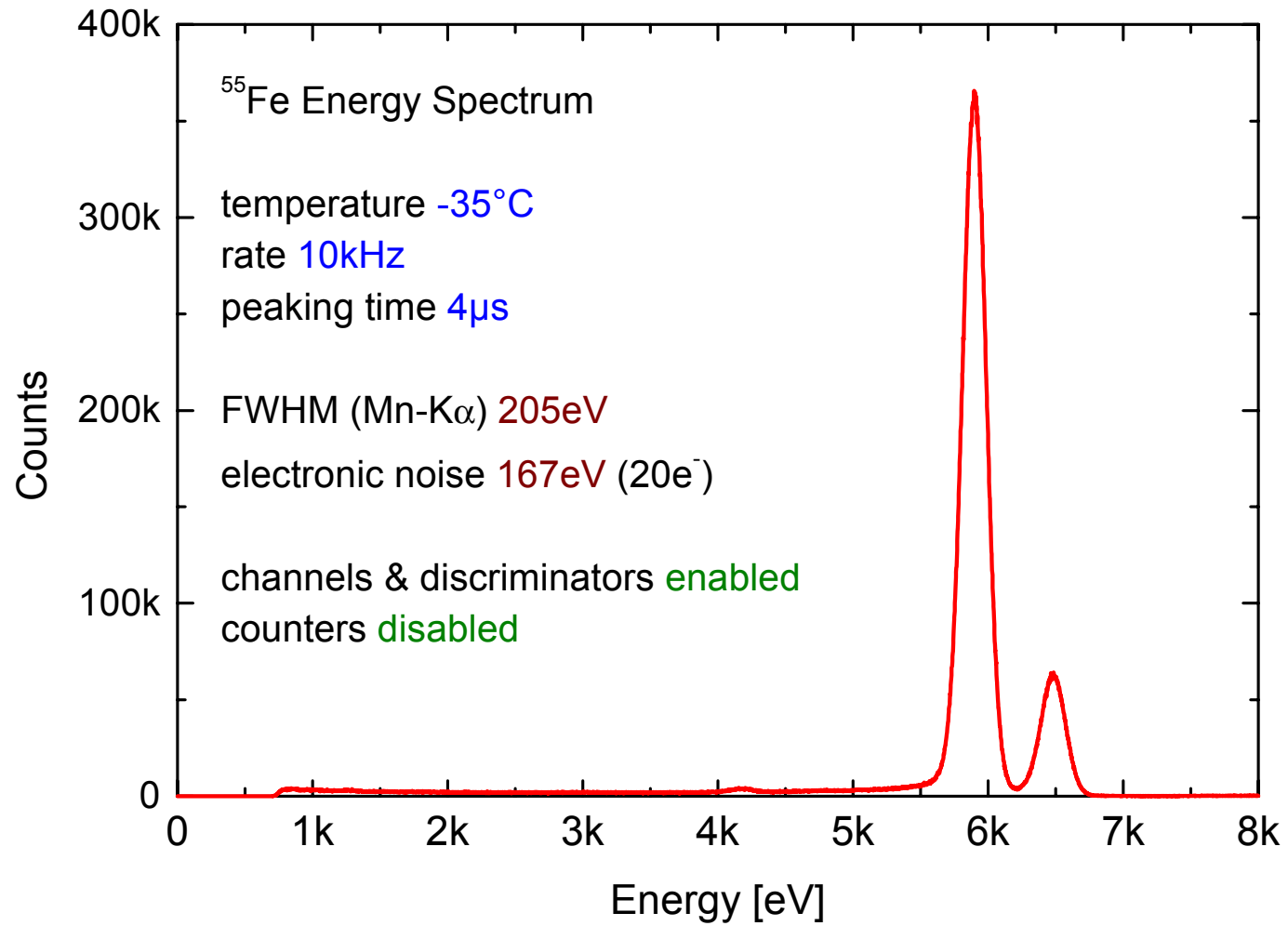




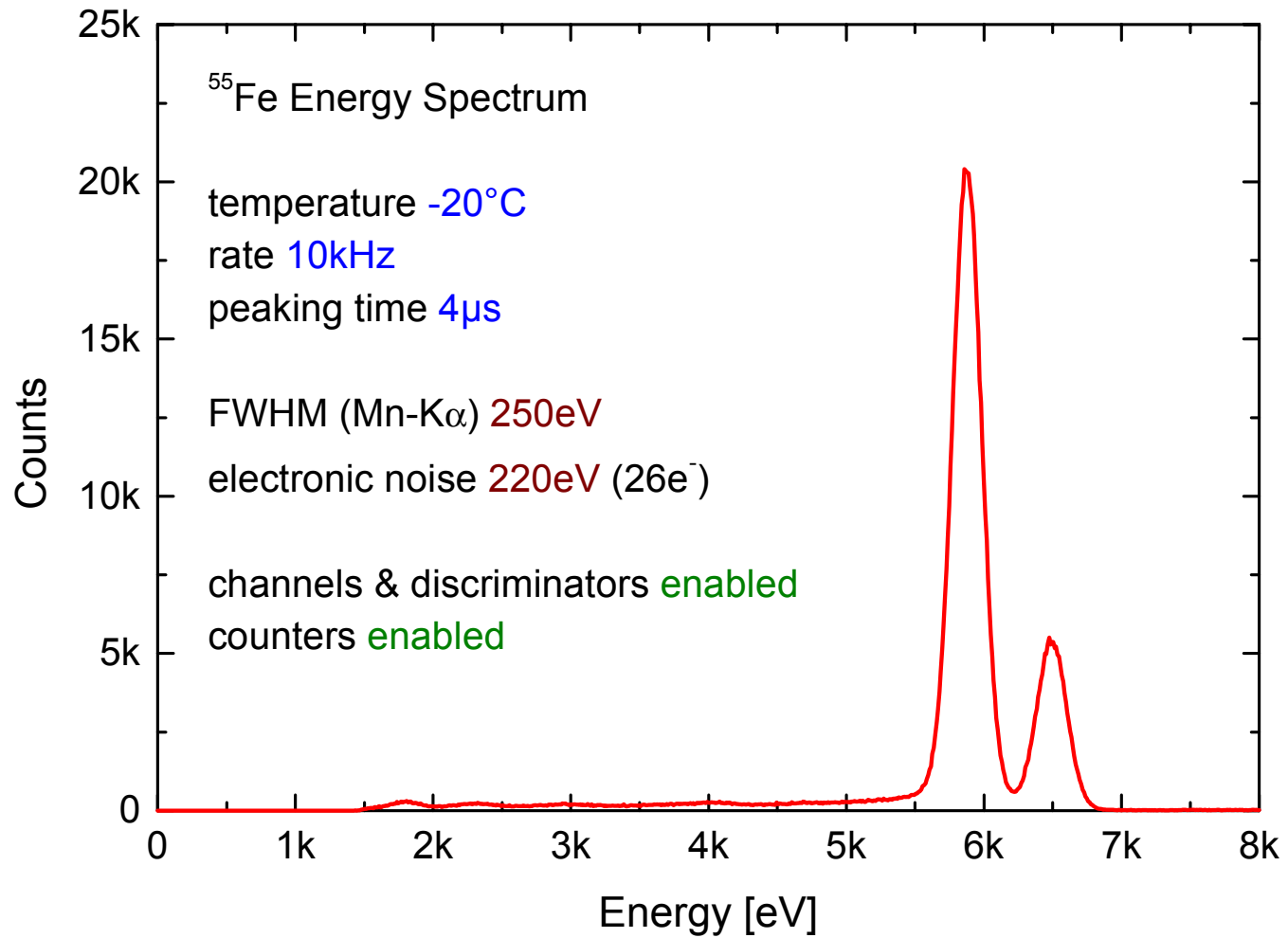
# Experimental



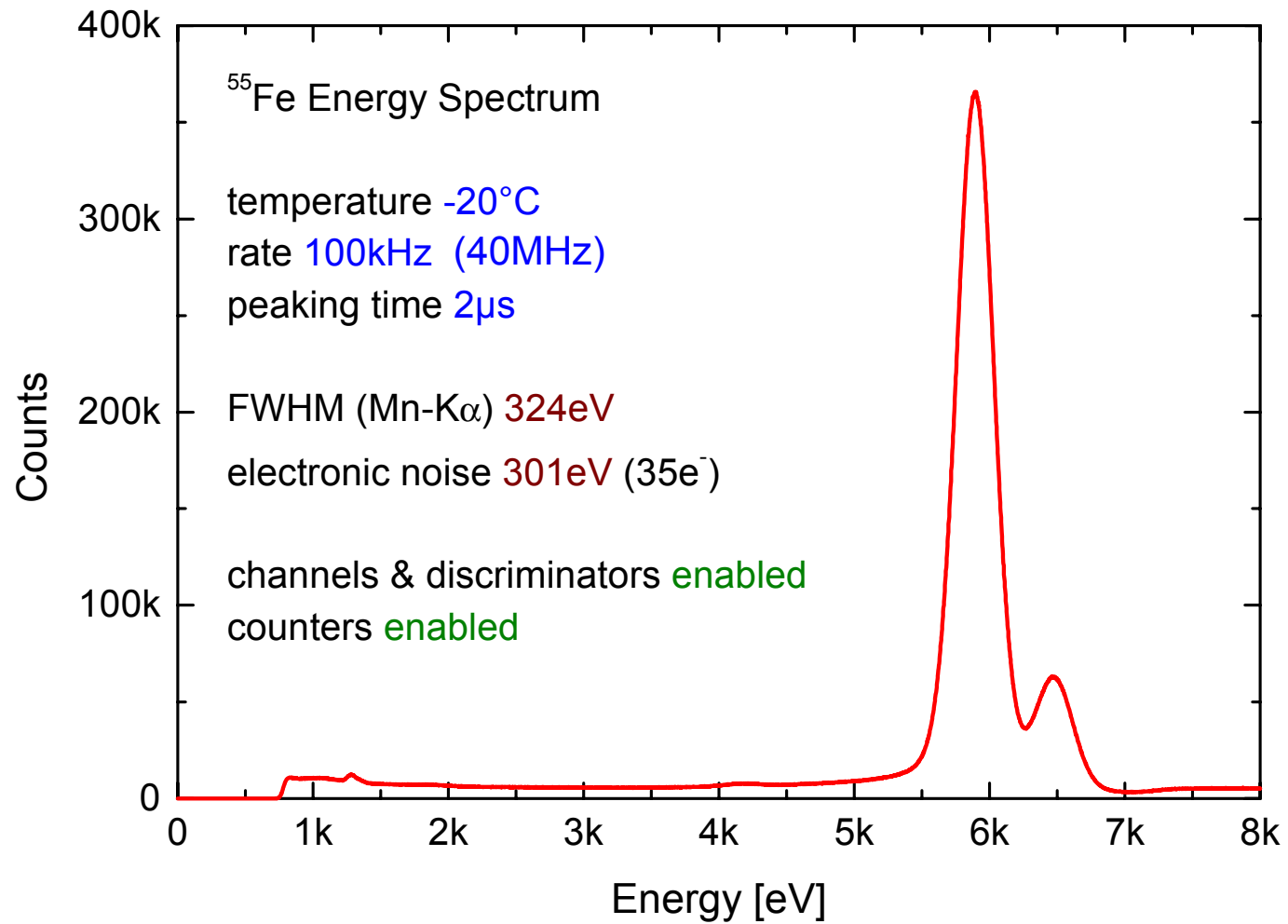
# Experimental



# Experimental



# Experimental



# Readout interface

The screenshot displays a Linux desktop environment with several application windows open:

- Konsole:** Shows terminal output for the `NSLS ASIC1 detector` application. The output includes system boot messages and a command prompt where the user has entered `ls /usr/doc/xvfb`.
- ASIC Operation controls:** A window for configuring the ASIC. It features a **Gain** dropdown menu with options: 1.0V/uC (selected), 0.5 V/uC, and a `set EBLK` button. Below this is a **Shaping time** dropdown menu with options: 0.5 us (selected), 1.0 us, 2.0 us, and 4.0 us. A **Display F.S.** field is set to 1000. A **Count** field is present. A **MCA window** button is at the bottom.
- Trim DAC Settings:** A window showing a 10x10 grid of DAC values. To the right of the grid are input fields for **Pixel** (67), **Thresh.** (0), **SCA 1** (0), and **SCA 2** (0). Below the grid are checkboxes for **Channel disable**, **Enable Cal. Input** (checked), **Enable Leakage Output**, and **Enable Analog Output**. Buttons for **Enable All Cal.**, **Disable All Cal.**, and **Global Reset** are also present.
- Set levels:** A window with sliders for **Thresh** (1024), **SCA 1 hi** (4095), **SCA 1 lo** (2299), **SCA 2 hi** (4095), and **SCA 2 lo** (1239). A **close** button is at the bottom.
- Global Settings:** A window with a table of DAC values for three chips. Below the table are dropdown menus for **Chip\_1**, **Chip\_2**, and **Chip\_3**, and a **Clear** button.

The **Global Settings** window contains the following table of DAC values:

Pixel	Thresh.	SCA 1	SCA 2
20	20	26	
63	63	57	
46	46	50	
48	48	56	
0	0	0	
0	0	0	
63	63	63	
61	61	41	
0	0	0	
63	63	63	
0	0	0	
62	62	56	
60	60	58	
41	41	47	
57	57	61	
0	0	0	
48	48	54	
63	63	53	
0	0	0	
63	63	63	
55	55	47	
21	21	48	
22	0	0	0
23	63	63	63
24	0	0	0
25	48	55	43
26	0	0	0
27	52	63	56
28	0	0	0
29	0	0	0
30	34	33	23
31	38	44	48

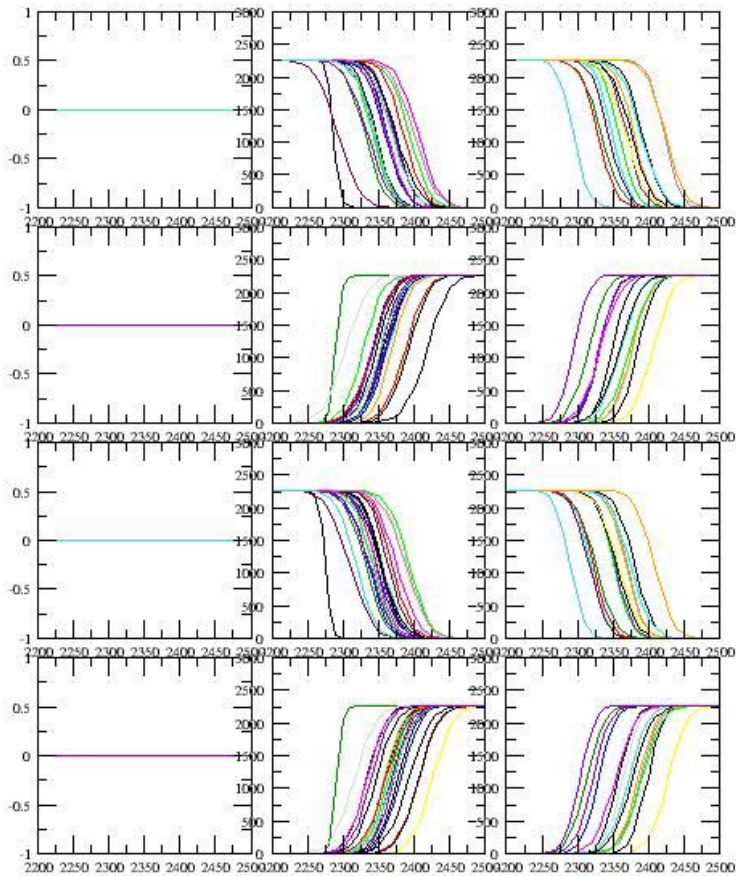
The console window shows the following output:

```

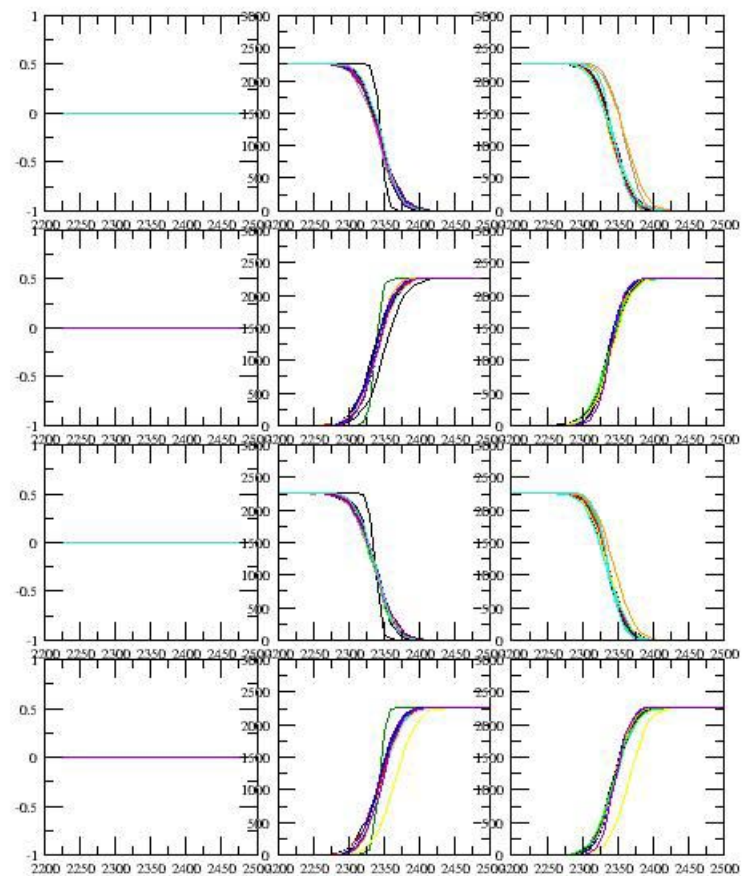
man/man1/xvidt
man/man1/xvinfo
kg/info/xvfb.1
kg/info/xvfb.m
kg/info/xvfb.postinst
kg/info/xvfb.preinst
61:~/uCLinux-dist-timer-mod/user/detect/python# xvfb
command not found
61:~/uCLinux-dist-timer-mod/user/detect/python# ls /usr/doc/xvfb

```

# Automatic threshold equalization



*before correction*



*after correction*

# Current detector



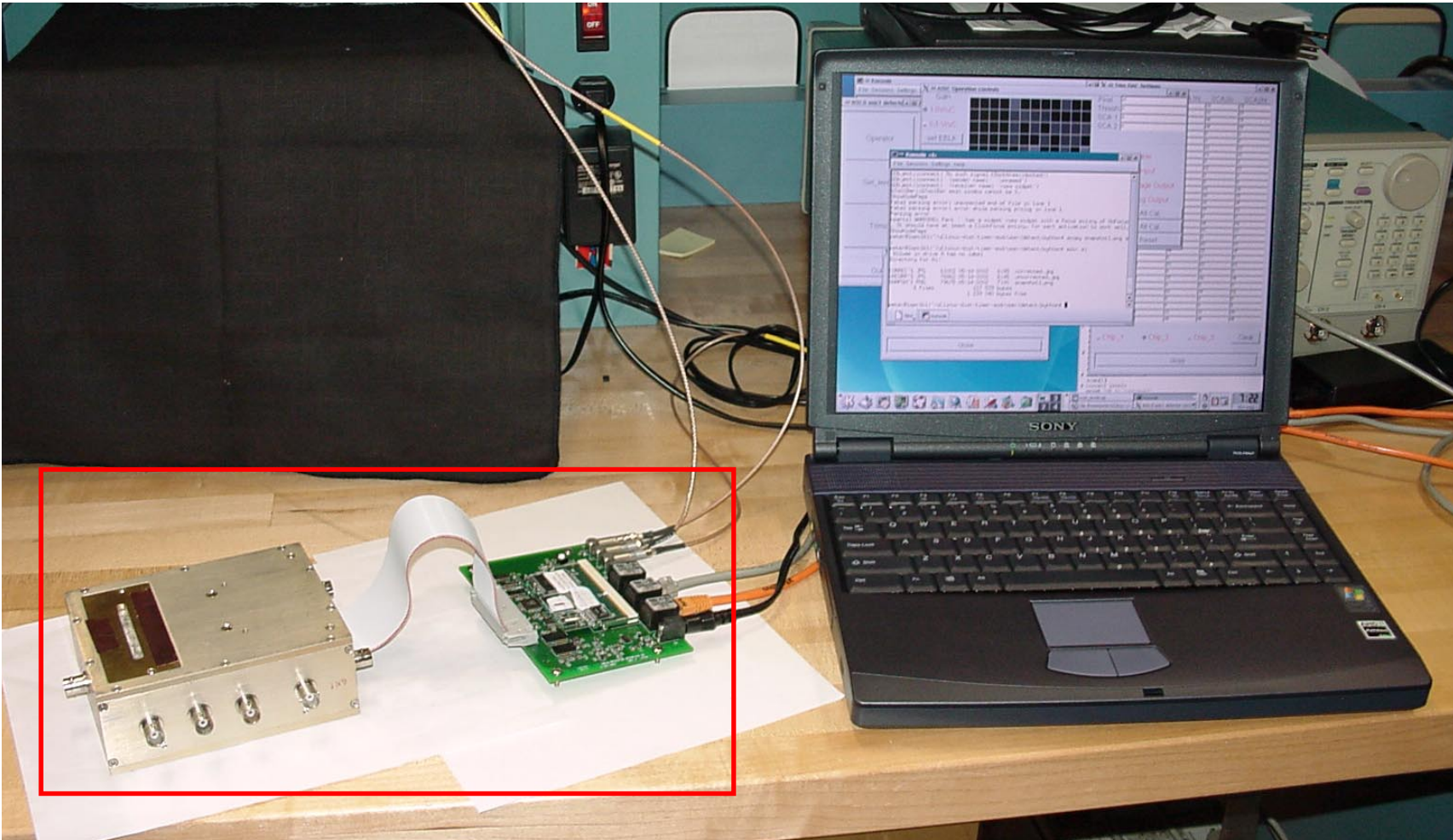
head - *preamplifiers*

$\approx 100$  channels,  $> 350$  eV,  $< 1$  MHz



rack - *shapers ...*

# New detector



$\approx 400$  channels,  $< 300$  eV,  $> 10$  MHz



## Next steps

- Test at high rate (in excess of 50kHz / pixel)
- Gap selection (10 $\mu$ m, 30 $\mu$ m, 50 $\mu$ m)
- ASIC optimization
- Test of four-quadrant version
- Peltier cooler implementation

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### Acknowledgment

DOE (support)

Veljko Radeka, Pavel Rehak, Graham Smith (discussion)

John Triolo (technical)