Front-End Electronics Development at BNL*

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presented at the International Workshop on Analog Front-End VLSI Electronics for Radiation Imaging Detectors, Marathon, Greece, Sept. 28-30 1995

1.0 Introduction

AT BNL the monolithic front-end electronics development effort is an outgrowth of work in discrete and hybrid circuits over the past 30 years. BNL's area of specialization centers on circuits for precision amplitude measurement, with signal-to-noise ratios of 100:1 and calibration to the same level of precision. Circuits are predominantly classical, continuous-time implementation of the functions now performed by hybrids, with little or no loss of performance. Included in this category are charge- and current-sensitive preamplifiers, pulse shapers, sample/hold, multiplexing, and associated calibration and control circuits. Presently integration densities are limited to 16 channels per chip

Table 1 is a list of chips under development. Note that for the low-C front end, we are pursuing both CMOS and bipolar implementations.

Two examples will be presented to illustrate the techniques needed to adopt hybrid circuits to the constraints of monolithic CMOS technology.

2.0 Circuit Examples

2.1 Programmable pulse shaper

Classical pulse shaper designs rely on RC products to set the peaking time. In monolithic technology the poor tolerance of passive components may cause large variations in these time constants. Therefore we set the RC product using programmable arrays of resistors and capacitors which can be digitally adjusted [1].

Even when precise time constant control is not required, we may wish to provide a range of values to allow users to adapt the chip to changing experimental conditions, e.g. luminosity upgrades in colliders. To address this second need, we have designed into IC28 (see

* This research was supported by the U.S. Department of Energy: Contract No. DE-AC02-76CH00016

Table 1) a shaper with peaking time and gain each digitlly adjustable over a range of about 3:1. Waveforms of this shaper are shown in Fig. 1.

2.2 Charge-sensitive preamp for very low detector capacitance

Silicon drift detectors [2] are unique in having extremely low anode capacitance (< 100 fF) together with a large sensitive area (>10 cm^2). In designing a low noise preamplifier, the series noise which is proportional to C_{in} can thus be very low:

$$ENC^2 = 4kT\left(\frac{R_s C_{in}^2}{\tau_p}\cdot a_{F1} + \frac{\tau_p}{R_p}\cdot a_{F2}\right) \quad (1)$$

where ENC is the equivalent input noise charge, R_s and R_s are the equivalent series and parallel noise resistances, τ_p is the peaking time, and a_{F1} and a_{F2} are dimensionless form factors (of order 1) related to the details of the pulse shape.

For example, in this application with $\tau_p = 50ns$, the ENC can be kept below 200 r.m.s. electrons for $R_s < 1k$ and $R_p > 500k\Omega$. In this case the R_s goal is easy to achieve, but R_p higher than a few times 10^4 Ω is difficult because of the lack of high-resistivity materials in the CMOS process. (In hybrid technology, high-quality resistors up to the 10^8 Ω range are available.) If we use a physical resistor made with the highest sheet-resistivity material available (the nwell), it will have about 2 pF of parasitic capacitance. This adds noise and causes instability in the feedback loop. Switched-reset techniques are excluded because the drift detector needs an amplifier which is continuously sensitive.

The only remaining solution is to try to make a high-value resistor from a long-channel FET. The resistance of a MOSFET operating in the triode region is

$$R_{eq} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(V_{gs} - V_T)} \quad (2)$$

where μ is the inversion layer mobility, C_{ox} is the gate oxide capacitance, *(W/L)* is the FET width/length ratio, and $(V_{gs} - V_T)$ is the gate bias voltage at equilibrum. If we use a PMOS transistor, then a device with *(W/L)* = 1 and $(V_{gs} - V_T)$ = 1V will have a resistance of 30 kΩ. Clearly, a long-channel device with small $(V_{gs} - V_T)$ is needed. There are, however, important other constraints on this device. First, we need to keep the capacitance of the channel to the gate small to avoid degrading the noise and/or stability of the feed-back loop. It is also necessary to have a bias point which is stable against V_T variations. These criteria can be summarized as:

$$C_G = C_{ox}WL < C_{det}, C_F \tag{3}$$

$$\frac{\sigma_{R_F}}{R_F} = \frac{\sigma_{V_T}}{(V_{gs} - V_T)} < \varepsilon \tag{4}$$

Taking 2 MΩ as a target value for R_F and constraint values of σ_{VT} = 150 mV and ε = 10%, we get from (4) and (2):

$$(V_{gs} - V_T) > 1.5V \tag{5}$$

$$\frac{W}{L} < 0.01 \tag{6}$$

and from (3) with C_F= 200 fF,

$$WL < 100\mu\text{m}^2 \tag{7}$$

These constraints are summarized graphically in Fig. 2, which shows the design space of W and L for the MOS resistor. When combined with the design rule limits on W and L, there is no solution to produce such a high-value resistance with low capacitance.

We therefore adopted a novel bias scheme, illustrated in Fig. 3, to produce a gate bias voltage which tracks changes in threshold variation. The input stage of the preamp is a folded cascode with NMOS input device M1. The feedback device, M2, is connected from output to input as shown. We create a scaled replica of M1 (M1'), bias it at the same current density as the input device, and connect it as a diode to generate a potential which tracks the gate of M1, even with variations in NMOS threshold voltage and current. Next, we use a diode-connected PMOS device (M2') to create a voltage equal to the desired Vgs of the feedback device M2. M2' is a scaled copy of M2, so it tracks variations in PMOS threshold including those caused by the body effect on these floating-source devices. Finally, the W/L ratio of M2' is chosen to produce a (V_{gs}-V_T) which gives the desired resistance in M2. Equation (3) in the figure shows that (V_{gs2}-V_{T2}) is independent of threshold voltages and power supply voltages. It depends only on geometrical ratios (α, n, and $(W/L)_2$), and sublinearly on the technological parameters μ and C_{ox} , and the bias current I_2. This has the important consequence that the variation of feedback resistance is no longer dependent on the bias voltage, i.e. one can bias the feedback device very near threshold and still have its resistance variation depend only on the variation in μ, C_{ox}, and I_2. Hence we can set (V_{gs2}-V_{T2}) to about 150 mV and relax constraint (6) to

$$\frac{W}{L} < 0.1 \tag{8}$$

The relaxed constraint is also shown on Fig. 2. We now have an allowed region in the design space of W_2 and L_2. Our circuit uses a feedback device with W/L = 3/20 microns biased at about 150 mV above threshold. Preliminary measurements on fabricated devices

show that the target resistance is achieved within 20% and that the parallel noise contributed by the feedback device is consistent with the resistance measured by the I-V characteristic. It is able to source a leakage current of over 300 nA and behaves predictable up to an input charge of over 80 fC. By controlling the gate voltage manually the equivalent feedback resistance can be increased up to tens of GΩ, with a concurrent reduction in parallel noise. With a high feedback resistance and a shaping of 10 microseconds, the ENC is 80 r.m.s. electrons. This value is close to the 1/f noise limit for this n-channel input device. The power dissipation is 2.3 mW/channel.

References

1. Durham, A., Hughes, J.B., and Redman-White, W., “Circuit Architectures for High Linearity Monolithic Continuous-Time Filtering”, IEEE Trans. on Circuits and Systems-II., 39(9), Sept. 1992, 651-657
2. E. Gatti and P. Rehak, Proc. 2nd Pisa Meeting on Advanced Detectors, Grosetto, Italy (1983); Nucl. Instr. and Meth. 225(1984) 608; Nucl. Instr. and Meth. 226(1984) 129

Front End IC's at BNL
1. Preamp/shaper for low-C detector • 50 ns, ENC < 250 e- @ CD < 1pF • Bipolar and CMOS versions
2. CSC Front End (GEM --> ATLAS muon det.) • preamp/shaper/track-and-hold/mux/CFD per channel • bipolar shaping; tp, gain programmable • ENC < 1500 e- @CD=150 pF @ 600 nsec
3. TRD Preamp/Shaper • 70 ns, dual gain range • ENC 1200 e- @ CD=15 pF
4. 5b FADC • 40 Msa/s • Nonlinear quantization (2 ranges); dynamic range 8b
5. JFET preamp for liquid calorimetry • rad hard (> 100 Mrad) • CD= 1nf, tp=50 ns • room temperature or cryogenic operation
6. CMOS Rad-hard preamp/shaper • 30 ns tp • match 35 pF CD
7. Absolute value capacitance measurement prototype • 0.4% error

TABLE 1.

$$ENC^2 = 4kT\left(\frac{R_s C_{in}^2}{\tau_p} \bullet a_{F1} + \frac{\tau_p}{R_p} \bullet a_{F2}\right) \quad (1)$$

$$R_{eq} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(V_{gs} - V_T)} \quad (2)$$

$$C_G = C_{ox} WL < C_{det}, C_F \quad (3)$$

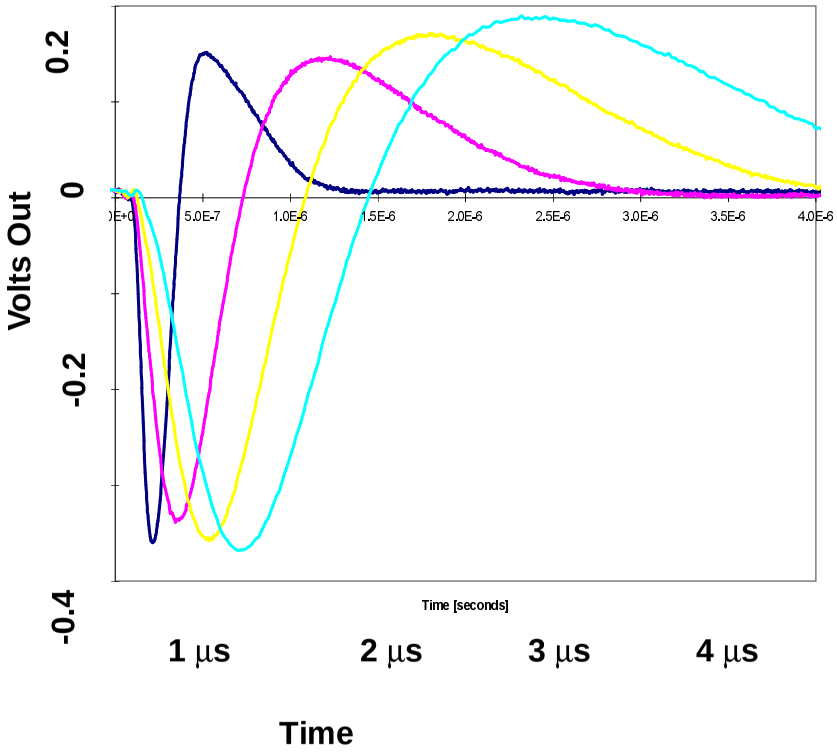
$$\frac{\sigma_{R_F}}{R_F} = \frac{\sigma_{V_T}}{(V_{gs} - V_T)} < \varepsilon \quad (4)$$

$$\frac{W}{L} < 0.01 \quad (5)$$

$$WL < 100\mu m^2 \quad (6)$$

CMOS Preamp/Shaper with programmable peaking time and gain for CSC

Peaking time 180 - 550 nsec



Gain 4 - 15 mV/fC

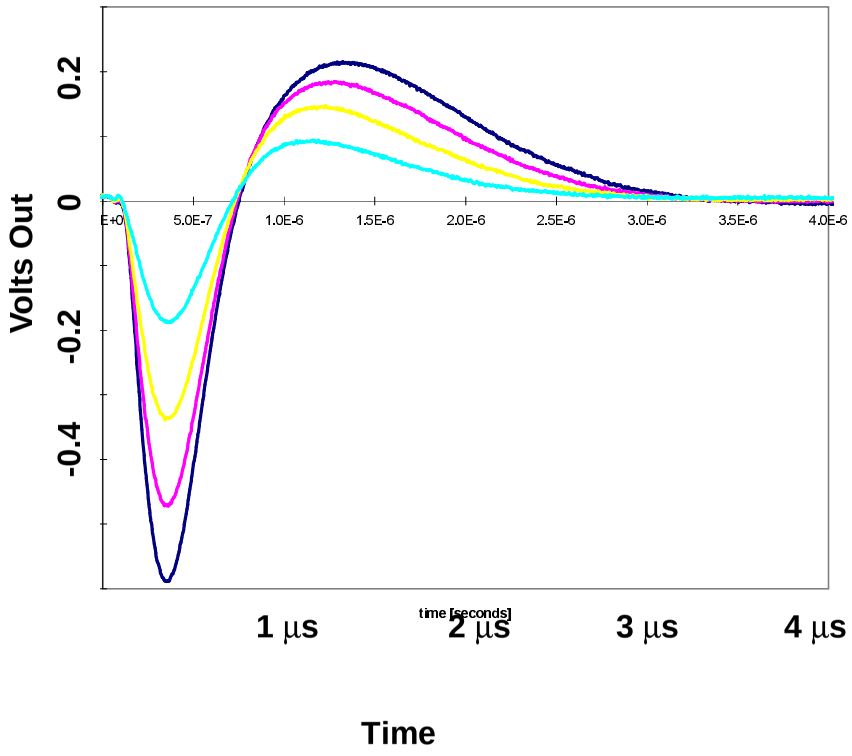


Fig. 1

Feedback Transistor Design Constraints

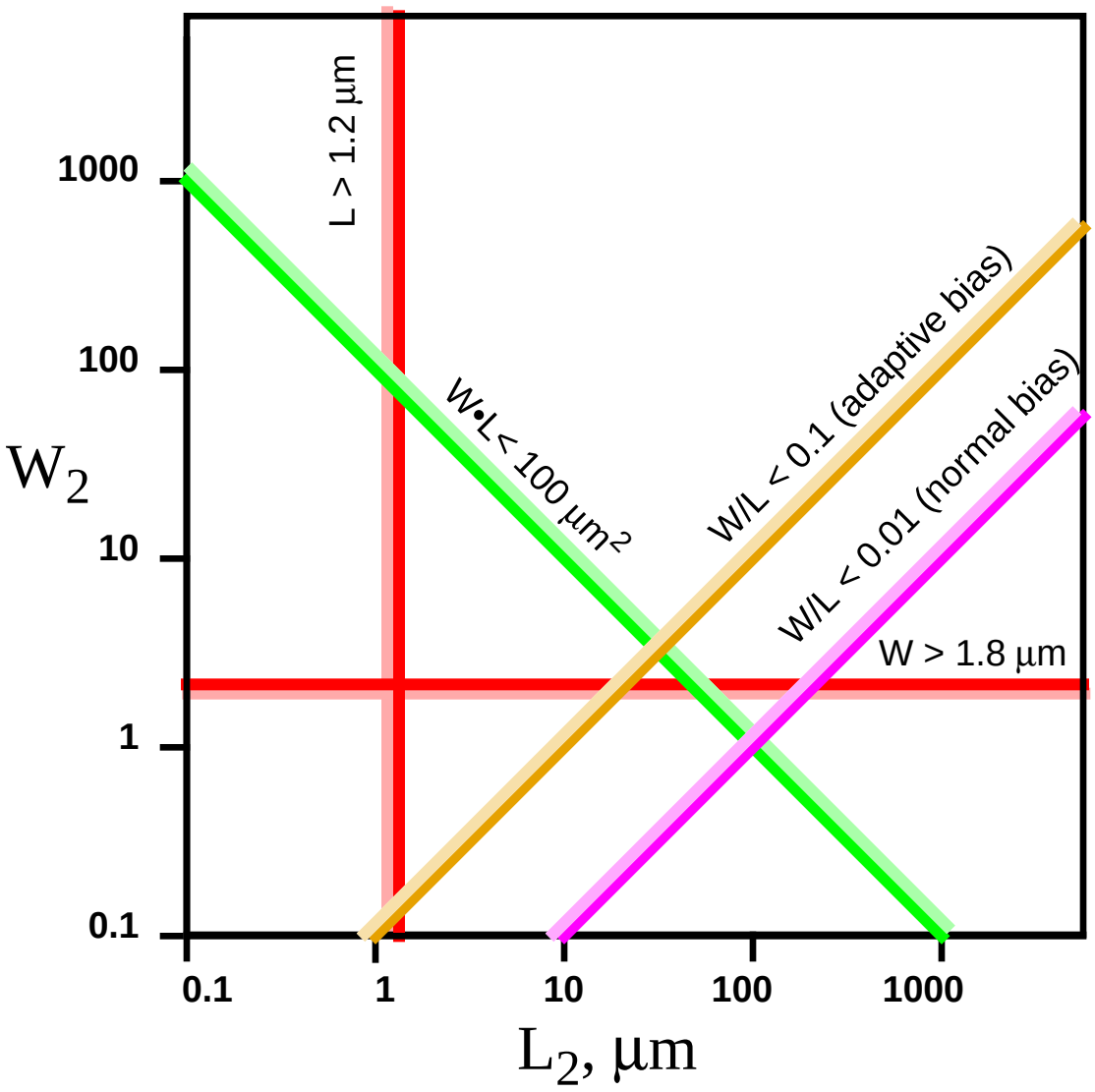
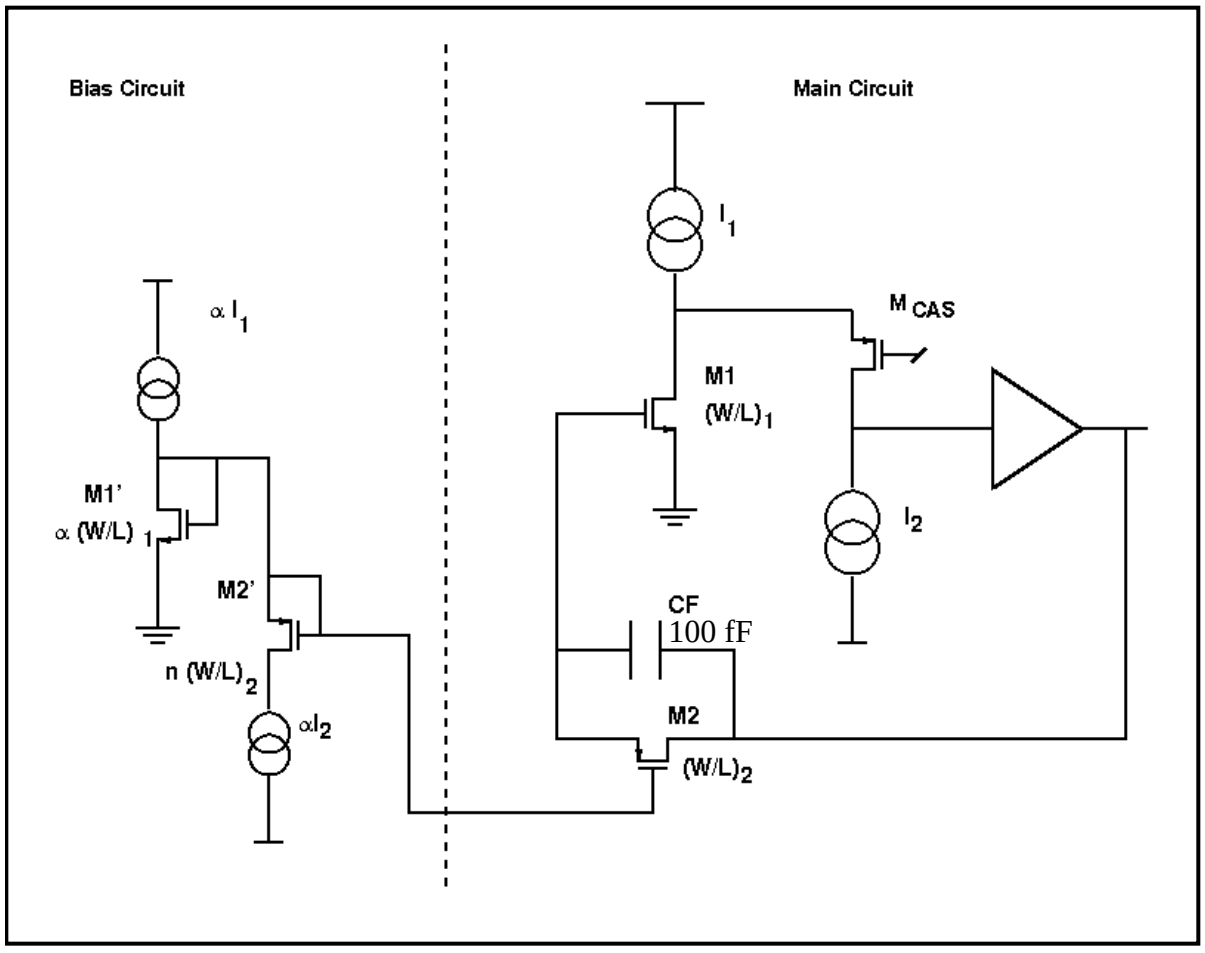


Fig. 2

Feedback FET Bias



Bias circuit function:

$$V_{g1'} = V_{g1} \tag{1}$$

$$V_{s2'} = V_{g1} = V_{s2} \tag{2}$$

$$\therefore (V_{gs2} - V_{T2}) = (V_{gs2'} - V_{T2'}) = \sqrt{\frac{2\alpha I_2}{\mu C_{ox} n (W/L)_2}} \tag{3}$$

---> gate voltage of feedback device M2 independent of V_{TP} , V_{TN}, V_{DD}, V_{SS}

Fig. 3