Readout Electronics for a High-Rate CSC Detector

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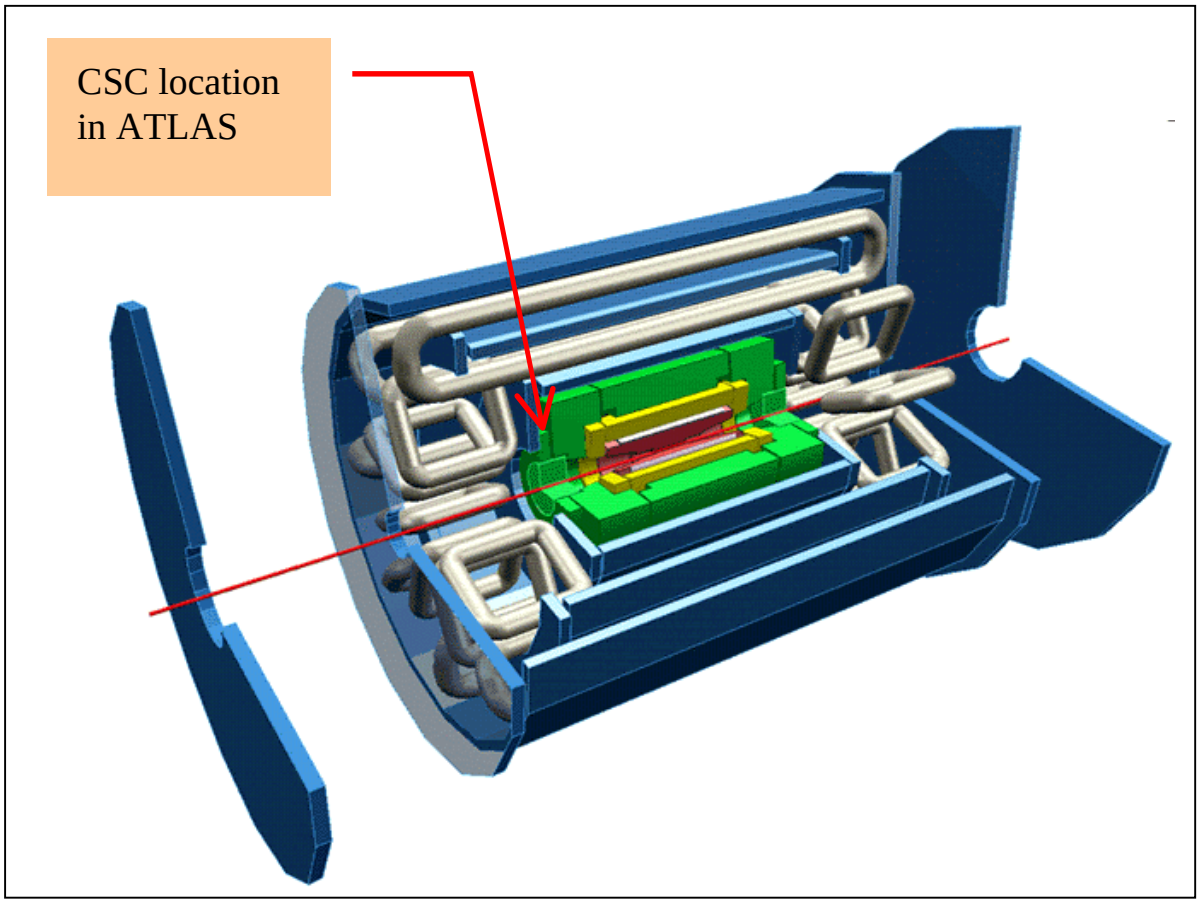
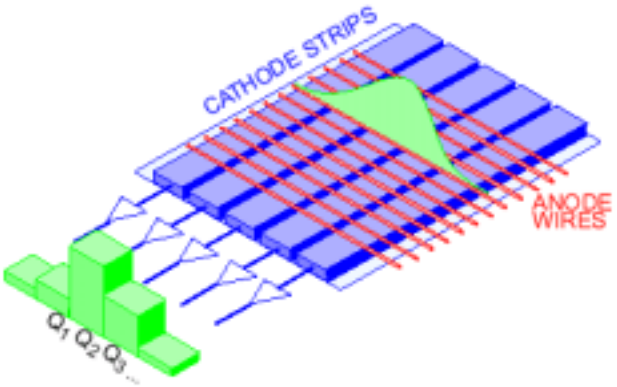


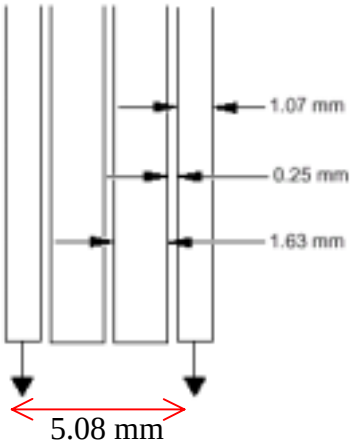
CSC Overview

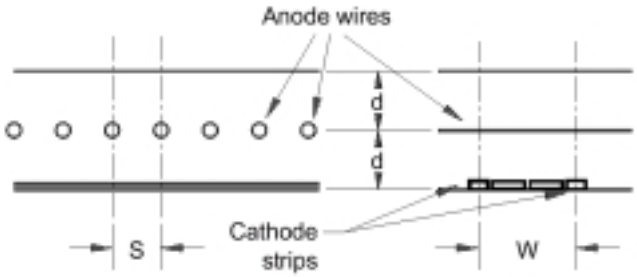
Functionality

60,000 channels of on-chamber readout electronics:

- Charge-sensitive preamplifier/shaper
- Calibration system
- Switched capacitor array analog memory
- Analog-digital converter
- Data concentration
- Detector Control System card (DCS)





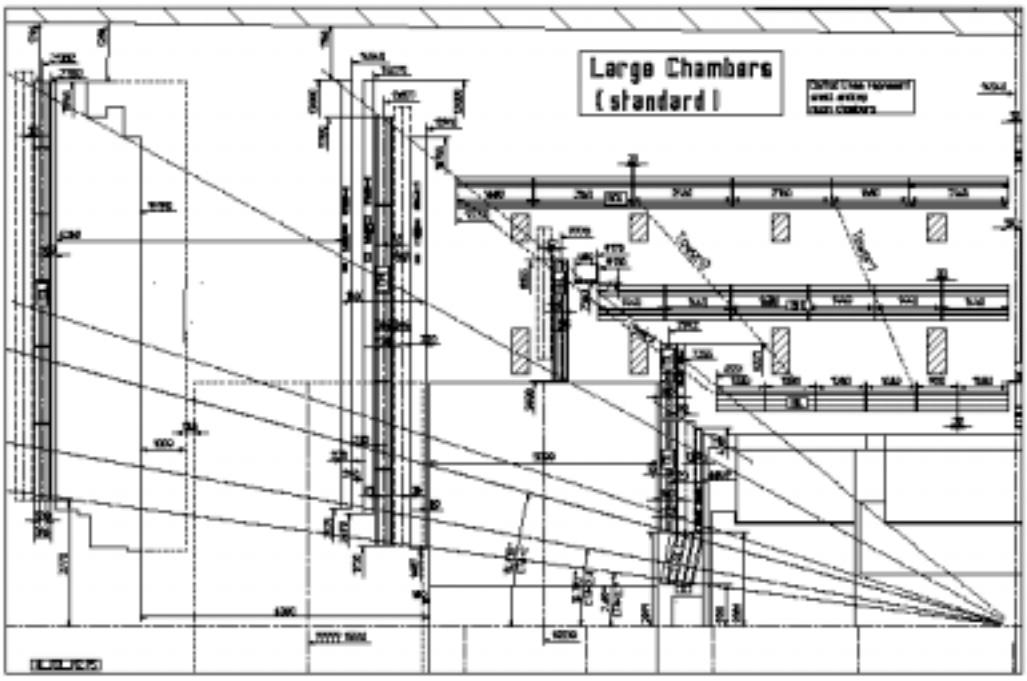


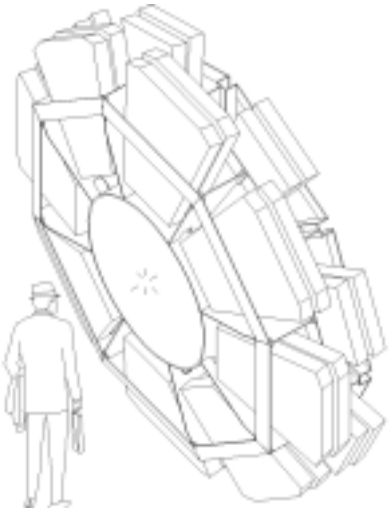
Requirements

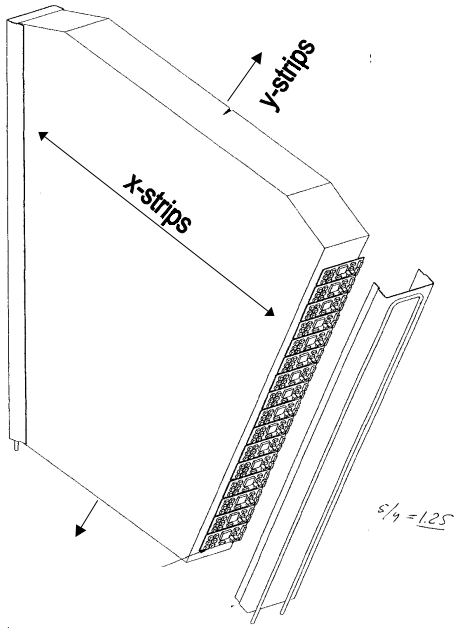
CSC electronics finds the muon position by interpolation of the charge collected in 3-5 adjacent strips.

Physics requirement is to measure this charge with sufficient precision to achieve a resolution 1/100 of the strip pitch, to assign the time of the avalanche to within one beam crossing, in a high rate environment where the rate per strip may reach 650 kHz at η=2.7.

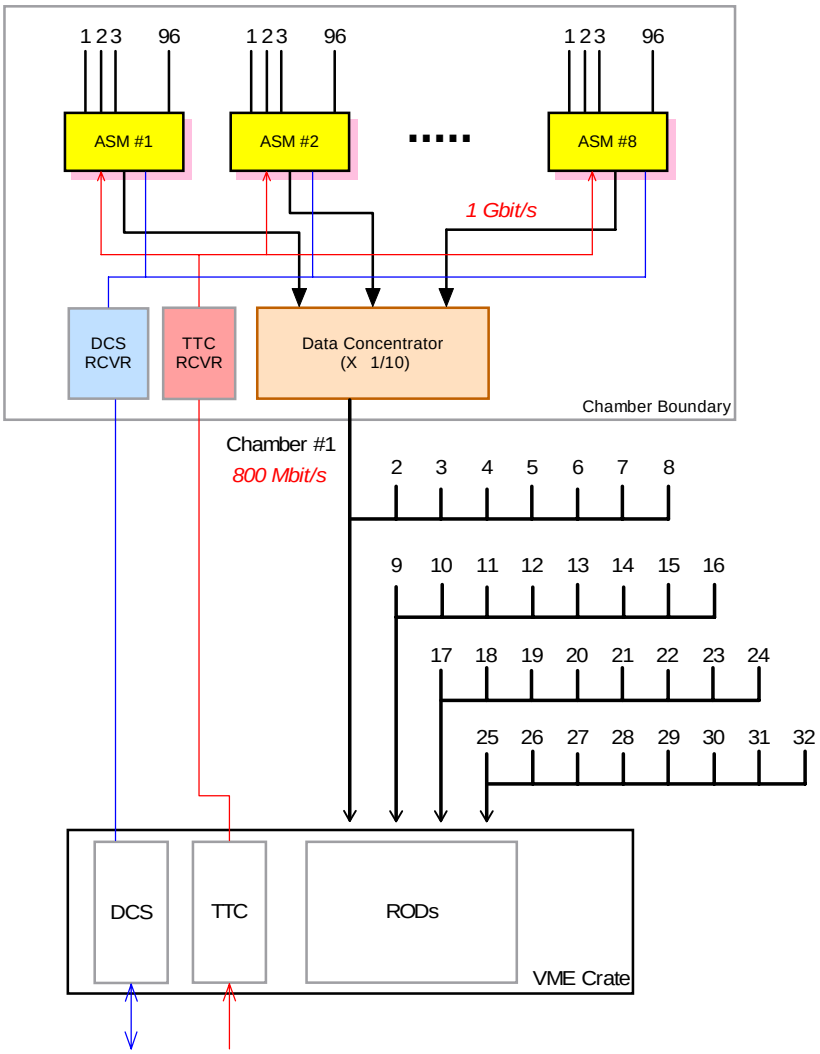
Chamber mechanics







CSC Readout Architecture



96-channel front end cards:

8 x 96 = 768 Precision coordinate channels
96 Transverse coordinate channels

Total number of channels:

864 channels per Chamber
864 x 32 = 27648 per each endcap

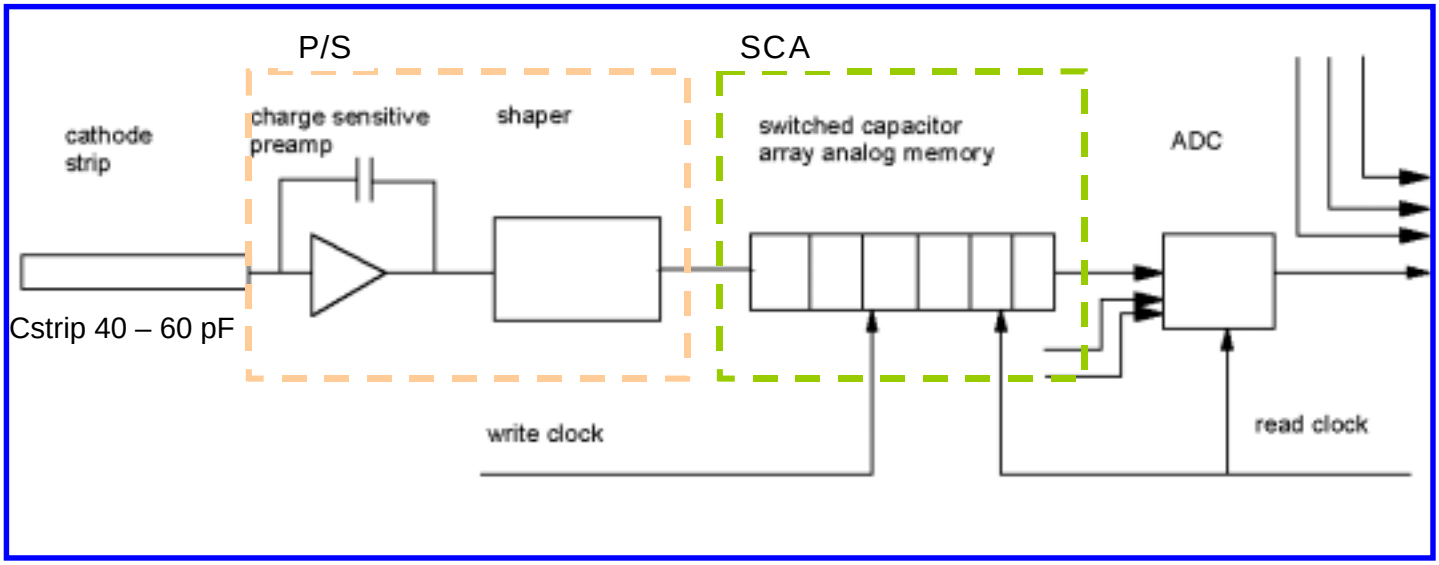
Total number of cards per endcap:

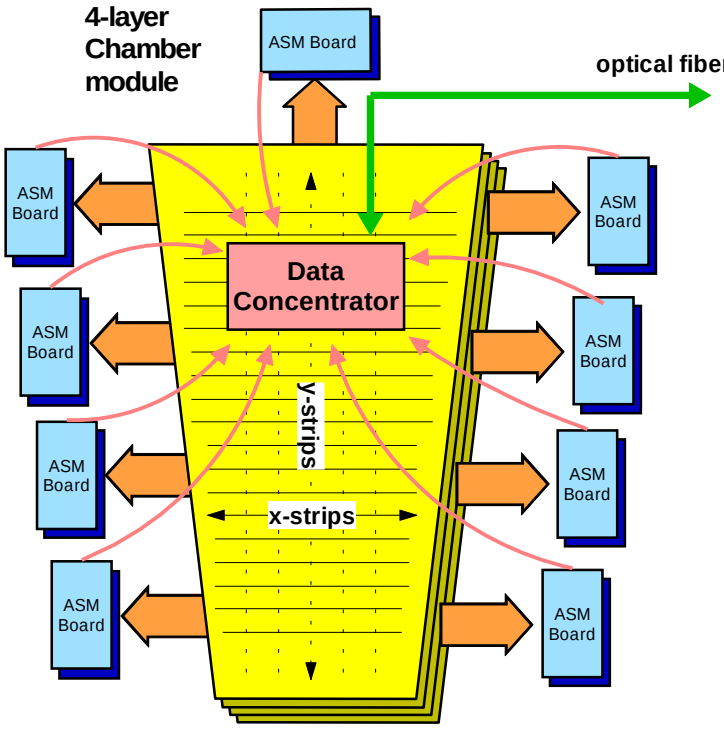
8 x 32 = 256

Electronics Overview

Amplifier-Storage Module (ASM) Boards:

96-channel boards that interface to the cathode strips





Amplify, filter strip signals.
Analog storage at 40 Msa/s during the Level 1 trigger latency.

Digitize on the ASM board.

Data concentrator for zero suppression and sparsification.
Reduce data by 8x – 15x.

Signal Processing

Signal to noise ratio

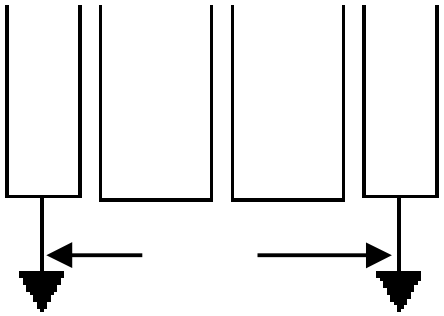
$\sigma_x/x = k\ \sigma_Q/Q \qquad k \sim 2$

Want $\sigma_x/x \sim .01$

Require $\sigma_Q/Q < 1/200$

$Q_{ave} \sim 70$ fC

$\Rightarrow \sigma_Q =$ 2000 e-



Shaping

Pulse width must be kept short to avoid pileup:

FW1%M < 430 ns.

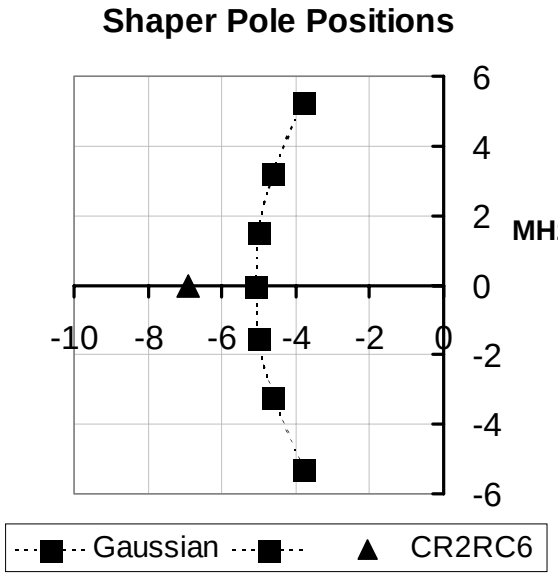
CR-RC^n shaper very asymmetric:

short peaking time (noise), or high n.

Complex-pole shaper:

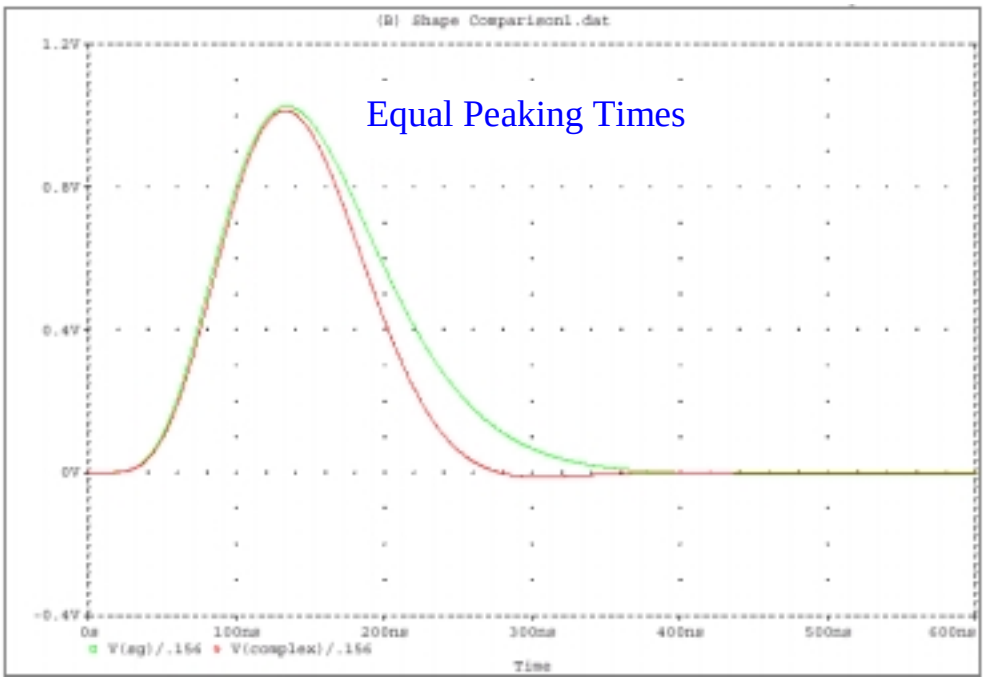
More symmetric pulse for same n.

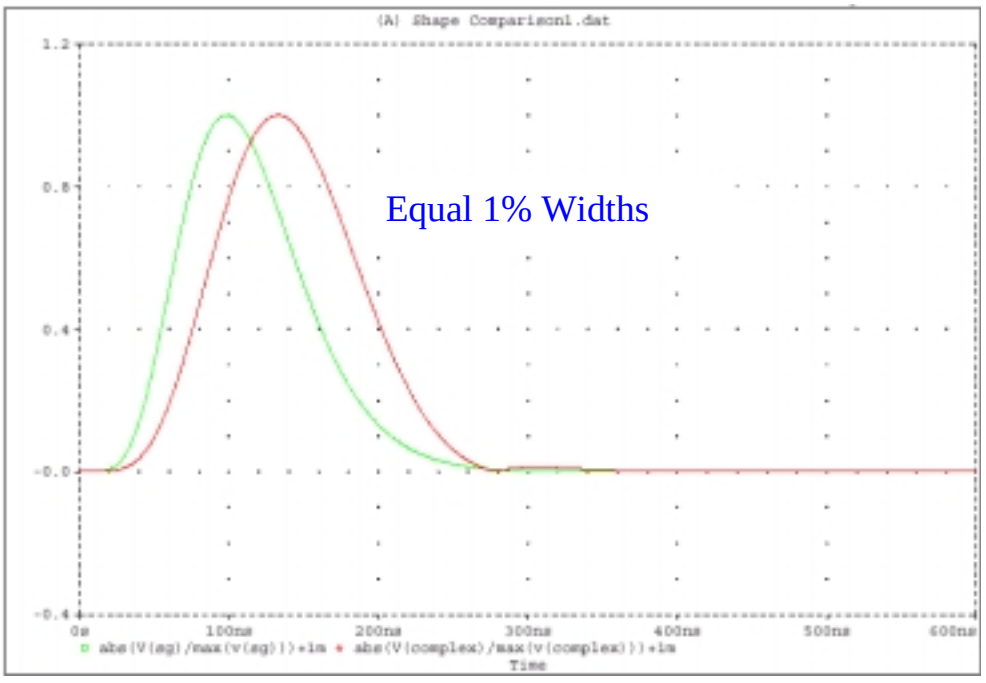
Reduce noise without increasing power.



Ohkawa, NIM 138 (1976) 85-92, "Direct Syntheses of the Gaussian Filter for Nuclear Pulse Amplifiers"

Shaping Filters with Complex Poles





CR - RC6

7^{th} order complex

(we use bipolar shape to reject LF noise)

Preamp/Shaper ASIC (P/S)

Technology: 0.5 um CMOS

Behavioral model (MathCAD) finds ENC as function of Power, W, and L.

Includes:

- Strong, moderate, weak inversion regime with continuous expressions based on EKV model
- Transistor DL, DW
- Short gate effect on Vt
- Output conductance $g_d = g_d(I_{ds}, L)$
- Body effect
- 1/f noise from measurements on HP 0.5um process
- Hot electron excess noise (dependent on L, VDS) from literature

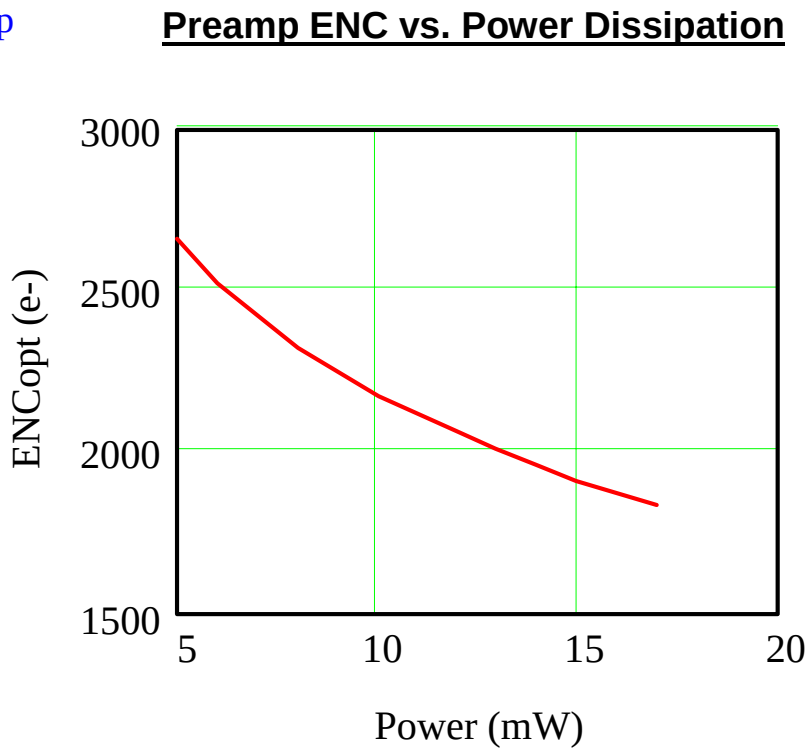
Numerical optimizer finds L and W for lowest noise with power as constraint.

Also calculates optimum W,L for other transistors in preamp circuit to minimize excess noise.

Also calculates poles, Zin, stability.

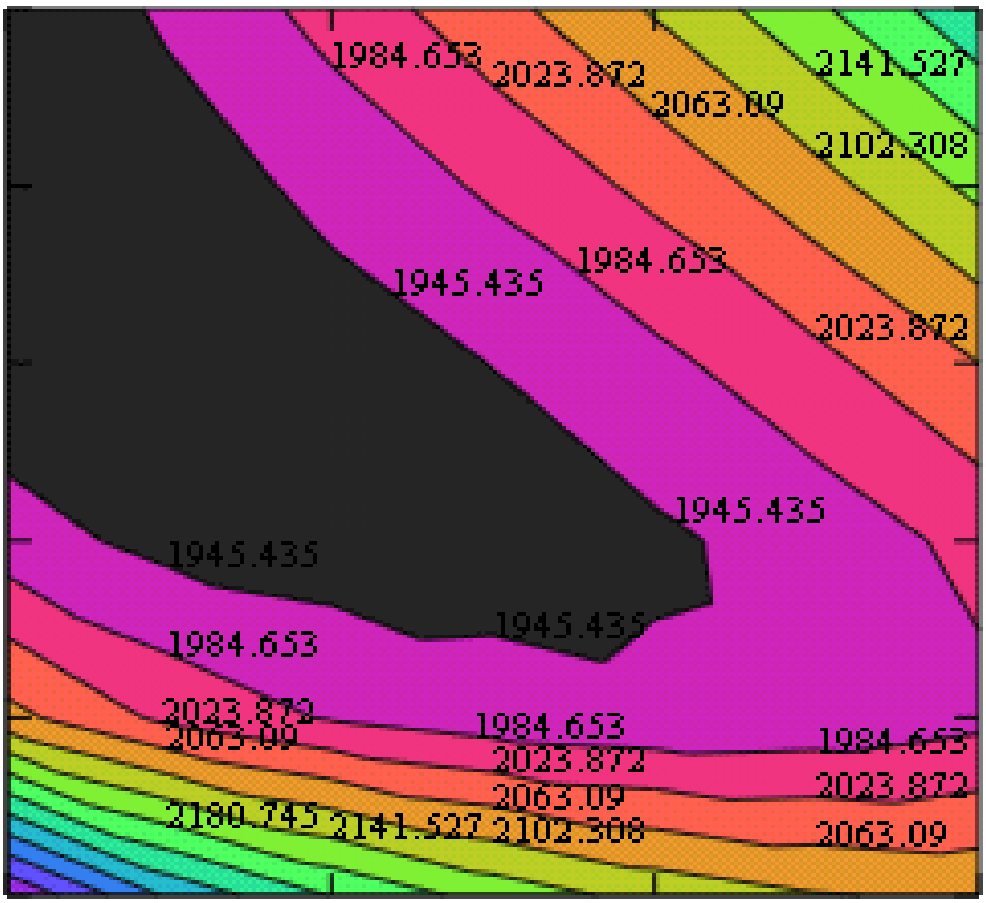
Very useful for pre-SPICE calculation.

Similar programs used for preliminary sizing of devices in shaper amplifiers.



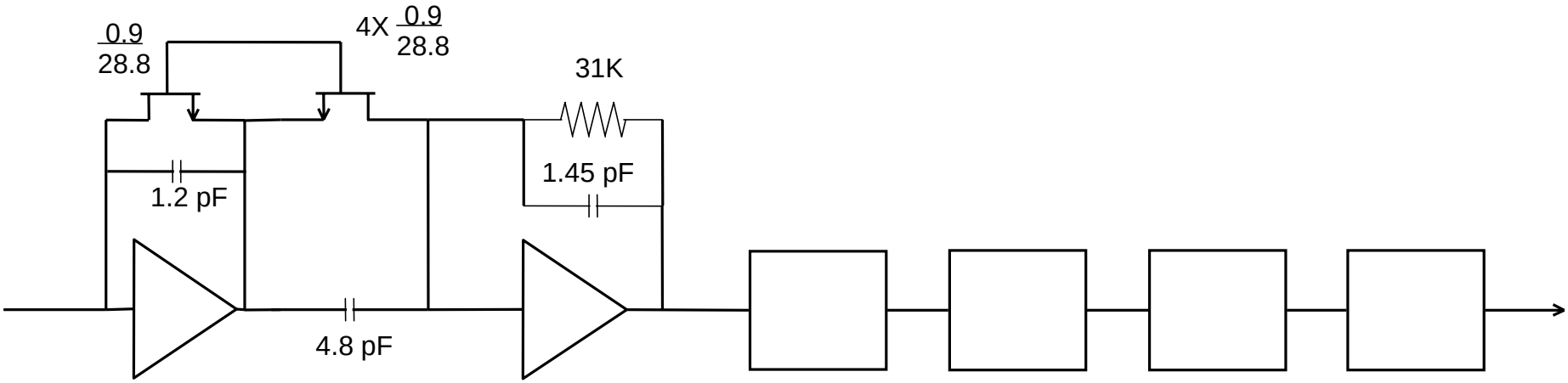
Preamp Optimization

Preamp ENC vs. W and L



CSC Preamp/Shaper

Block Diagram



Preamp

Compensation

1st Pole
5.12 MHz

2nd-order
Lowpass

5.24 MHz
Q = .5234
H0 = 1.67

2nd-order
Lowpass

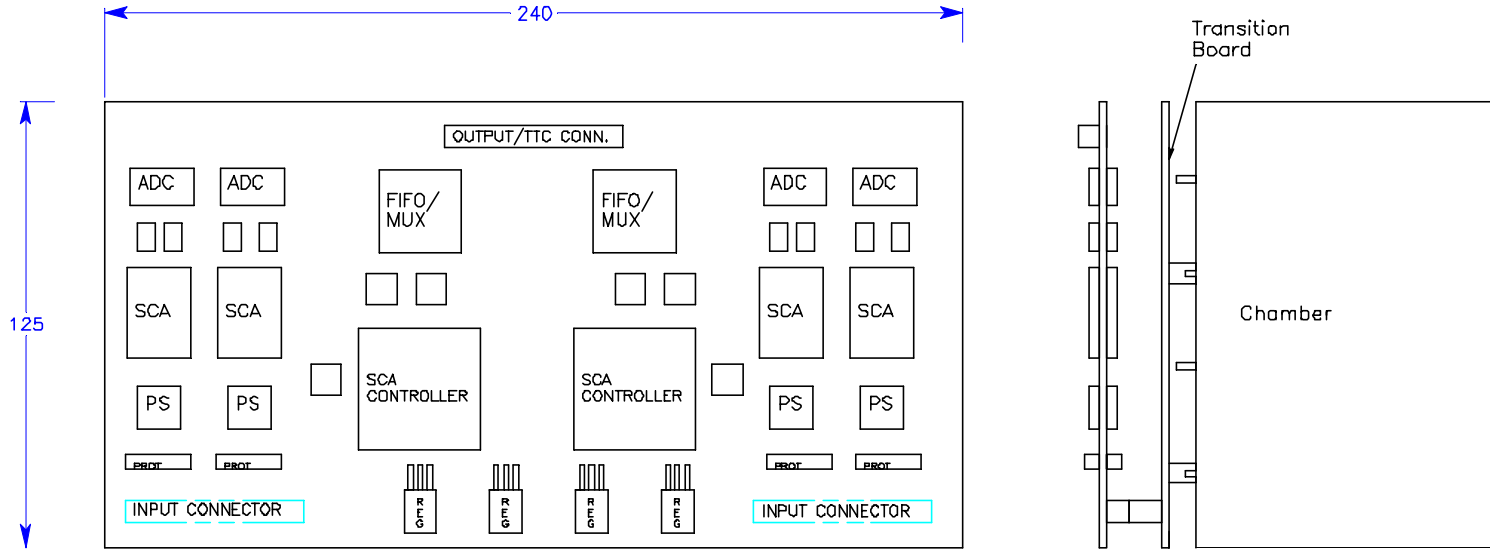
5.63 MHz
Q = .6098
H0 = 1.22

2nd-order
Bandpass

6.51 MHz
Q = .8549
H0 = 3.0

Class AB
Ouput
Buffer
Gain = 2

96-channel ASM Board



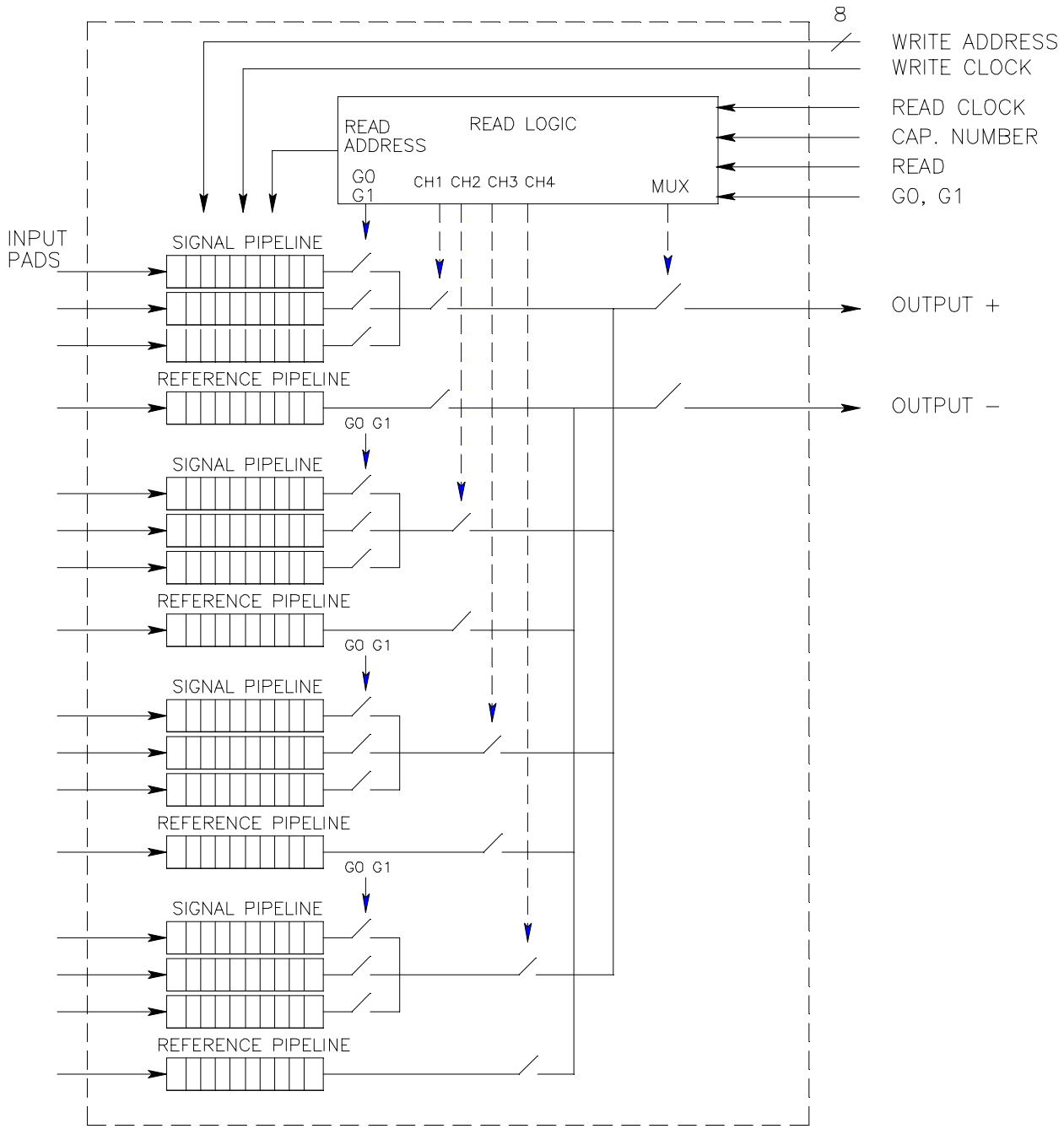
This board would read out signals from 2 CSC planes. A similar board on the opposite face of the chamber would read out the other 2 planes.

The transition board re-maps the 96 strips into a single row connector on the long edge of the top side.

Density per channel is 6X higher than LAr Front End Board

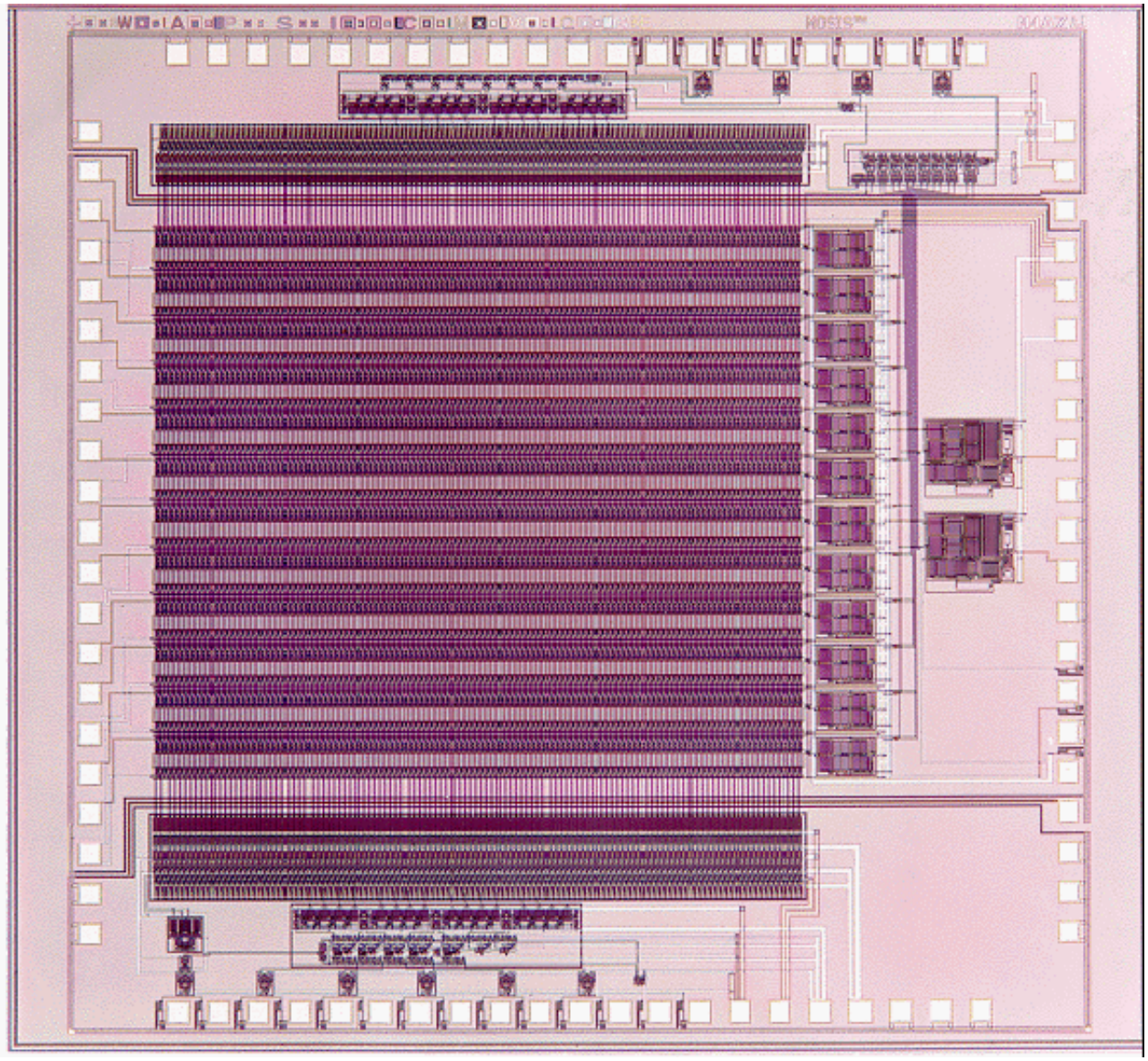
SCA Block Diagram

144 cells/channel
16 channels, organized as 4 groups of (3 + 1 reference)
Simultaneous read and write (deadtimeless)



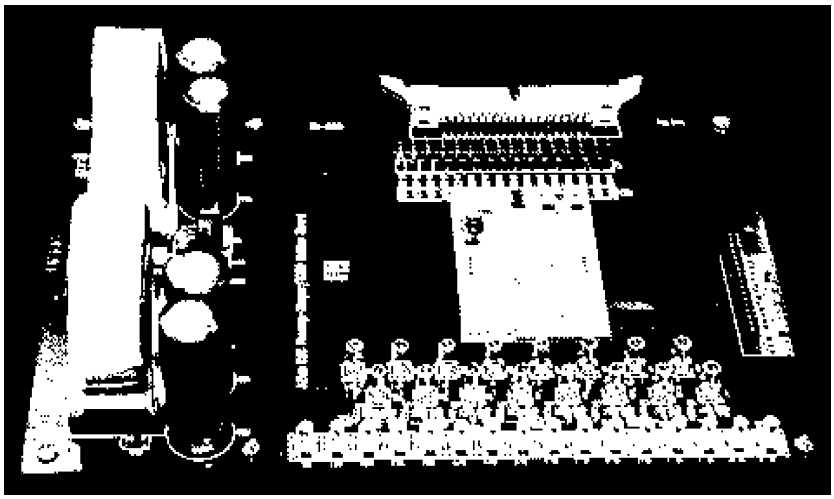
SCA Die Photograph

Technology (final version): DMILL 0.7µm CMOS

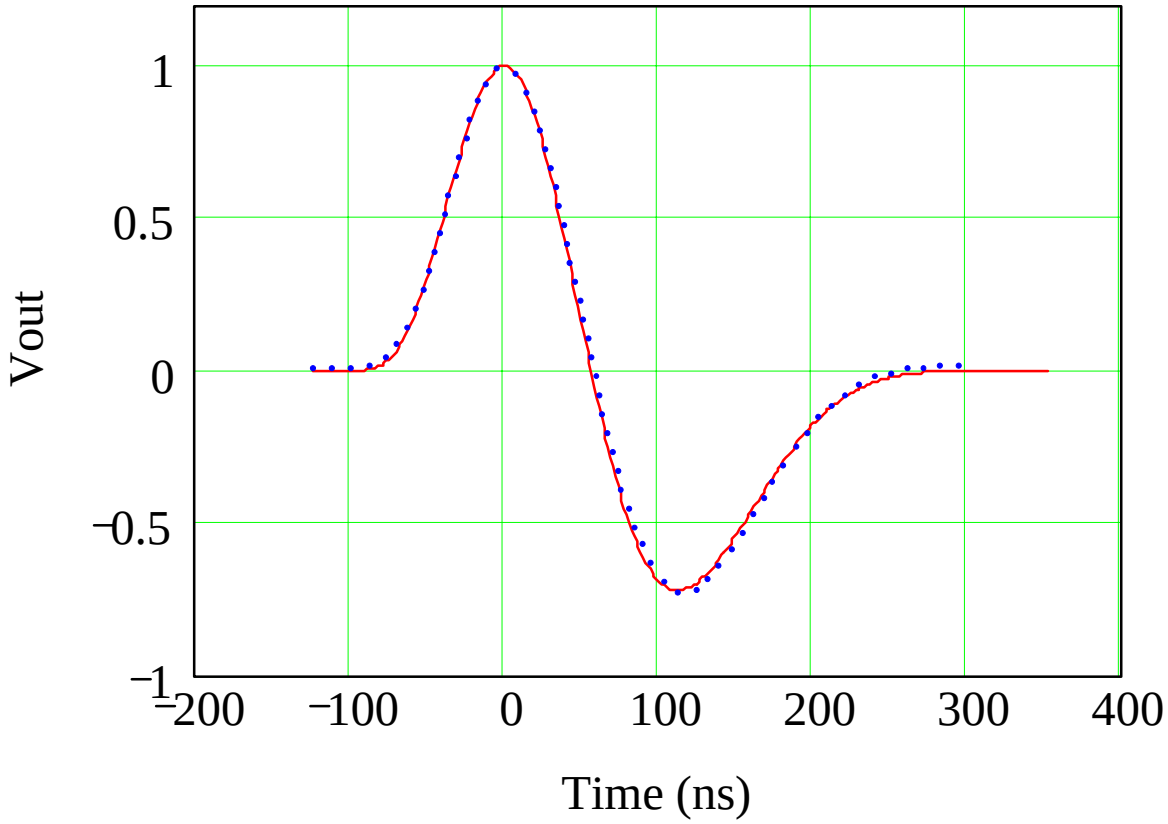


P/S Results

Measurement board

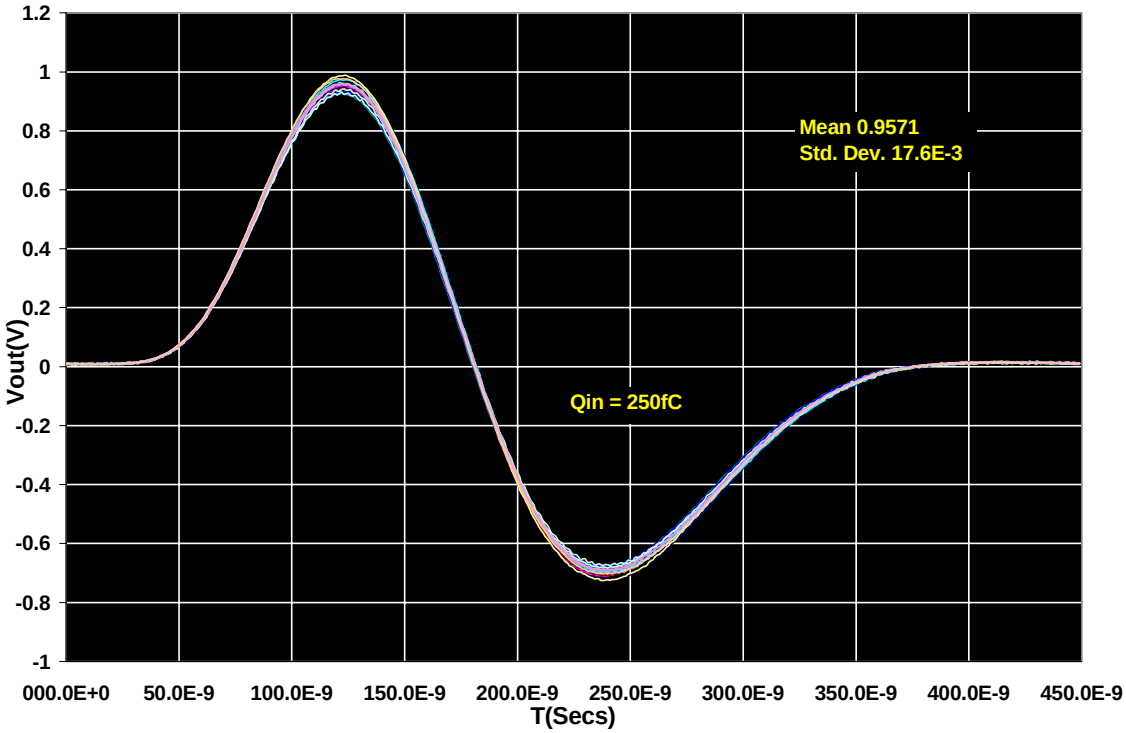


Pulse Shape simulated (solid red line) and measured (blue dotted line)

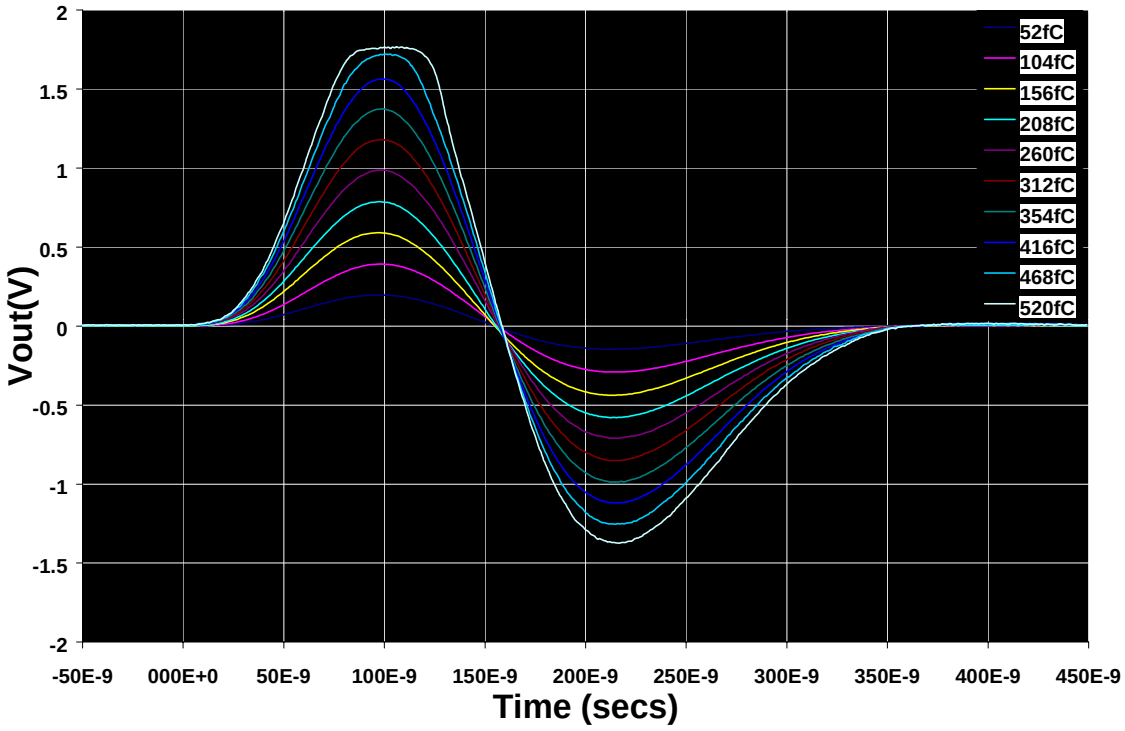


P/S Results

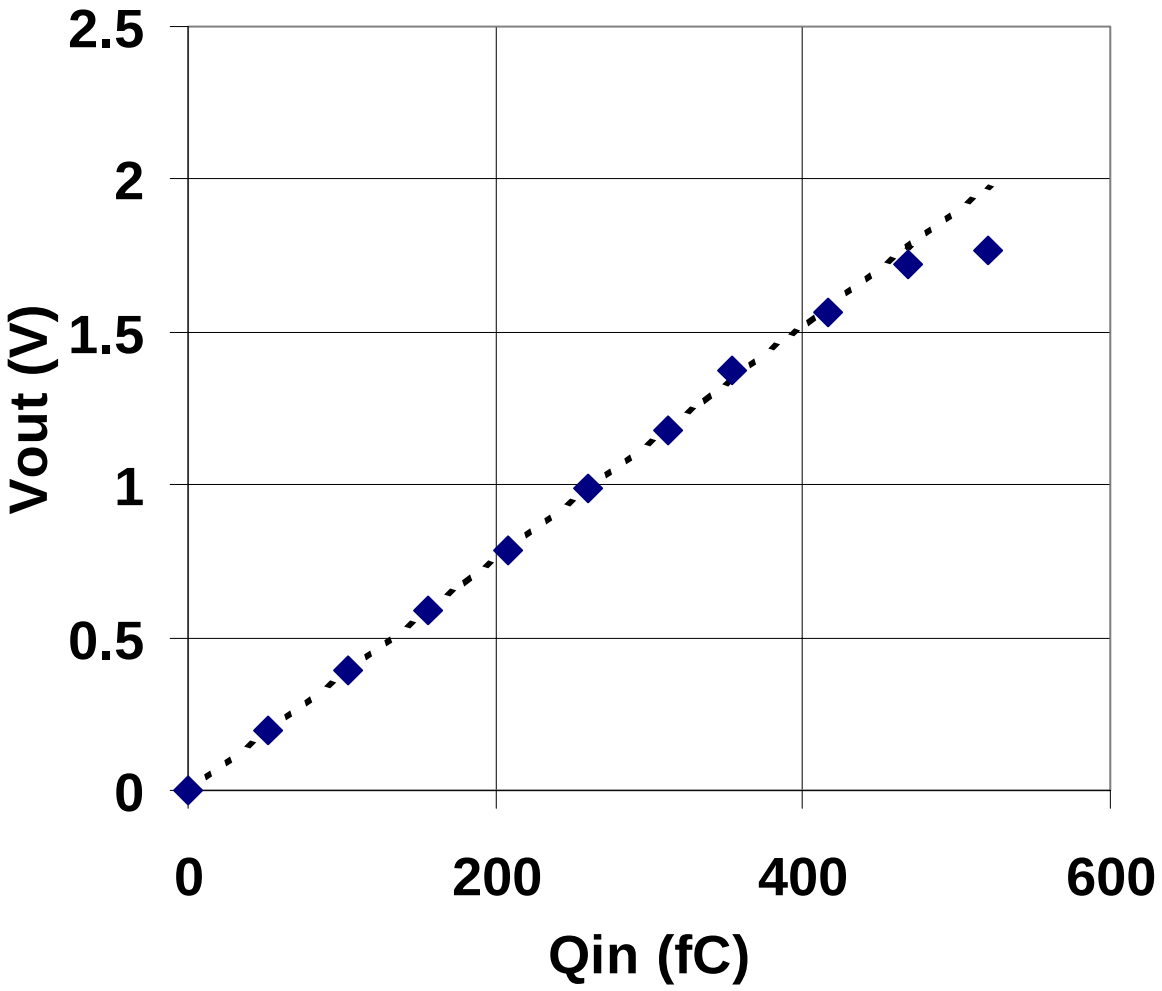
Channel-to-channel variation (2%)



Rail-to-rail output

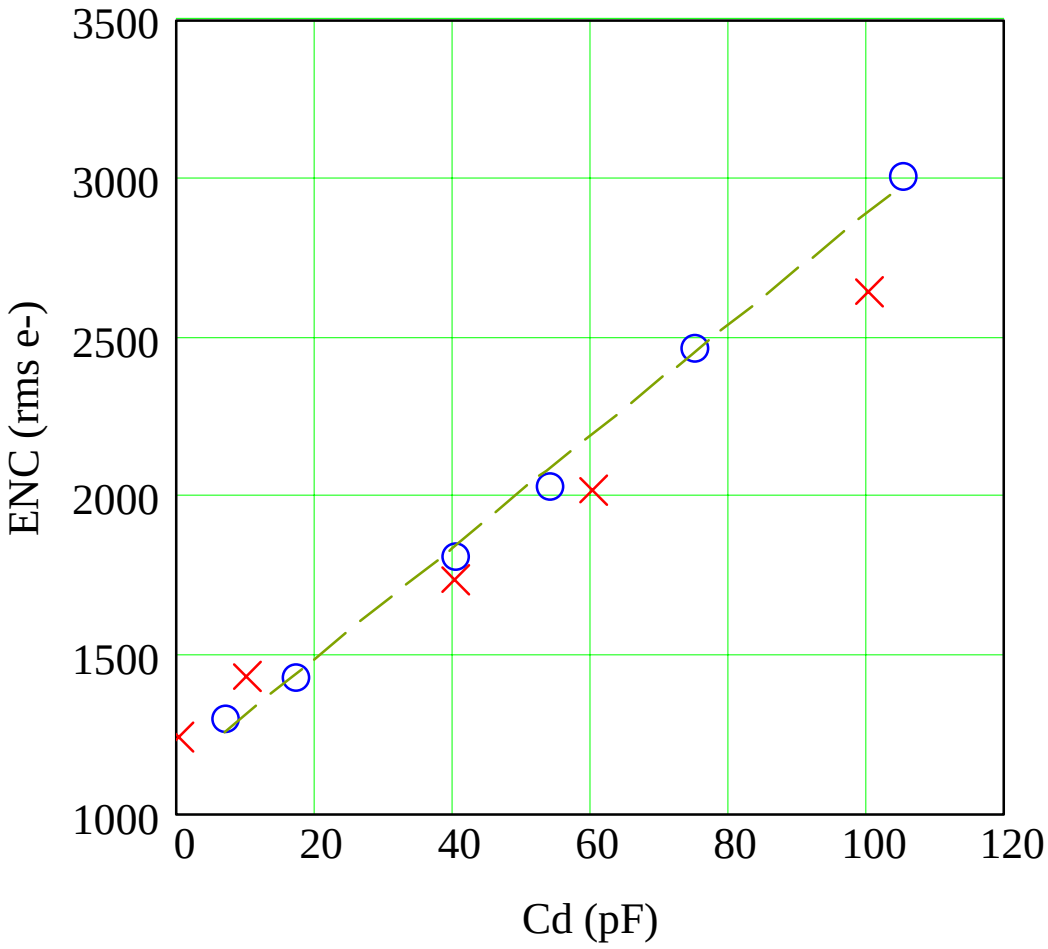


P/S Linearity



P/S Noise Results

Noise vs. input capacitance

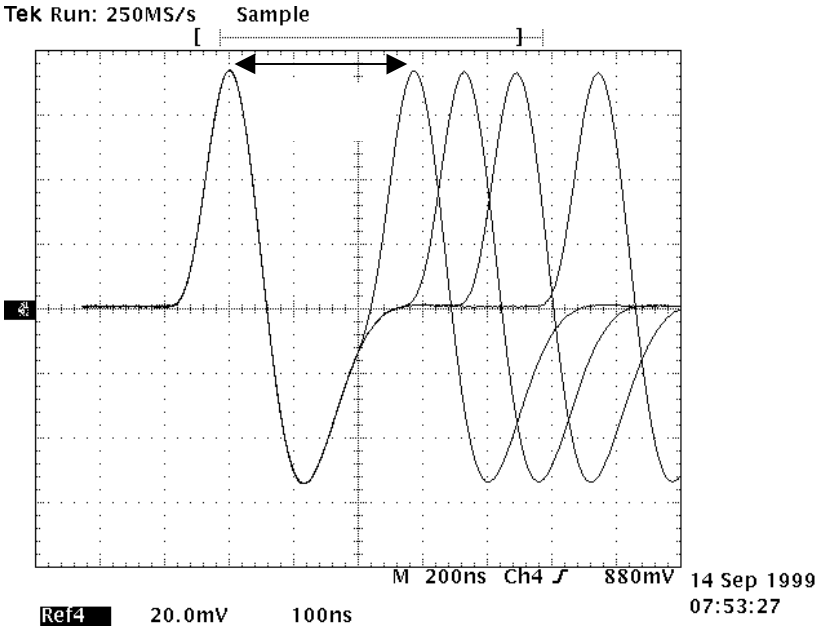


Simulated: ×

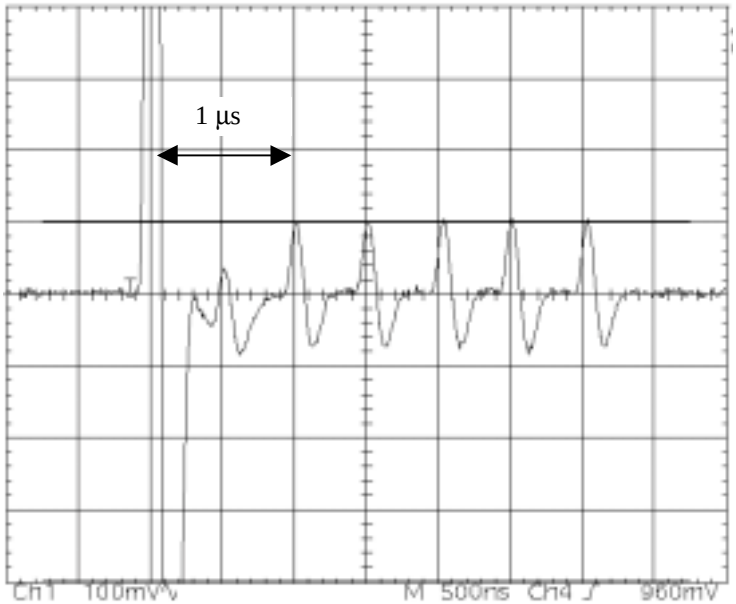
Measured: O

P/S high rate response

Pileup



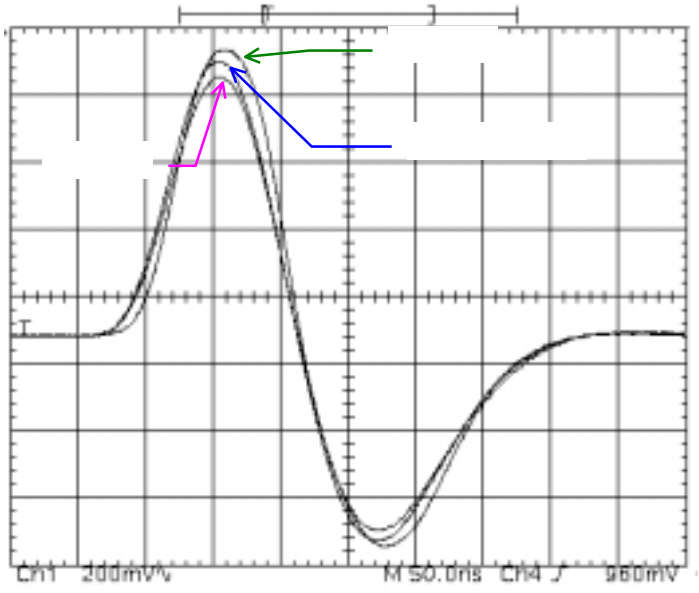
Recovery from 2X overdrive



P/S Output Driver Results

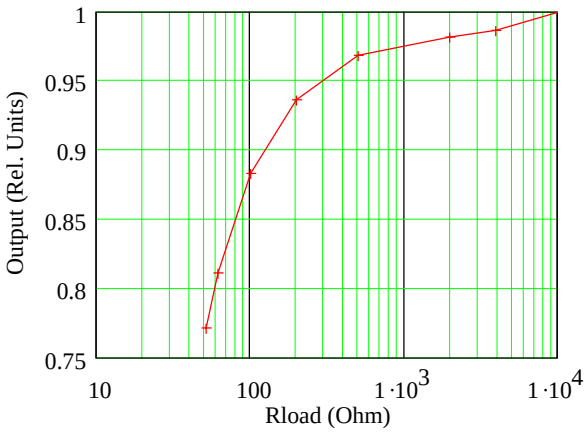
Effect of resistive and capacitive loading

200 fC input

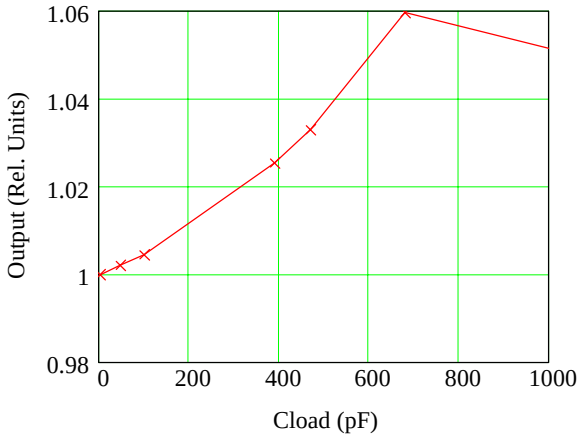


Output loading:

Resistive



Capacitive



ATLAS CSC Preamp/Shaper IC

Technology	0.5 μm CMOS
Channels	16
Die size	2.78 x 3.96 mm
Architecture	Single-ended
Intended Cdet	20 – 100 pF
Input device	NMOS W/L = 5000/0.6 μm, Id = 4mA
Noise	1140 + 17.6 e-/pF
Gain	3.8 mV/fC
Max. linear charge	450 fC
Class AB Output swing	To power supply - 250 mV
Pulse shape	7^{th} order complex Gaussian, bipolar
Pulse peaking time, 5% - 100%	73 ns
FW1%M	340 ns
Max. output loading (3% distortion)	500 Ω, 500 pF
Crosstalk	0.8% adjacent, 0.5% non-adjacent channel
Power supply	Single +3.3V
Power Dissipation	32.5 mW/chan

Planned future work

Test of modified SCA
- verify operation of new readout logic
- evaluate readout rate

First prototype ASM board:
- controller for modified SCA
- package for P/S
- chain test with detector at high rate beam

Radiation effects
- evaluate ASICs
- evaluate COTS components of ASM board

Data concentrator
- algorithm development and simulation
- partitioning, mechanics, interconnect

P/S second iteration prototype
- power dissipation
- configurable gain and peaking time

TTC and DCS interfaces

Faraday shield and cooling