

# Performance and Radiation Tolerance of the ATLAS CSC On-Chamber Electronics

Kurt Vetter

Brookhaven National Laboratory

<http://www.inst.bnl.gov/~vetter/>

Presented At LEB2000

Krakow Poland

September 13, 2000

# ***Outline***

## **1. System Overview**

- Chamber Configuration
- Signal Flow
- Signals and Noise
- High Rate Performance
- Pre-Amp/Shaper
- Sampling

## **2. ASML**

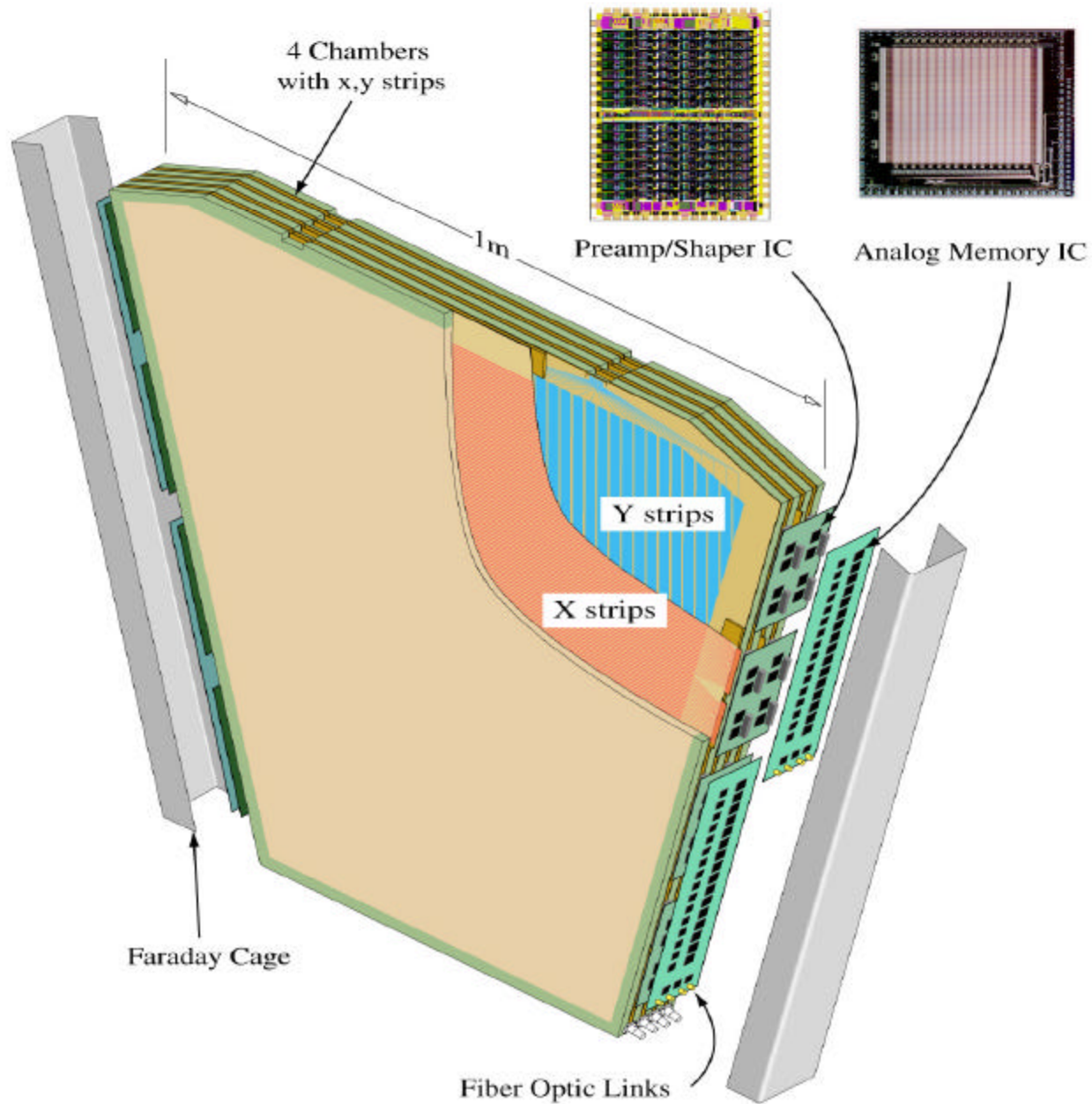
- Functionality
- Optical Links
- Data Transmission

## **3. Radiation**

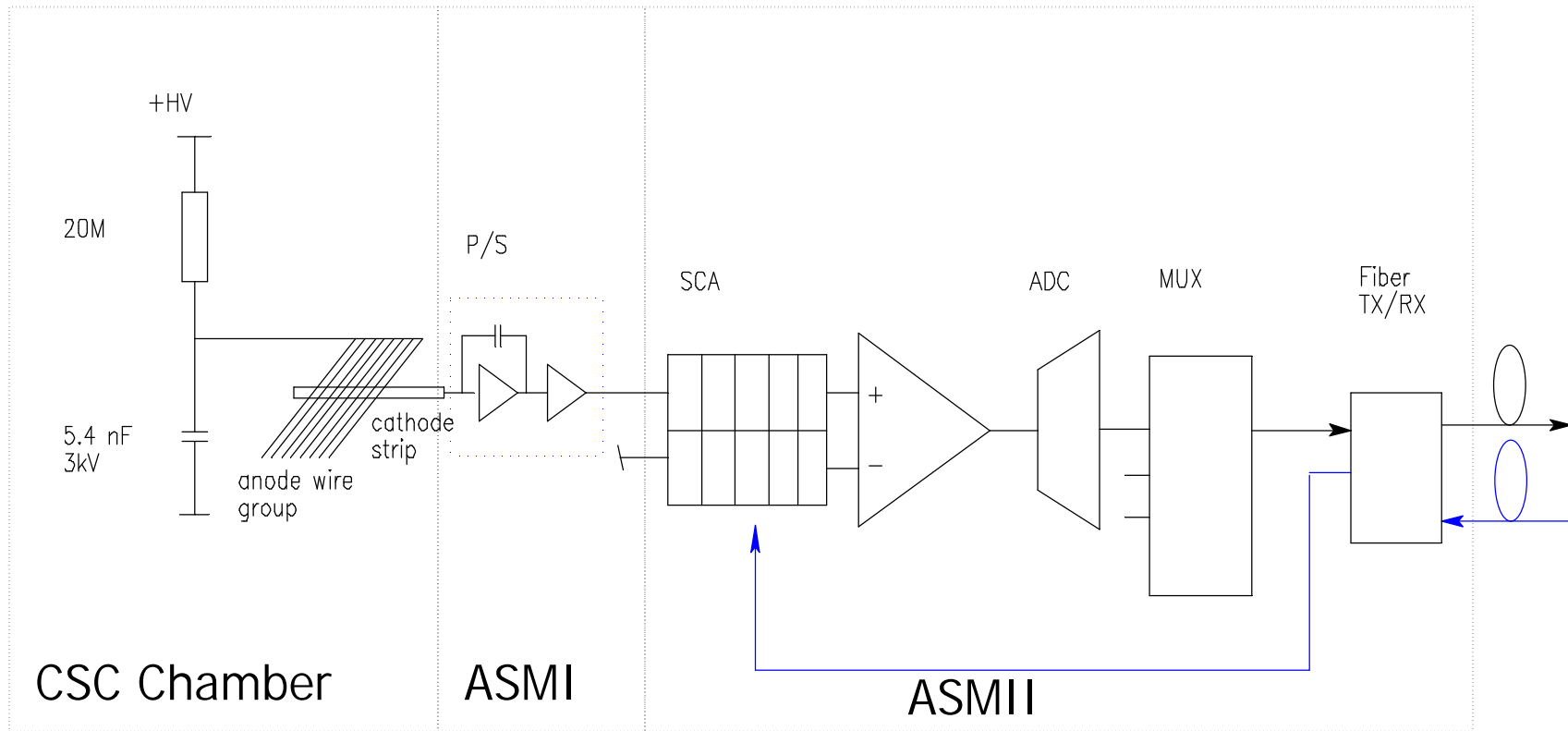
- Requirements
- Component Testing
- Test Plans

## **4. Summary**

# ATLAS CSC with Electronics



# Signal Processing Chain



# Signals and Noise

## 1. Chamber electrode Configuration

- 4 gas gaps
- 192 precision strips
  - Readout pitch = 5.547mm
  - Cstrip 20-50pf
- 48 Transverse strips (no interpolation)

## 2. Signal Size

- Muon generates 75 electron-ion pairs (Landau peak)
- gas gain  $\sim 10^5$
- 12% of charge is collected by the precision cathode in 100ns
- signal size  $\sim 900,000 e^-$  (144 fC)  $\approx Q_{\gamma}$
- central strip of cluster receives  $\sim 1/2$  of charge  $\Rightarrow 72$  fC ( $Q_{\gamma,cent}$ )

## 3. Noise

- Electronics noise shouldn't degrade position resolution

$$\sigma_{x,elec} \approx \frac{\sqrt{3} d \sqrt{ENC}}{Q_{\gamma}} \approx 33 \mu m$$

**ENC  $\approx 0.5$  fC  $\approx 3100e^-$   $\approx$  TOTAL input referred noise**

# Signals and Noise

## 4. Signal-to-noise

$$\text{Signal-to-noise (max. strip)} \approx \frac{Q_{\text{cent}}}{ENC} \approx \frac{72fC}{3100e^-} \approx 145$$

## 5. Dynamic Range and Gain (for 98.5% efficiency)

$$\frac{Q_{FS}}{Q_{\text{?}}} \approx 5$$

$$\text{? } Q_{FS} \text{ ? } 5 \text{ ? } Q_{\text{?}} \text{ ? } 725 \text{ ? } ENC \text{ ? } 360fC$$

## 6. Quantization

$$\frac{Q_{FS}}{2^{N_{\text{bits}}} \sqrt{12}} \approx ENC$$

$$2^{N_{\text{bits}}} \approx \frac{Q_{FS}}{\sqrt{12} \text{ ? } ENC} \approx 209$$

$$N_{\text{bits}} \approx 7.7$$

$$N_{\text{bits}} \approx 10 \text{ (} Q_{\text{quant}} \text{ ? } 20\% \text{ } ENC \text{) or } 12 \text{ (} Q_{\text{quant}} \text{ ? } 5\% \text{ } ENC \text{)}$$

*12-bits preferred to accommodate negative lobe, gain and offset variations*

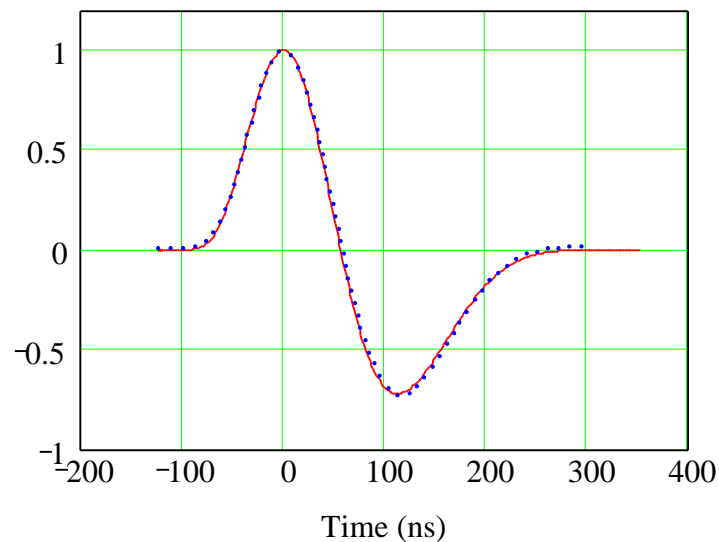
# High Rate Performance

- Overall background rate  $10^7$  Hz per chamber
- 50% charged particles, 50% neutron and ?
- Charged particle background is rejected by
  - timing window around trigger (out of time)
  - or by pattern recognition of non-projective tracks
- Neutrals can deposit high charges:
  - 50% of neutrals above  $Q_{FS}$
  - 1% of neutrals above  $6Q_{FS}$
- Neutrals produce short-range electrons usually confined to 1-layer
- But a neutral hit anywhere in chamber induces charge on all strips by anode-cathode crosstalk:

$$Q_{cross} \approx \frac{C_{ac}}{C_{filt}} Q_{anode} \approx 10^{24} Q_{anode}$$

# Pre-Amp Shaper

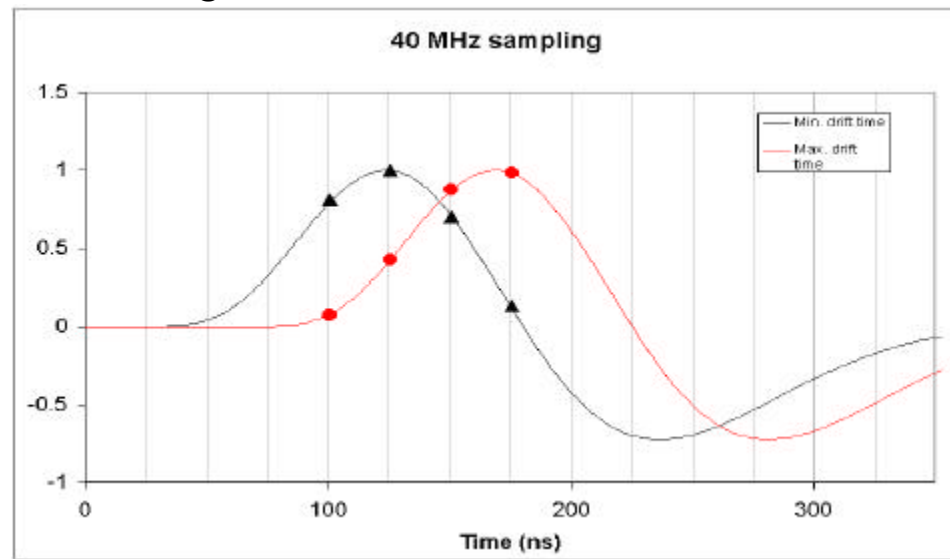
- Optimal pulse shaping is a compromise between noise, which degrades position resolution, and pileup which contributes to inefficiency.
- Bipolar pulse preferred in high-rate environment.
- From Monte Carlo study, peaking time should be  $\sim 100$  ns and  $FW1\%M < 430$  ns
- Bipolar 7<sup>th</sup>-order shaper using complex poles gives same return to baseline as 12<sup>th</sup>-order  $CR^2$ - $RC^n$  configuration
- Pulse Waveform



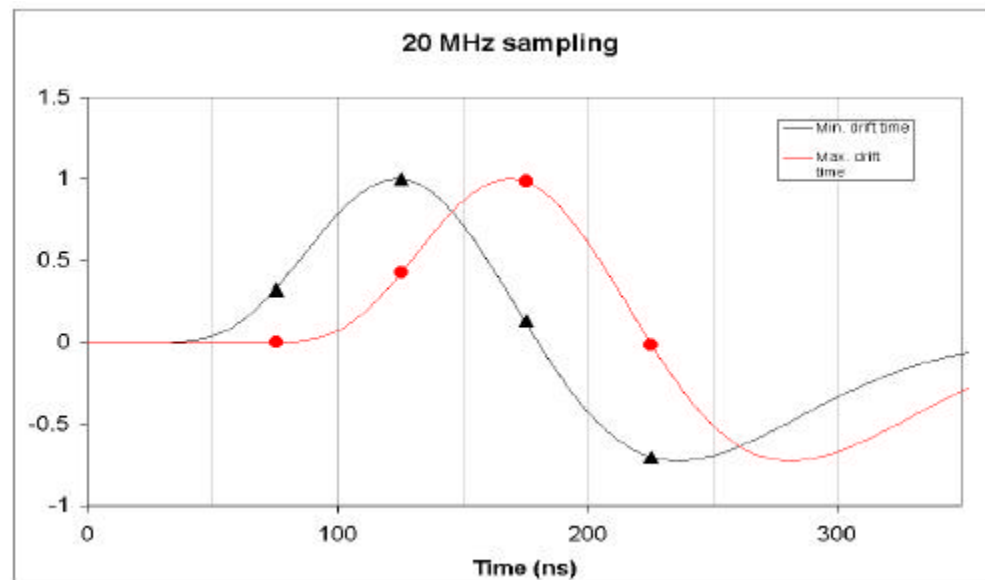


# Sampling Rate

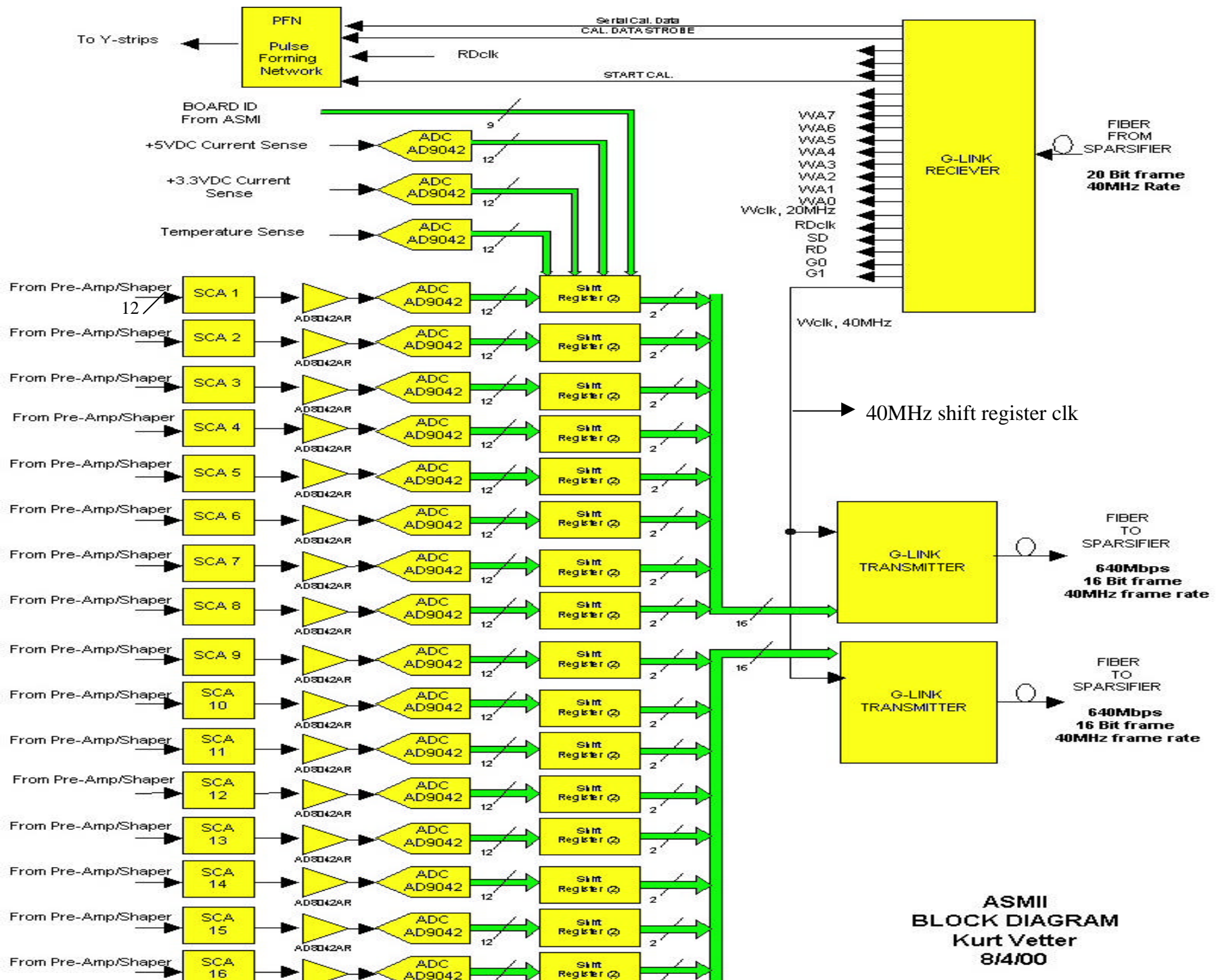
- With 40 MHz sampling and only 4 samples, we can't always get the peak and both neighbors



- 20 MHz sampling/4 samples gives a wider window and doesn't degrade the resolution or efficiency

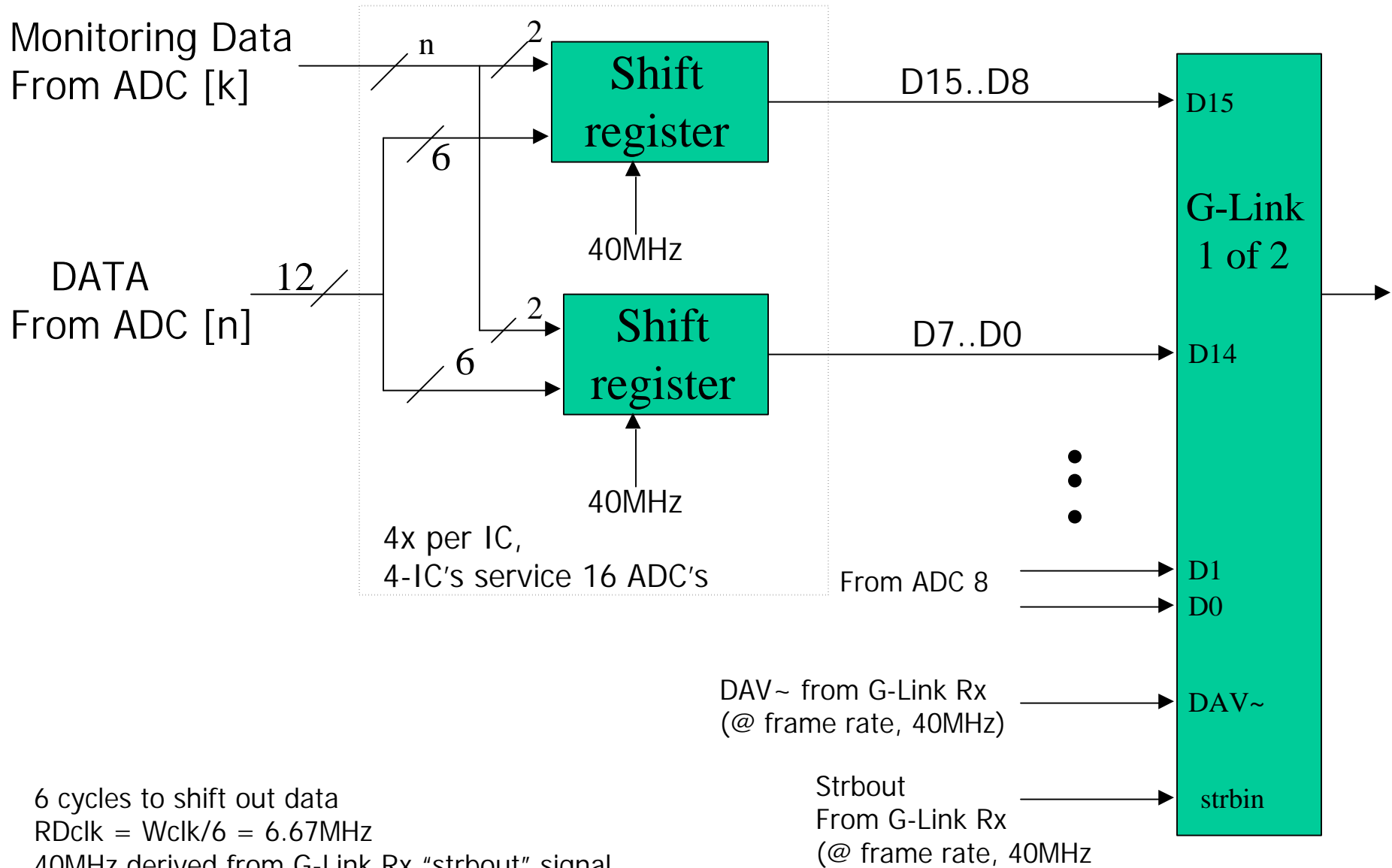


# ASMI Block Diagram

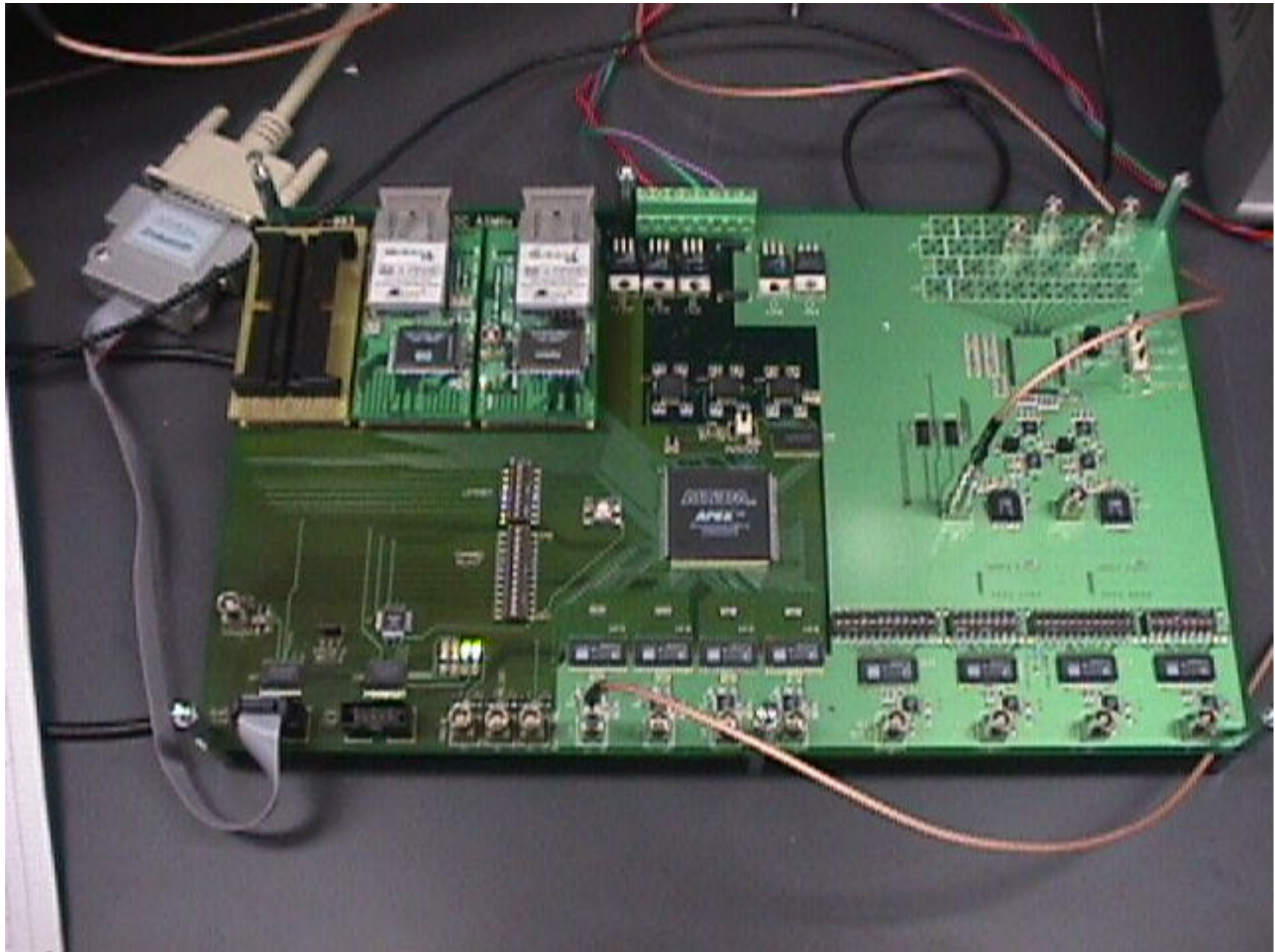


# Readout Implementation

2-Bits per ADC, Single Frame Mode  
(1 of 2 transmitter links shown)



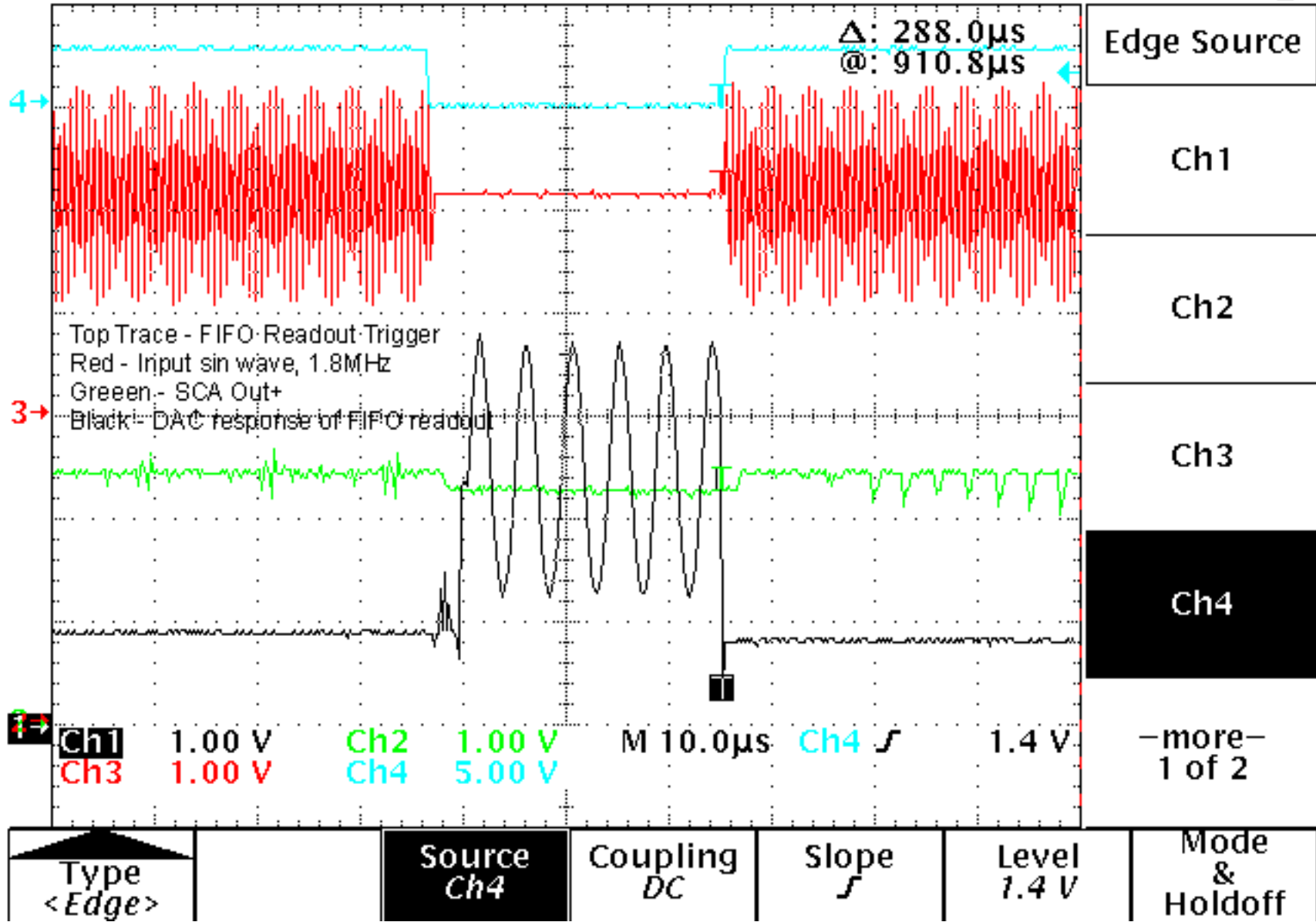
# ASMIa Prototype



# SCA Muon Mode Response

Tek Run: 5.00MS/s

Sample



# Optical Data and Control Links

- Two G-Link Transmitters
  - Transmit raw data quantized to 12-bits from SCA
  - 16 bit data field
  - 40MHz frame rate
- One G-Link Receiver
  - Provides SCA control
  - Provides Calibration data and control
  - 20 bit data field
  - 40MHz frame rate
  - 14 SCA control bits
  - Provides Frame Clock for G-Link Transmitters
- ADC Outputs Serialized into G-Link data field
  - Two serial lines per ADC, 6-bits deep
  - 40MHz serial data rate
  - 8 ADC's serialized into one G-Link Tx

# Data Transmission

- Buffer data for L1 latency in SCA (~2.5us, 50-cells at 20MHz)
- Transmit 4-time samples within L1 trigger rate of 100KHz
  - Must transmit 4-samples in less than 10us
  - One time sample corresponds to reading 12 SCA channels
  - 15 SCA READ CLK cycles required for one time sample
  - 4 time samples corresponds to 60 SCA READ CLK cycles
  - SCA READ CLK  $\geq$  6.67MHz (4-samples = 9us)
- Transmit On-Chamber current and temperature
  - Digitize current sense and temperature
  - Data fused into main data stream as serial bit stream
  - Readout controlled by sparsifier
- Transmit board identification (board ID).
  - Data fused into main data stream as serial bit stream.
  - ID set by on-board switches or links.

# CSC Radiation Requirements and Tolerance

- REQUIREMENTS
  - Ionizing dose of 4.4krad/yr
  - Neutron flux of  $7 \times 10^{12}$  n/cm<sup>2</sup>/yr
  - Converts to  $1.8 \times 10^{12}$  1-MeV equivalent n/cm<sup>2</sup>/yr
  
- Radiation Tolerance Criteria for SEU
  - In-efficiency = 0.1%
  - In-efficiency per G-Link =  $0.78 \times 10^{-6}$
  - Link down time = 1ms
  - # of chips per link = 2
  - Data dropped after recovery = 8-triggers
  - Link down probability per SEU = 100%
  - Acceptable SEU rate = 1 SEU per 43 minutes per chip

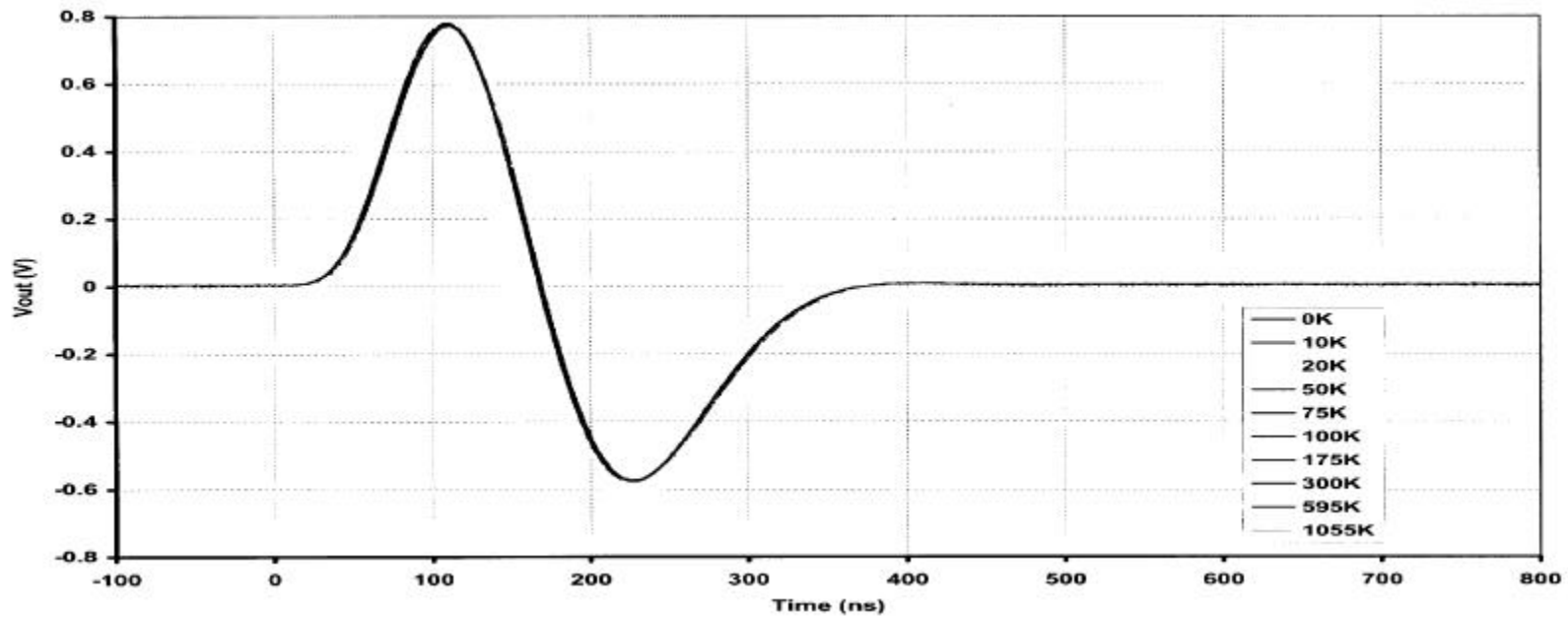


# On-Chamber Components

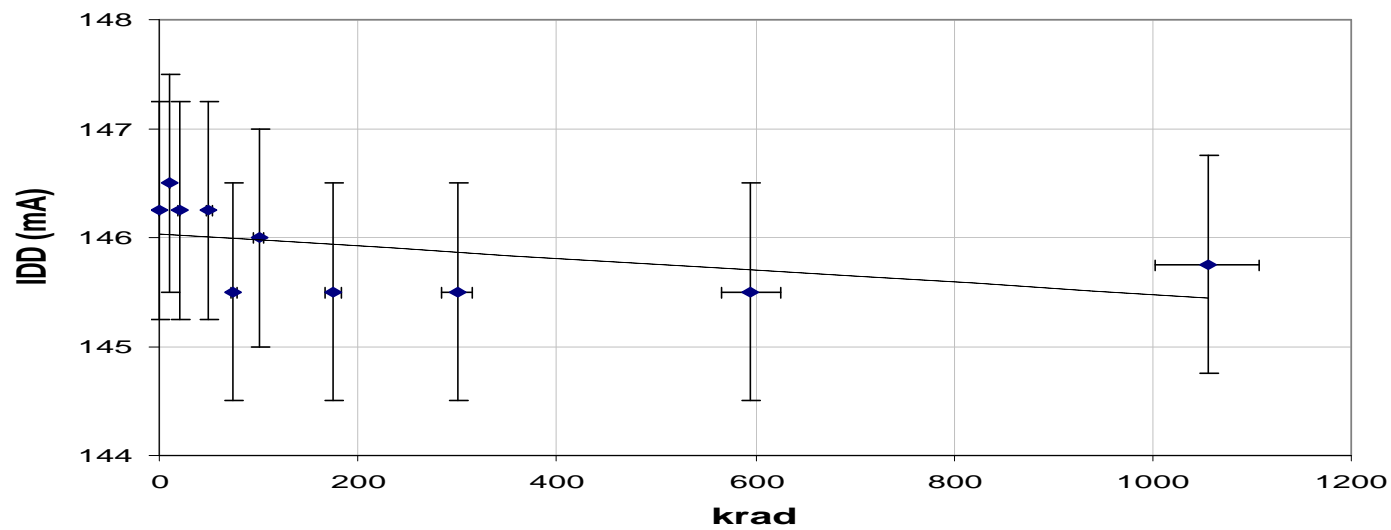
COMPONENT	COMMENTS
HDMP 1022	Extensive testing has been performed. Plan to conduct our own test.
HDMP 1024	Developing test hardware at UCI
SCA	Testing to be completed by LAr.
AD9042 (ADC)	Used on LAr FEB. Extensive testing performed by Denes at Princeton.
AD8042 (op-amp)	Used on LAr FEB. Ionizing survival test done by Lar.
Level Translators MC10H116	No testing done to date.
DAC?	Trying to develop alternate solution for 0.5% required calibration pulse accuracy.
74ALS166	COTS Qualification
Pre-Amp/Shaper	Passed ionizing test.
ASMI/ASMI I	Test final ASMI I under Sparsifier control. <i>Does anything unexpected happen?</i>

# Preamp Shaper Irradiation Results

0.5um CMOS HP

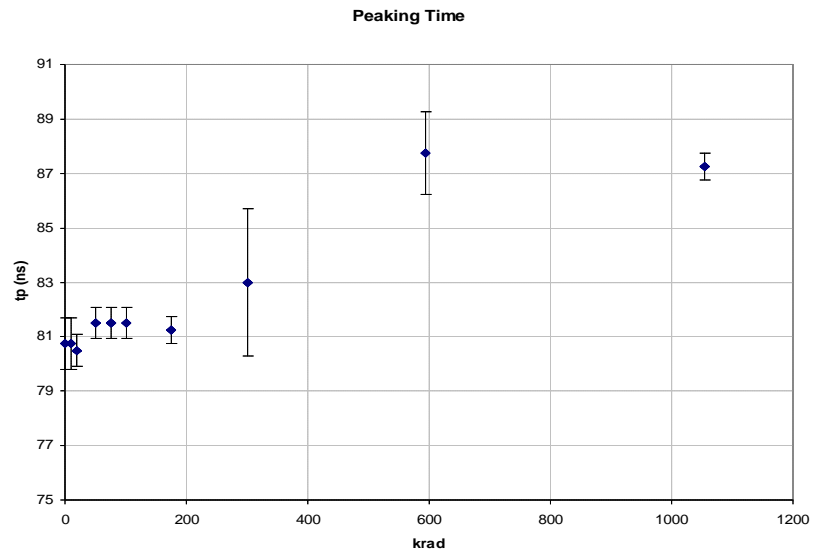
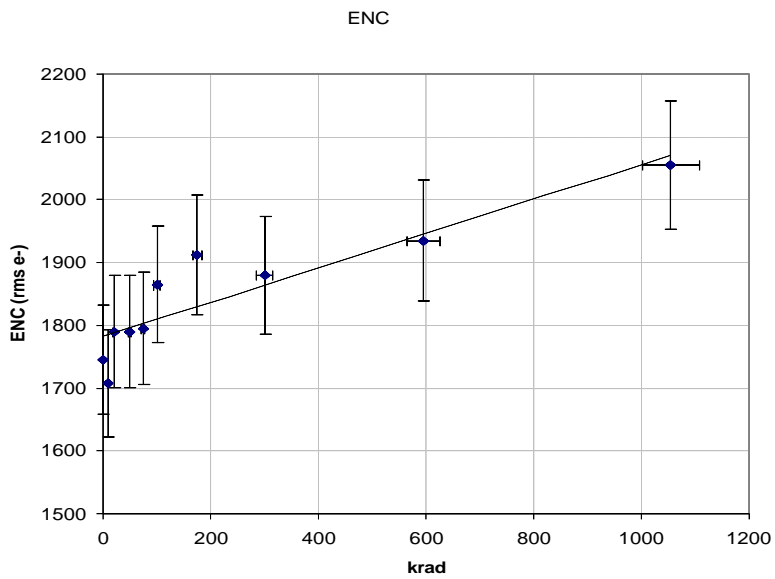
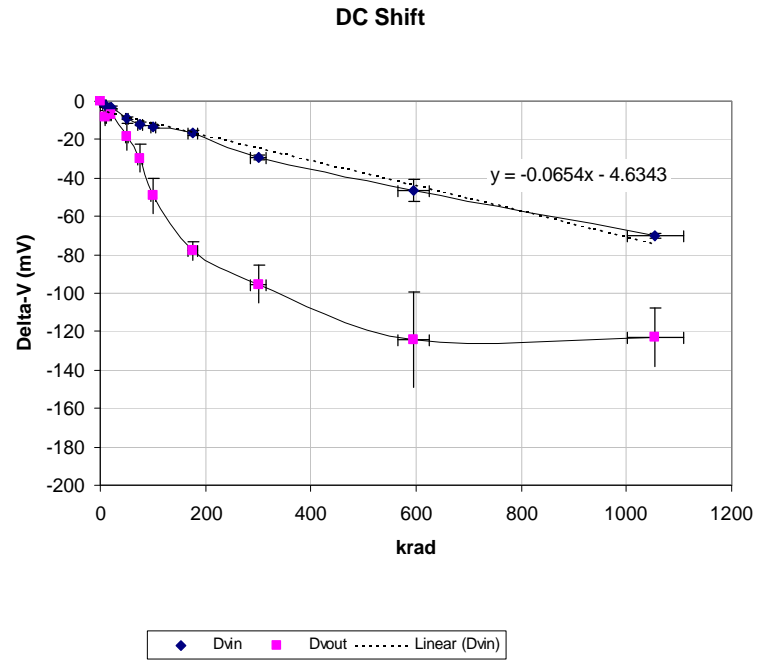
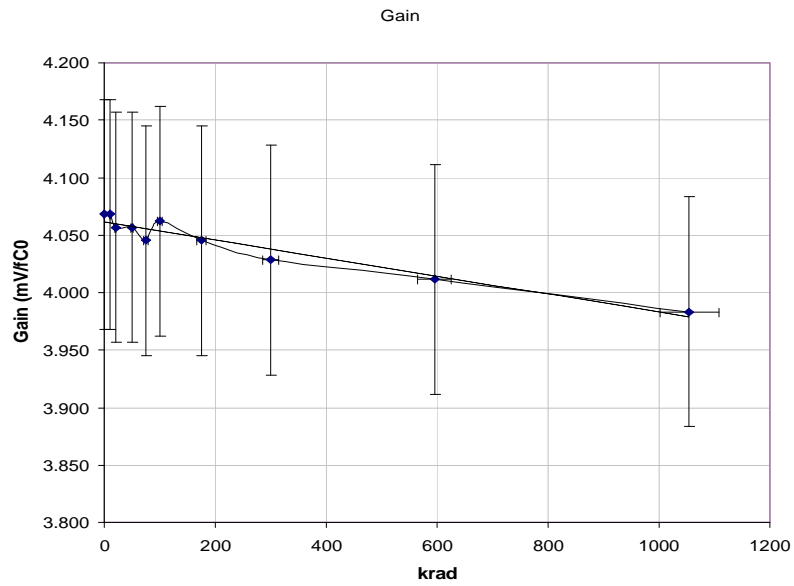


## IDD



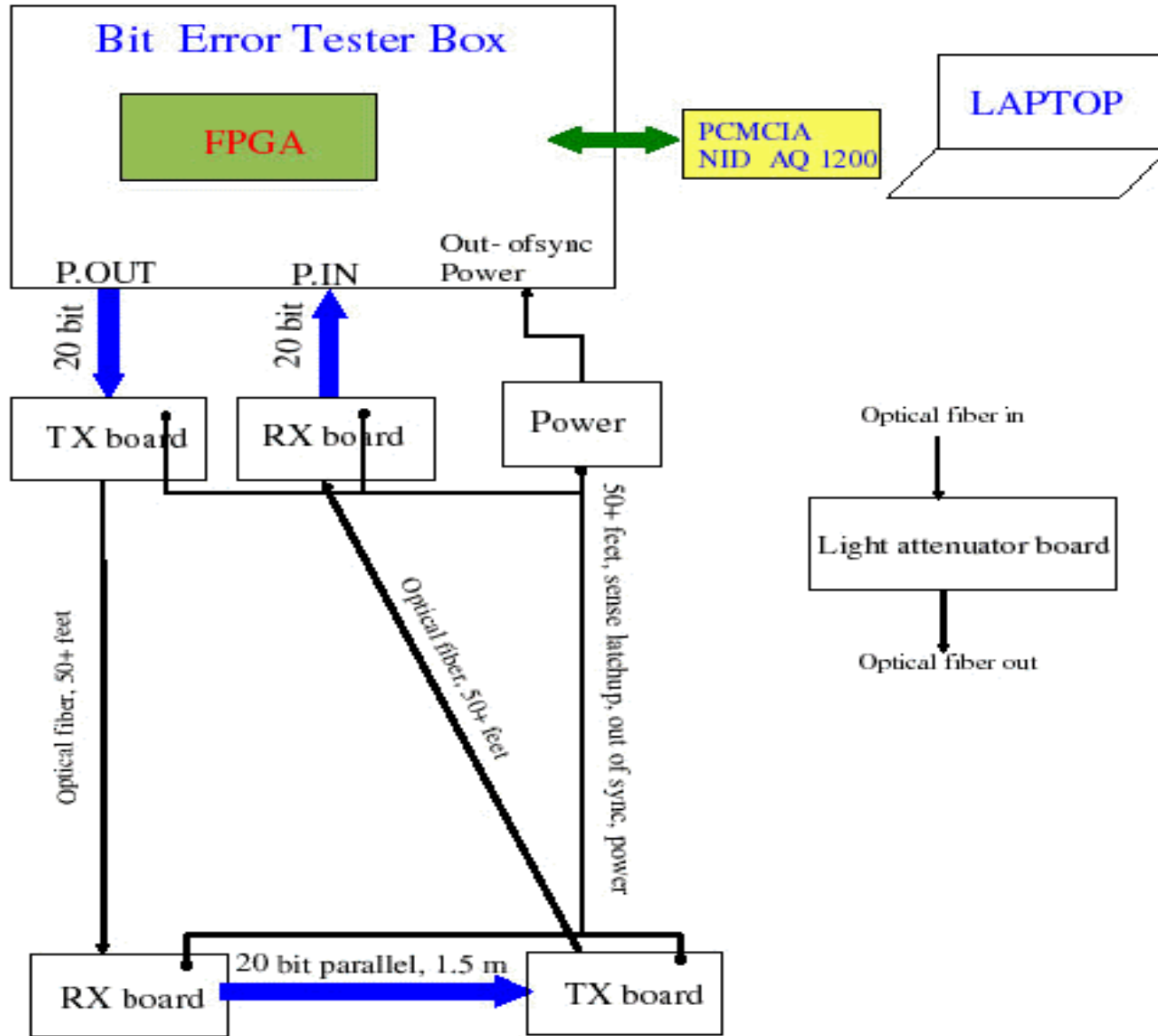
# Preamp/Shaper Irradiation Results

## 0.5um CMOS HP



# G-Link Receiver Test

SEU TEST SETUP BLOCK DIAGRAM



# Summary and the Road Ahead

1. Minimize SEU problem by moving SCA control logic off-chamber
2. Developed 24-channel prototype ASMLII to verify SCA Muon Mode
3. Beam test data verified performance of Preamp/Shaper and 20MHz sampling
4. Developed VME DAQ board to support beam test of front end electronics
5. Preamp/Shaper passed Ionizing radiation test to 1Mrad
6. G-Link Receiver and Transmitter boards have been built
7. Characterize G-Link Receiver for Ionizing and Neutron radiation by Dec. 2000
8. More detailed testing of SCA Muon mode required
9. Plan to develop full 192-channel ASMLII within next few months
10. Beam test complete on-chamber electronics prototypes in spring of 2001
11. Evaluate cooling approach
12. Coordinate radiation test and qualification efforts with LAr and UCI