Impact of Technology Scaling on Low Noise Front End Circuits

Paul O'Connor, Brookhaven National Laboratory

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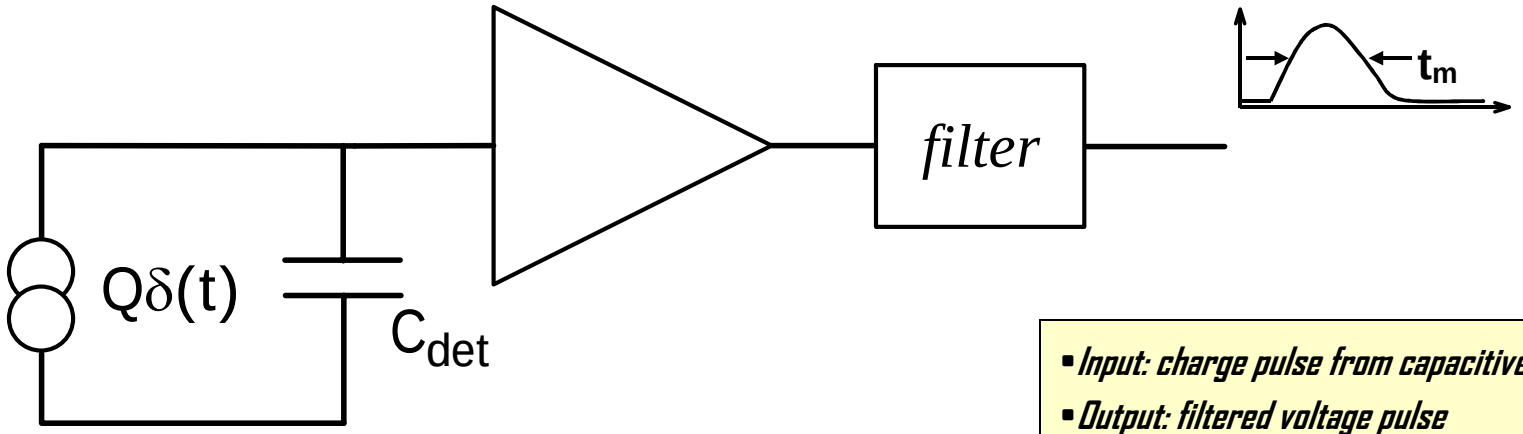
Charge preamplifier/shaper as detector front end

- Low noise is critical for many experiments
  - *Ageing of gas detectors*
  - *Fast, inefficient scintillators*
  - *Thin semiconductors for tracking*
  - *Position determination by interpolation*
  - *Particle ID by dE/dx*



- *Input: charge pulse from capacitive source*
- *Output: filtered voltage pulse*
- *System noise is dominated by the input transistor*

Outline

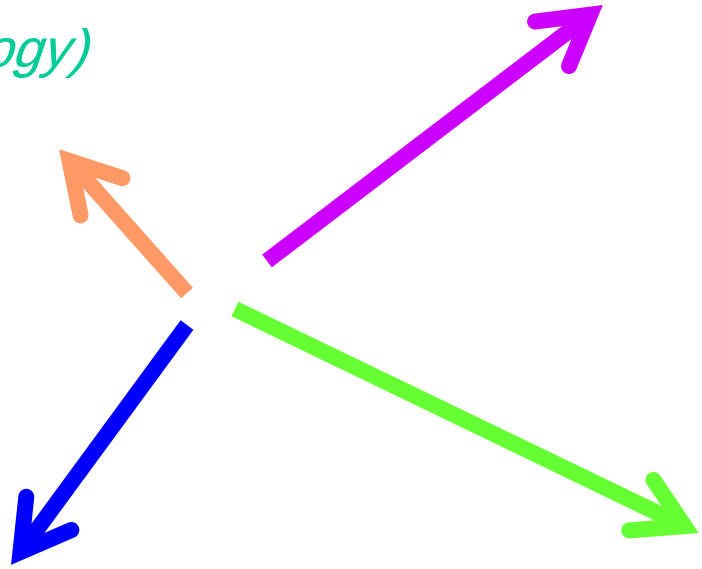
- Low noise analog design in monolithic CMOS
  - *Preamplifier design*
  - *Shaping amplifier*
- Circuit examples
- MOS Scaling and CSA design
  - *Noise mechanisms in scaled devices*
  - *Optimum capacitive match to detector*
  - *Noise, dynamic range, and power vs. scaling length*
- Interconnect issues
  - *Detector-to-preamplifier*
  - *Front end-to-ADC*

Low Noise Analog Design

MOS Charge Amplifier Design

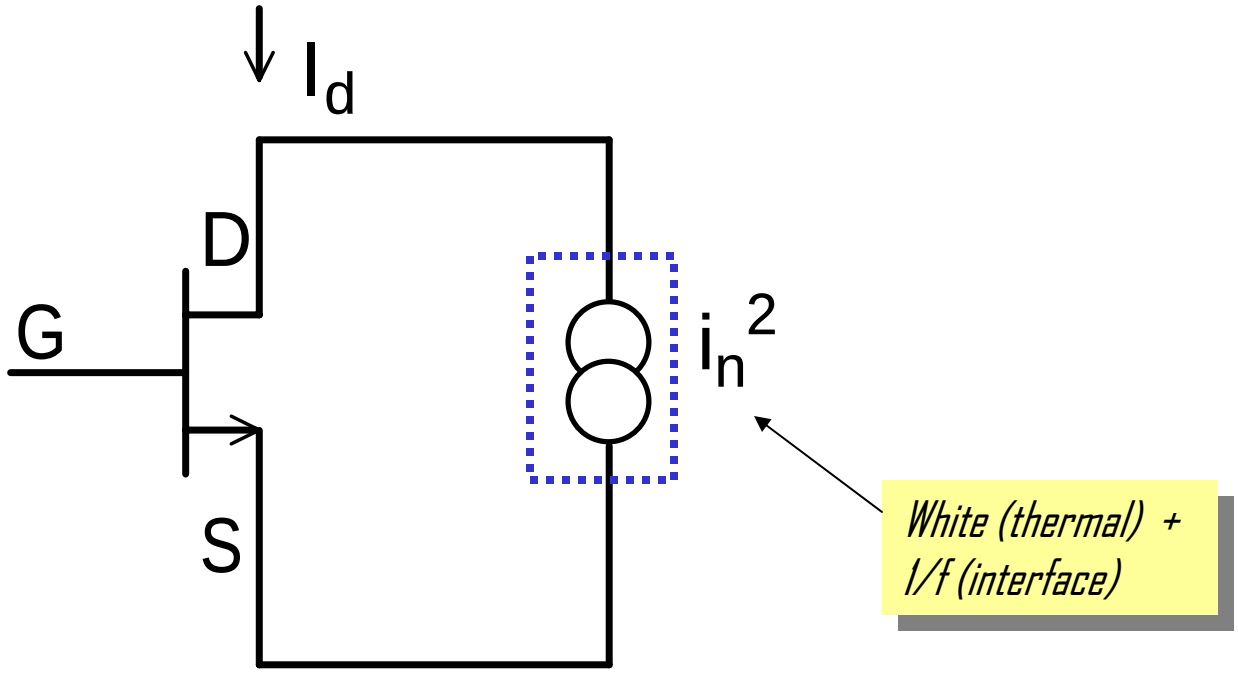
- Key parameters:
  - C_{det} , I_{det} , Q_{max} *(detector)*
  - *Rate,* P_{diss} *(system)*
  - f_T , K_F , I_{in} *(technology)*

- Key design decisions
  - C_{gs}/C_{det}
  - *Reset system*
  - *Weighting function*

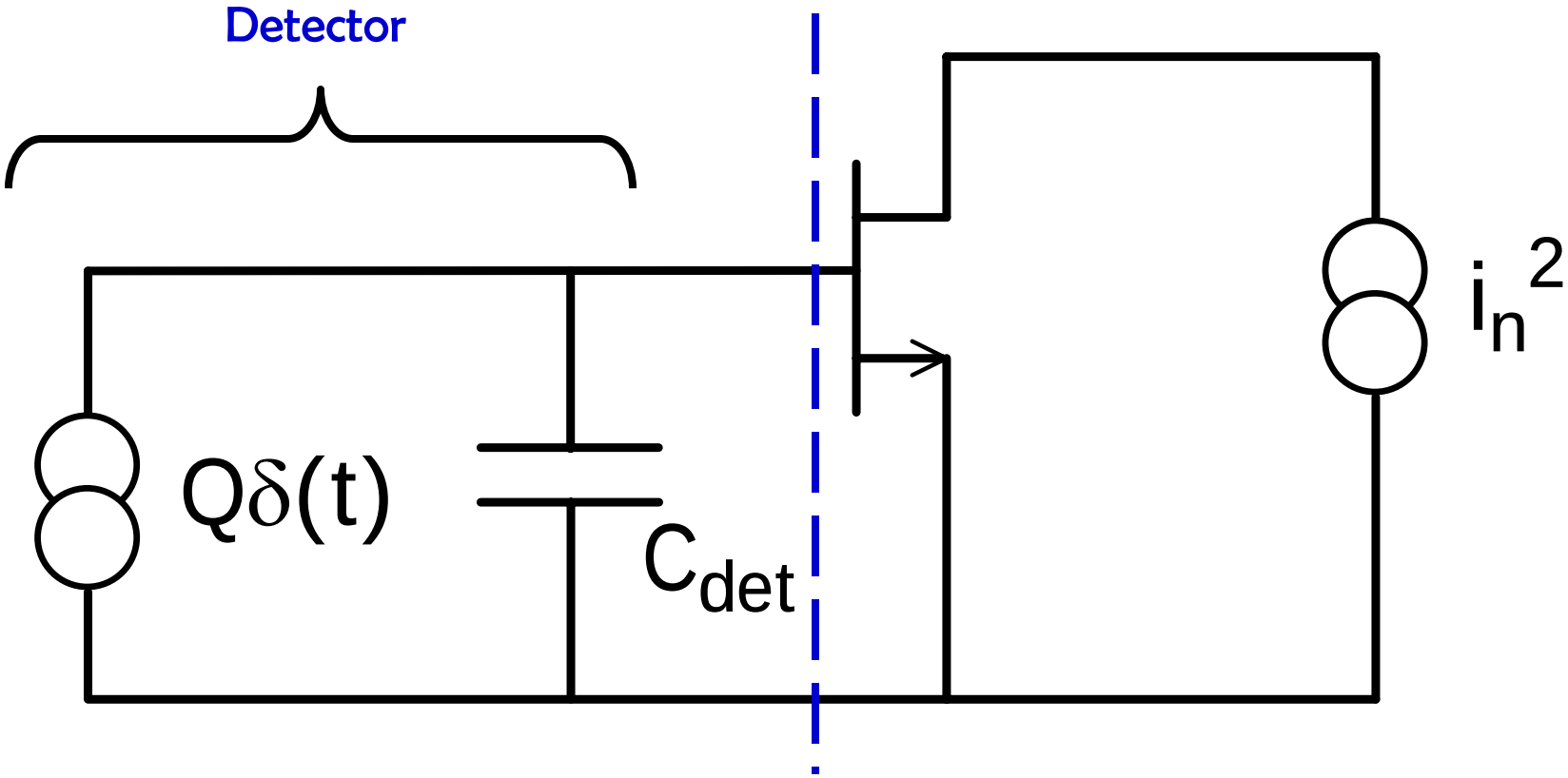


MOSFET Channel Thermal Noise

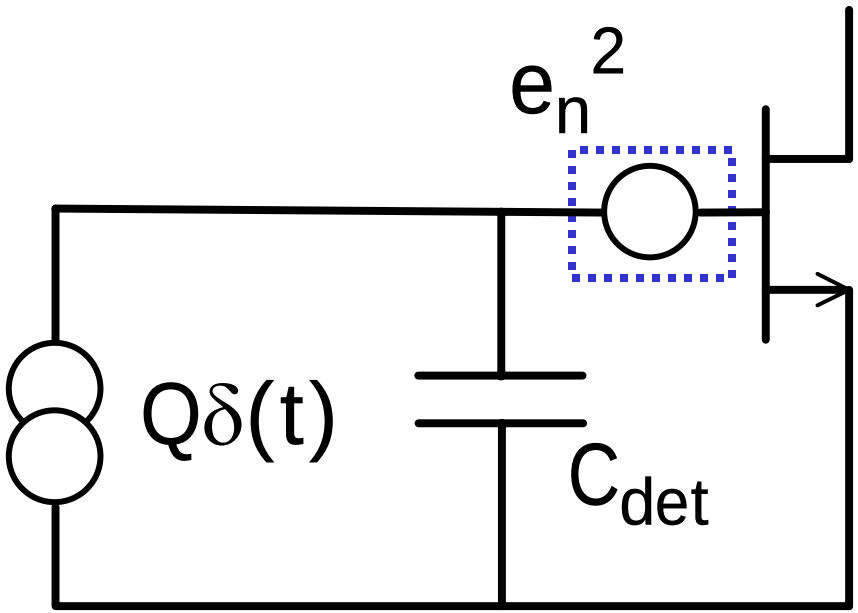
- Drain current and its fluctuation:



MOSFET connected to detector

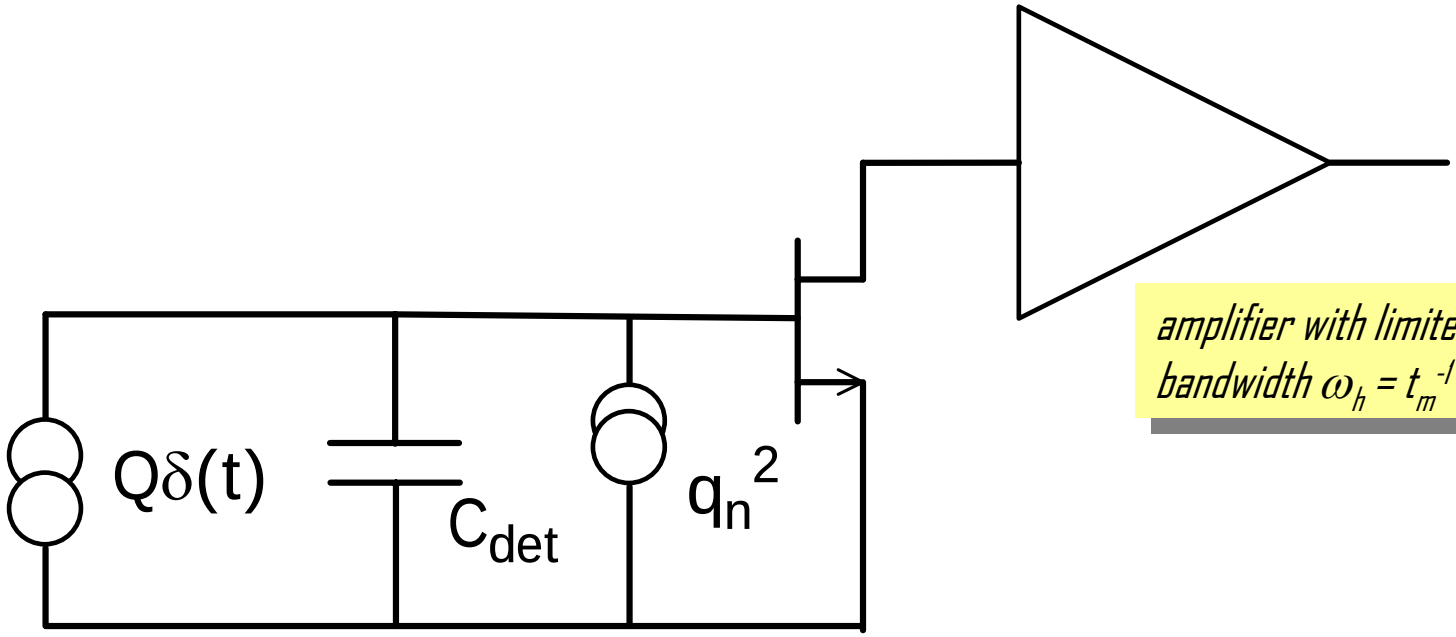


Transform noise to input



$$e_n^2 = \frac{4kT\gamma}{g_m} + \frac{K_F}{C_{gs} f}$$

Equivalent input noise charge



amplifier with limited bandwidth $\omega_h = t_m^{-1}$

$$ENC^2 = \left(\frac{4kT}{g_m t_m} + \frac{K_F}{C_{gs}} \right) C_{in}^2$$

Device sizing for minimum ENC

- Increasing MOS size decreases noise sources while increasing transistor contribution to C_{in}

$$ENC^2 = \left(\frac{4kT}{g_m \cdot t_m} + \frac{K_F}{C_{gs}} \right) C_{in}^2$$

$$C_{in} = C_{gs} + C_{det}$$

=> optimum transistor size for series white and 1/f noise:

$$C_{gs,sw,opt} = \alpha_{sw} C_{det}$$

$$C_{gs,1/f,opt} = \alpha_{1/f} C_{det}$$

Optimized ENC

- Transistor cutoff frequency $g_m = C_{gs} \cdot \omega_T = C_{gs} / \tau_{el}$

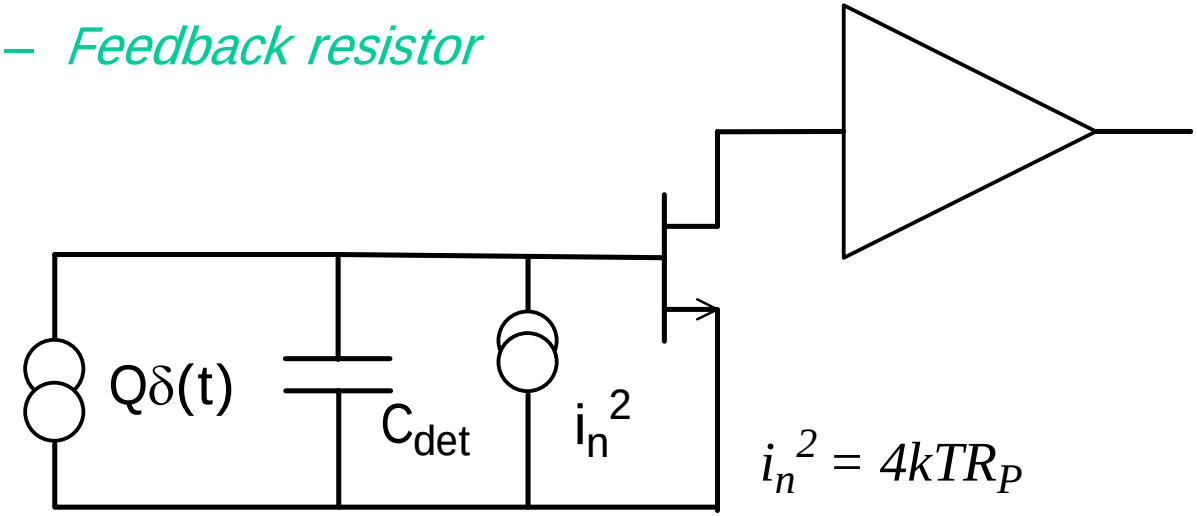
$$ENC_{sw,opt} \approx \sqrt{kTC_{det}} \sqrt{\frac{\tau_{el}}{t_m}}$$

$$ENC_{1/f,opt} \approx \sqrt{K_F C_{det}}$$

- Key ingredients for low ENC:
  - *low C_{det}*
  - *long t_m*
  - *short τ_{el}*
  - *Low K_F*

Parallel noise

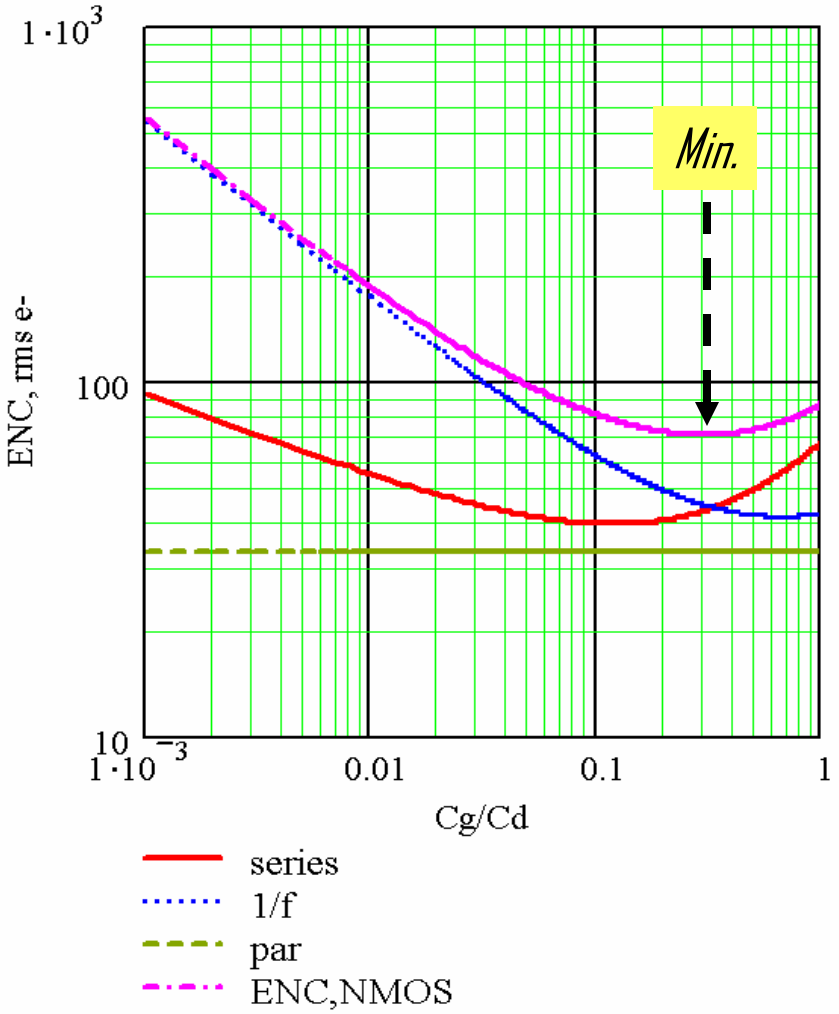
- From any noise current source connected to input:
  - *Detector biasing resistor*
  - *Shot noise of detector leakage current*
  - *Feedback resistor*



$$ENC_{par} = \sqrt{\frac{4kTt_m}{R_p}}$$

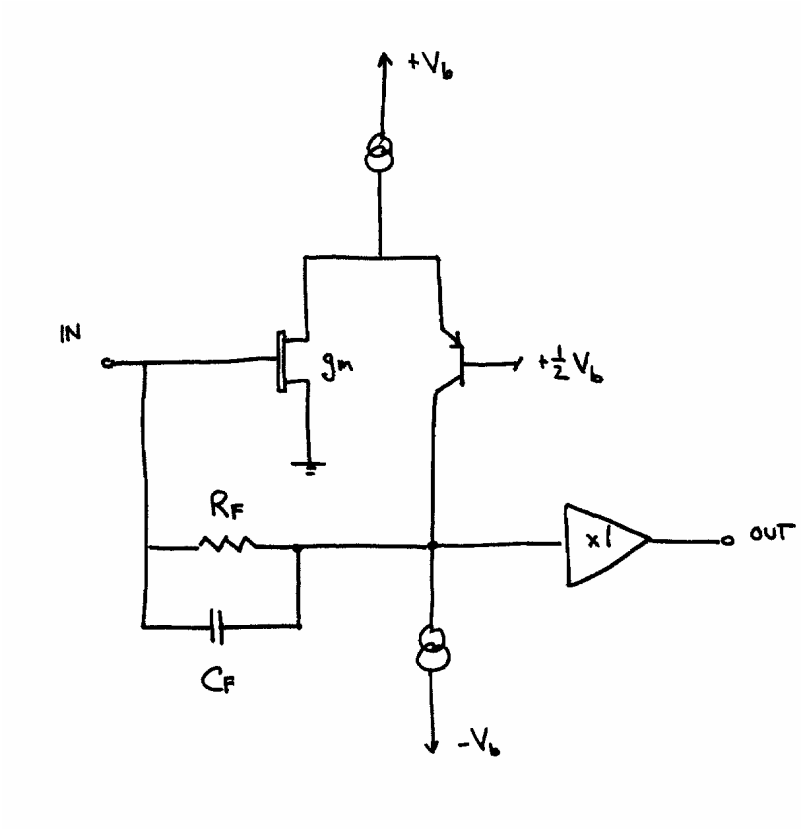
Capacitive matching – composite noise

- C_{det} = 3 pF
- t_m = 1 μs
- P_{diss} = 1 mW
- I_{leak} = 100 pA
- Technology: 0.35 μm NMOS

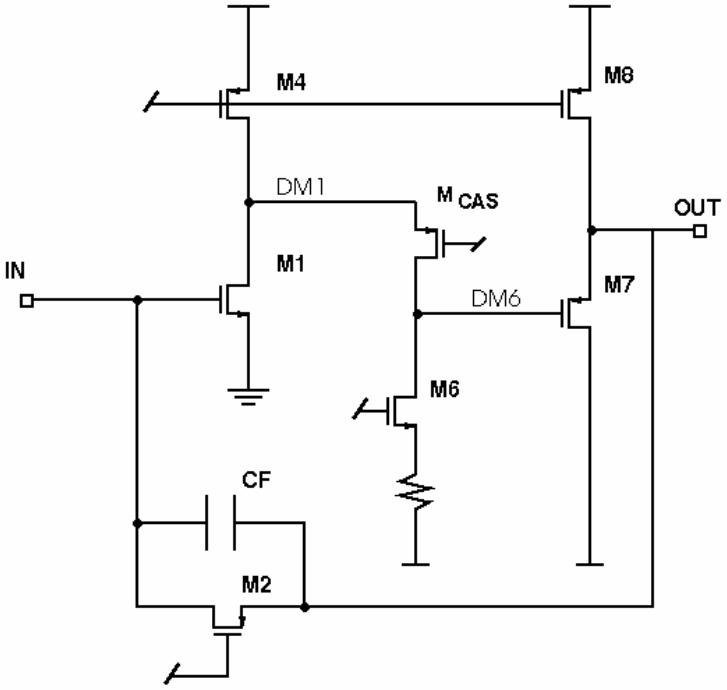


Basic Charge Amplifier

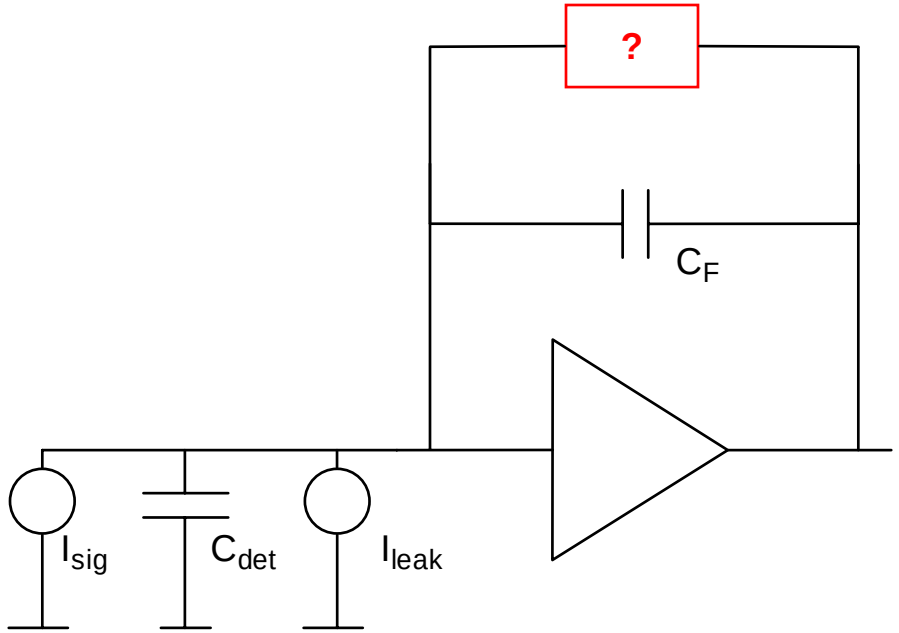
Configuration based on discrete/hybrid design



CMOS implementation

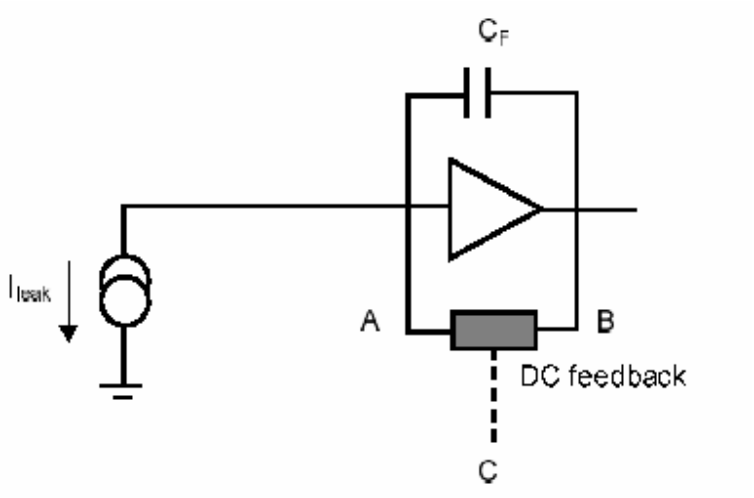


Preamp Reset – Requirements



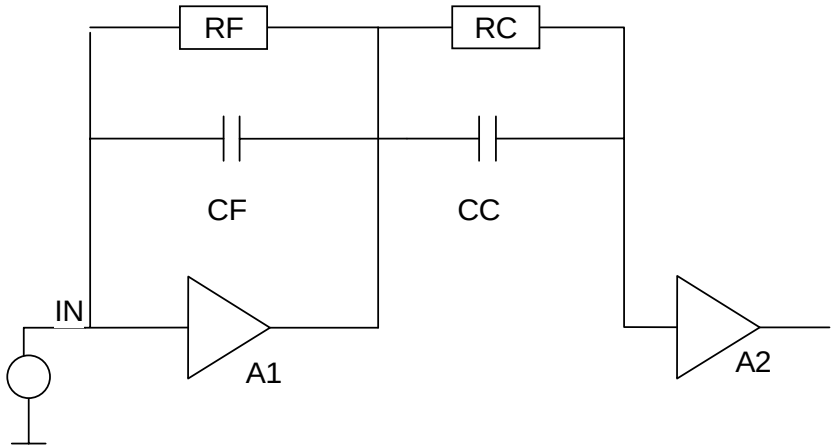
- all charge preamplifiers need DC feedback element to discharge C_F
- usually, a resistor in the MΩ – GΩ range is used
- monolithic processes don't have high value resistors
- we need a circuit that behaves like a high resistor and is also
  - *insensitive to process, temperature, and supply variation*
  - *low capacitance*
  - *lowest possible noise*
  - *linear*

Preamp Reset – Configurations

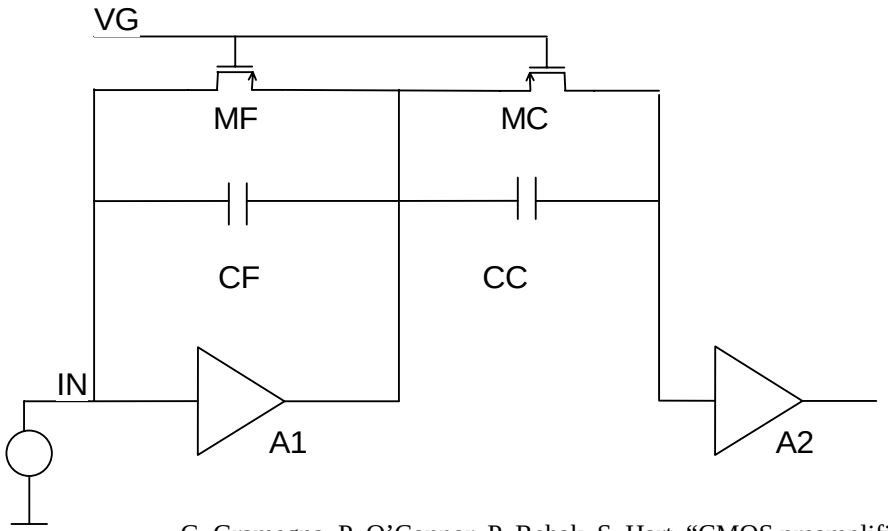


Feedback type	Circuit	R_{eff} (I_{leak} =0)	Advantages/ Disadvantages
Physical resistor	A –WW– B	R	+ simple - hard to make large R - parasitic C - doesn't adjust to I_{leak}
MOS switch	A B C(pulse)	$\frac{1}{C_F \cdot f_{reset}}$	+ simple - dead time - switch noise
Triode MOS	A B C Bias	$\frac{1}{\beta \cdot (V_{gs} - V_T)}$	+ compact + adjusts to I_{leak} - nonlinear
Feedback g_m	A B g_m C (Vref)	$\frac{1}{g_m}$	+ adjusts to I_{leak} - complex - excess noise - nonlinear
Attenuating current mirror	A B A_i<<1	$\frac{R}{A_i}$	+ aux. output for PZC - doesn't adjust to I_{leak}

Nonlinear Pole-zero Compensation



- Classical
  - *RF · CF = RC ·CC*
  - *Zero created by RC,CC cancels pole formed by RF, CF*



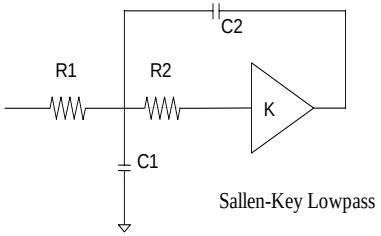
- IC Version
  - *CC = N · CF*
  - *$(W/L)_{MC} = N \cdot (W/L)_{MF}$*
  - *Zero created by MC, CC cancels pole formed by MF, CF*
  - *Rely on good matching characteristics of CMOS FETs and capacitors*

G. Gramegna, P. O'Connor, P. Rehak, S. Hart, "CMOS preamplifier for low-capacitance detectors", NIM-A 390, May 1997, 241 – 250.

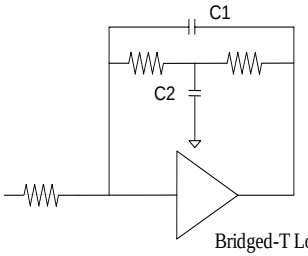
Integrated Shaping Amplifiers

- Limits the bandwidth for noise
- Gives controlled pulse shape appropriate for rate
- Control baseline fluctuations
- Bring charge-to-voltage gain to its final value
- By its saturation characteristics, sets upper limit on Q_{in}
- Feedback circuits give the most stable and precise shaping
  - *At the expense of power dissipation*
  - *Poor tolerance of passives limits accuracy of the poles and zeros*
- High-order shapers give the lowest noise for a given pulse width

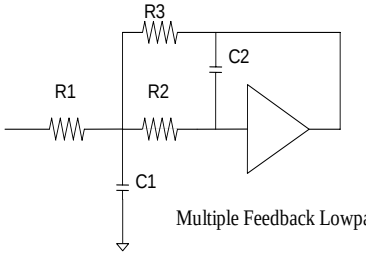
Filter topologies



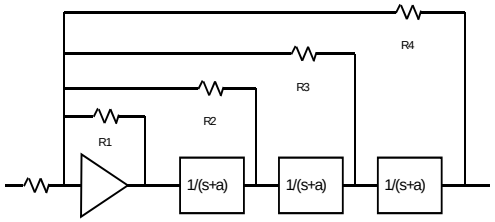
Sallen-Key Lowpass



Bridged-T Lowpass

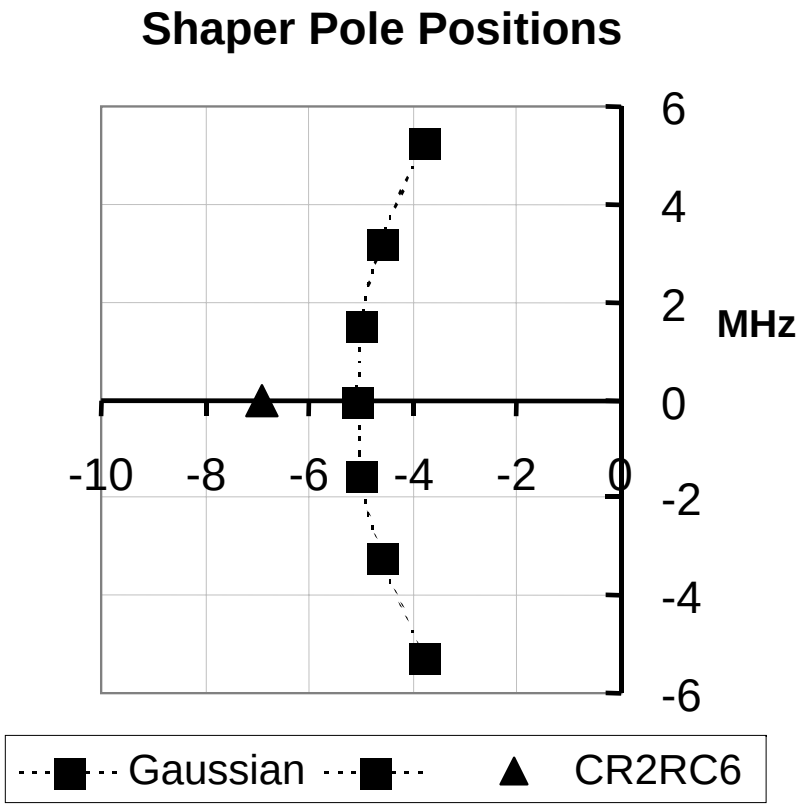


Multiple Feedback Lowpass



Follow-the-leader

Complex pole approximation to Gaussian pulse



Ohkawa synthesis method (Ohkawa, NIM 138 (1976) 85-92, "Direct Syntheses of the Gaussian Filter for Nuclear Pulse Amplifiers")

For given filter order, gives closest approx. to a true Gaussian

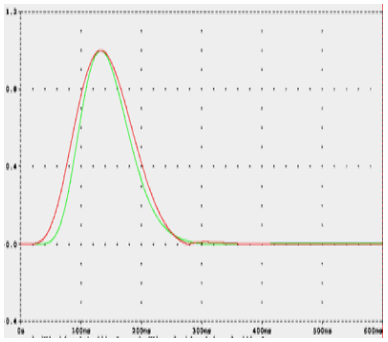
More symmetrical than CR-RC^n filter of same order for same peaking time

Noise weighting functions:

$I_{1,complex}/I_{1,CR-RC} = 1.18$ **series**

$I_{2,complex}/I_{2,CR-RC} = 0.81$ **parallel**

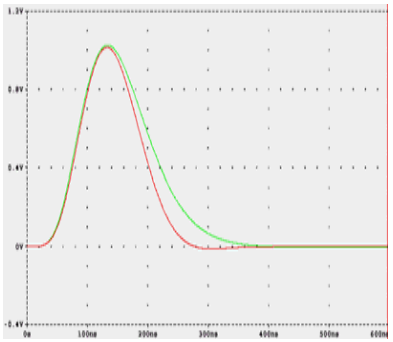
Complex shapers: advantages



7th order complex

12th order CR-RC^n

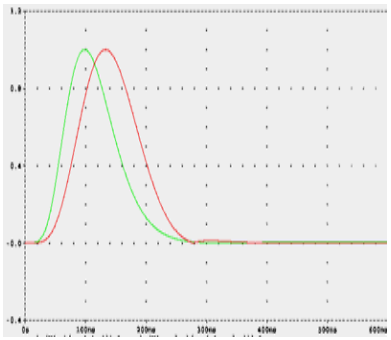
Equal peaking times, equal 1% widths



7th order complex

7th order CR-RC^n

Equal peaking times, equal order



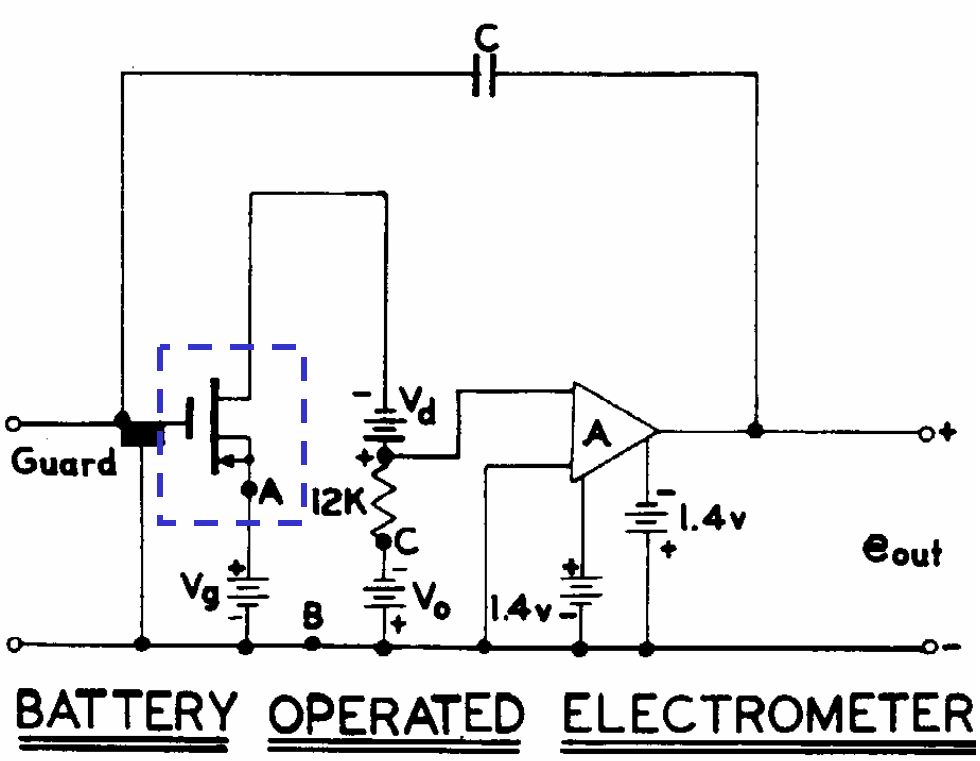
7th order complex

7th order CR-RC^n

Equal 1% widths, equal order

Examples

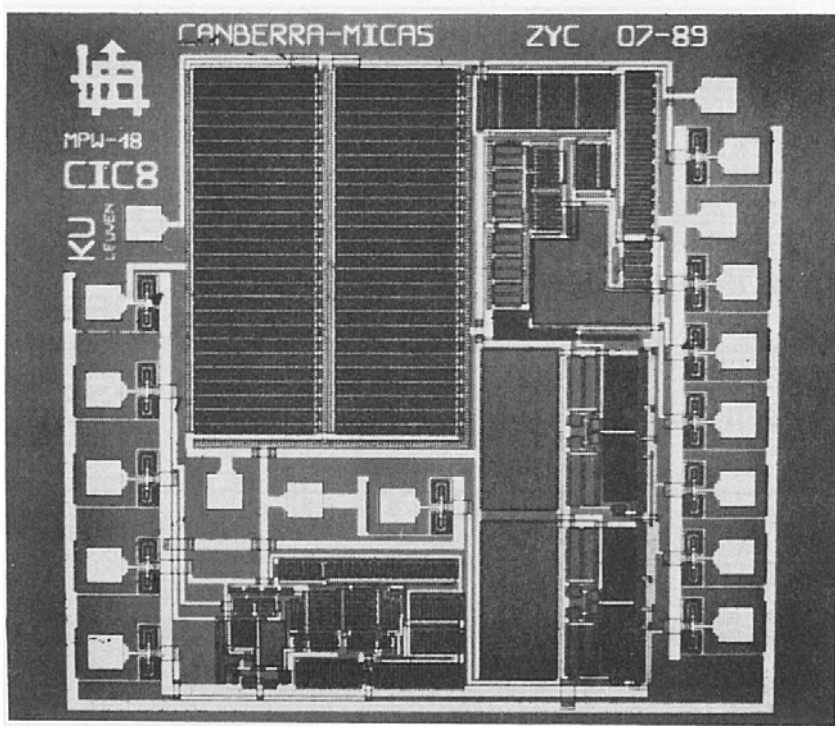
Charge Amplifier based on Silicon MOSFET (1967)



V. Negro et al., “A Guarded Insulated Gate Field Effect Electrometer”, IEEE Trnas. Nucl. Sci. Feb. 1967, 135 – 142

J.B. McCaslin, “A Metal-Oxide-Semiconductor Electrometer Ionization Chamber”, UCRL-11405 (1964)

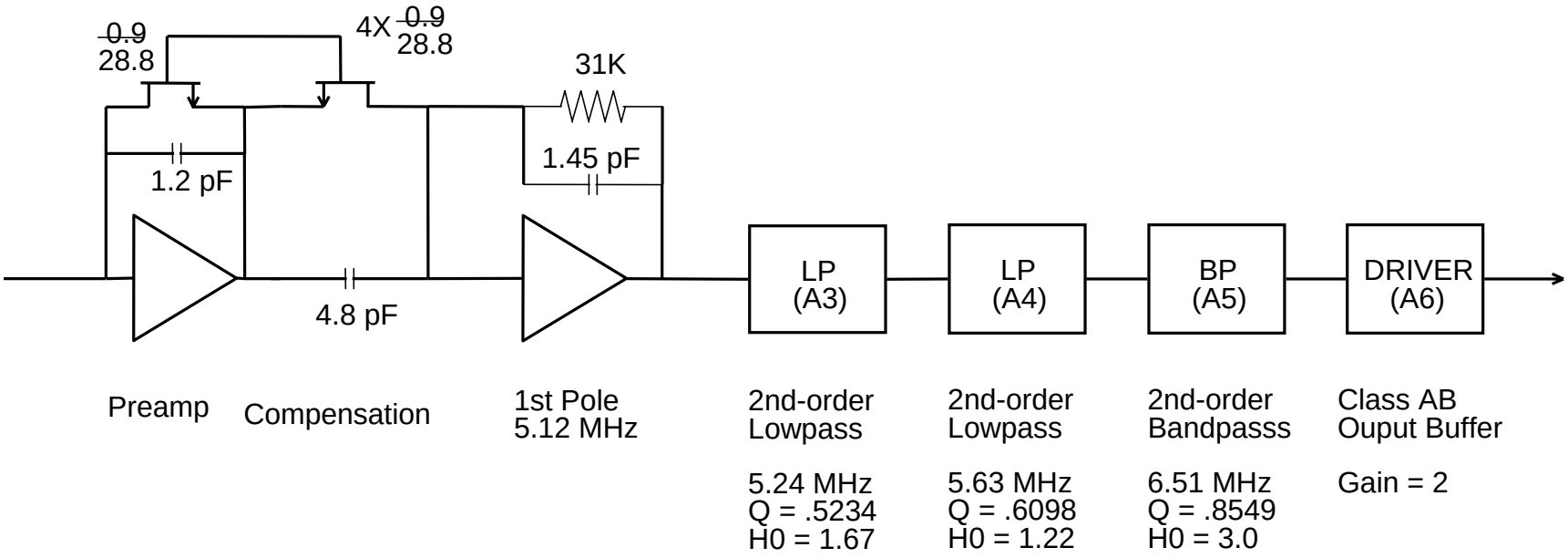
Spectroscopy amplifier (1989)



Technology	3.0 μm CMOS
Power Supply	+/- 5V
Chip size	2.5 x 2.5 mm
Channels	1
C_{det}	300 - 1000 pF
Reset	external resistor
Shaping	CR-RC^4, 1.6 μs
ENC	3800 + 4.1 e^-/pF
Power dissipation	96 mW

Z. Chang, W. Sansen, *Low-Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies*, Kluwer 1991 Ch. 5

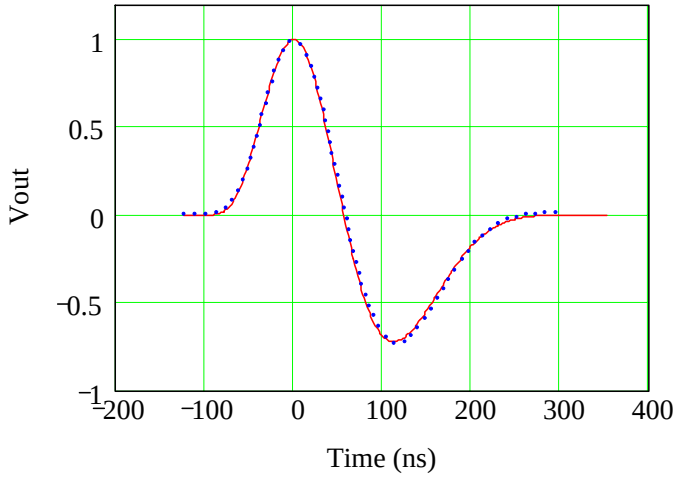
Preamp-shaper for cathode strip chamber

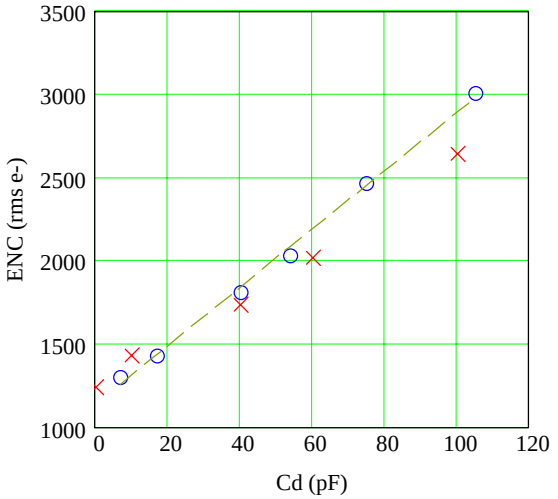


- Detector: cathode strips of 0.5m MWPC with 50 pF C_{DET}
- Charge interpolation to 1/100 of the strip pitch
- Fast (70 ns), 7^{th} order bipolar shaping for charged particle tracking in high rate environment

Preamp-shaper for cathode strip chamber

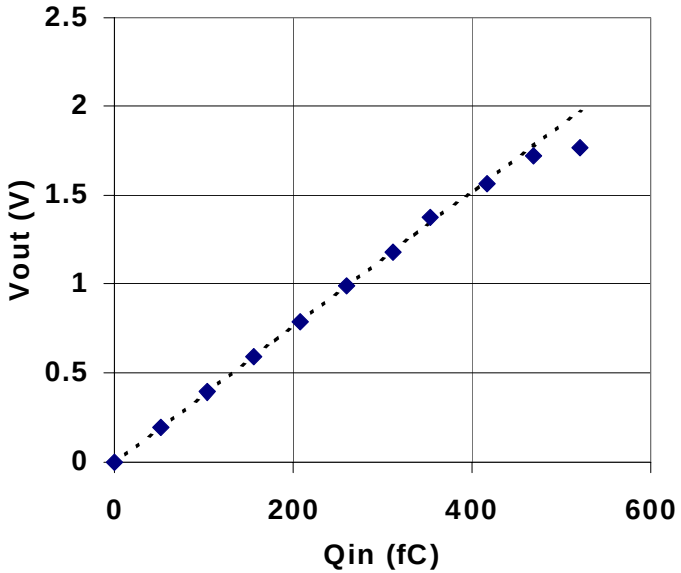
Pulse Shape simulated (solid red line) and measured (blue dotted line)

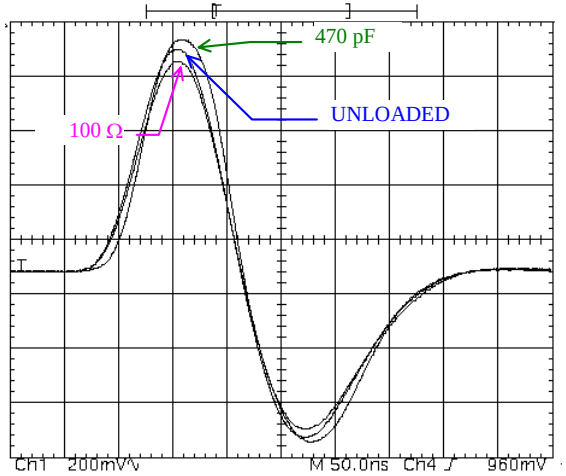




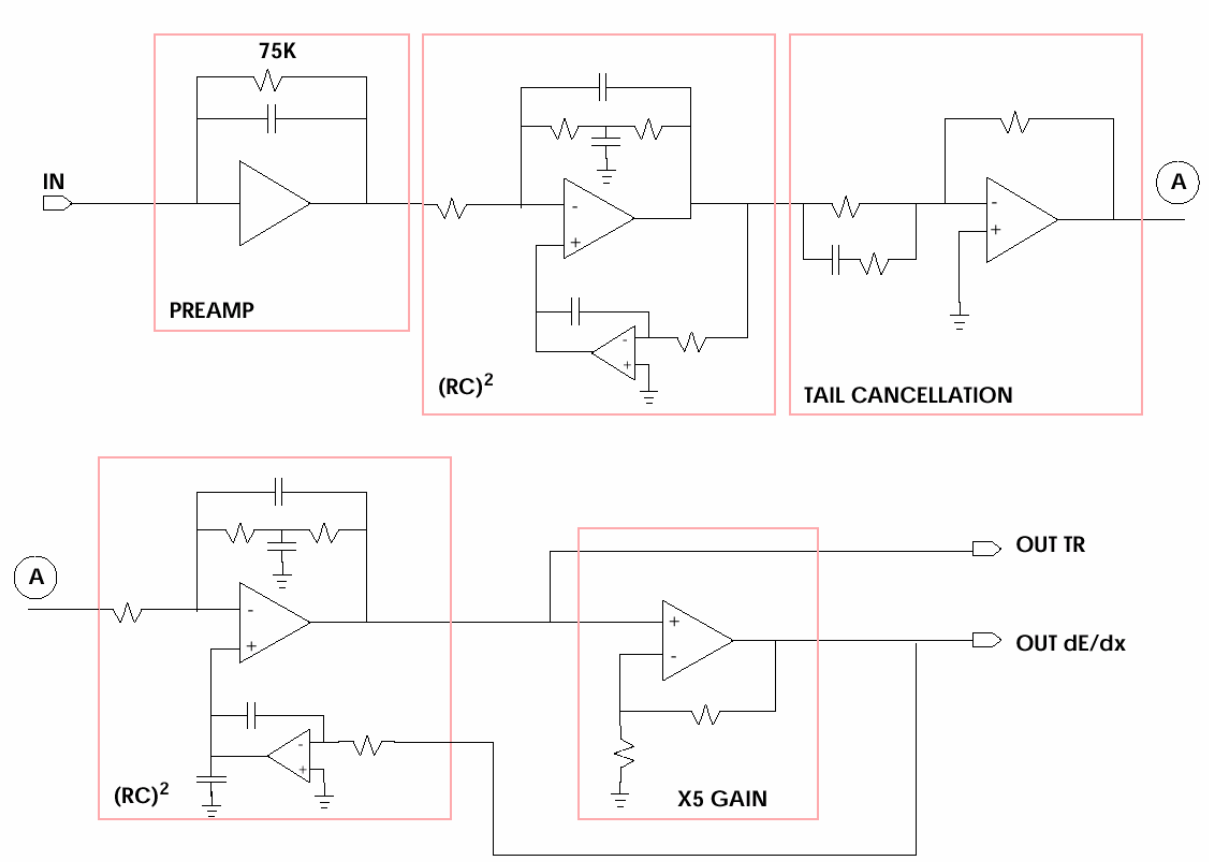
Simulated: ω

Measured: o





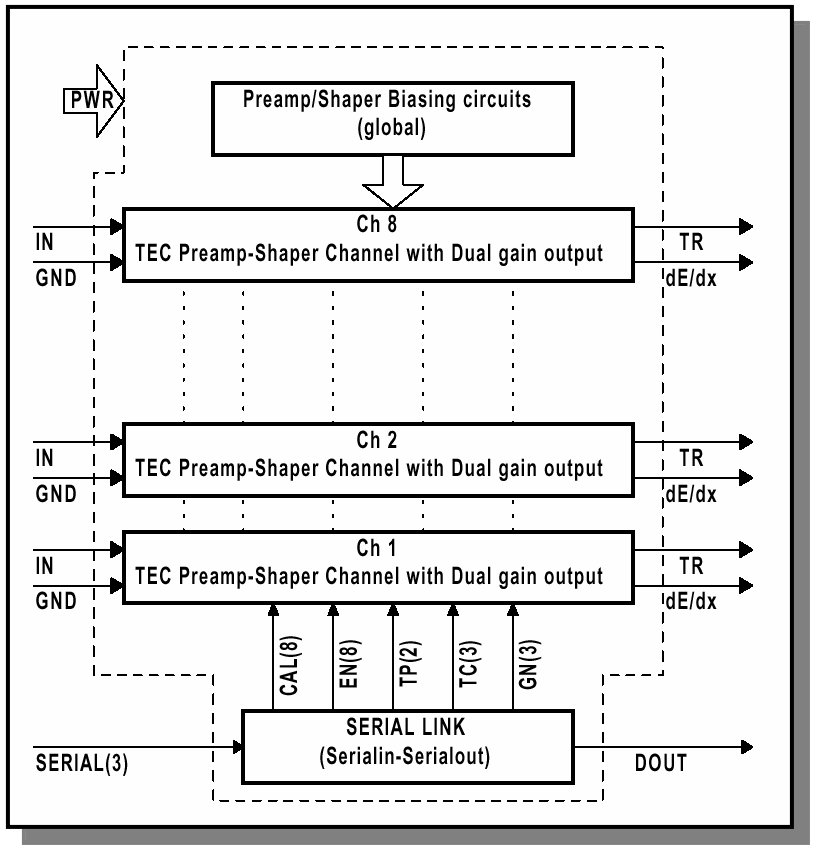
Time Expansion Chamber & Transition Radiation Detector Preamp/Shaper



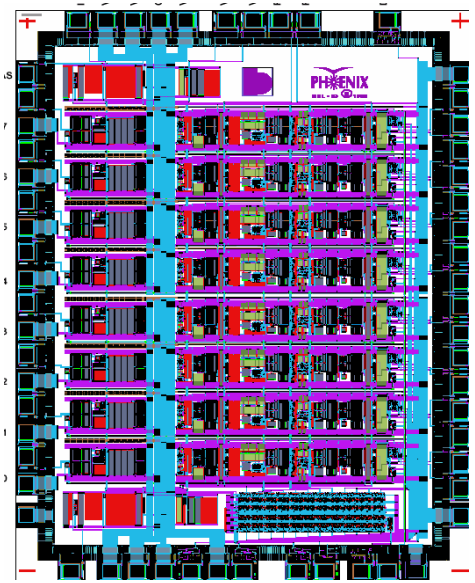
- 1m MWPC with 20 pF C_{DET}
- Fast (70 ns) shaping for charged particle tracking
- Dual gain outputs for measurement of dE/dx and Transition Radiation

TEC-TRD Preamp/Shaper

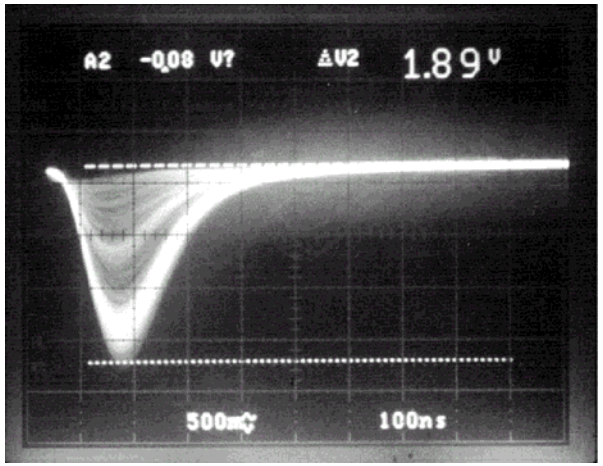
Block Diagram



Die Layout



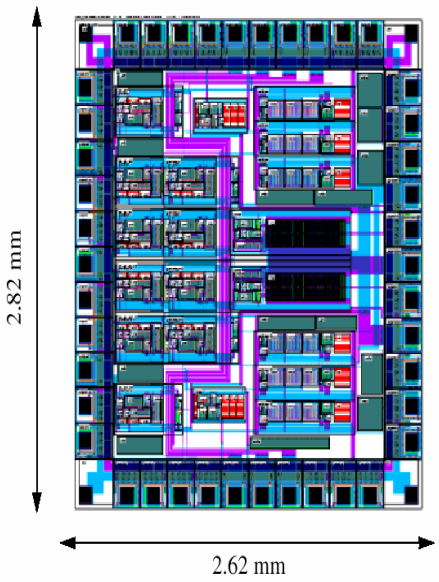
X-ray Response



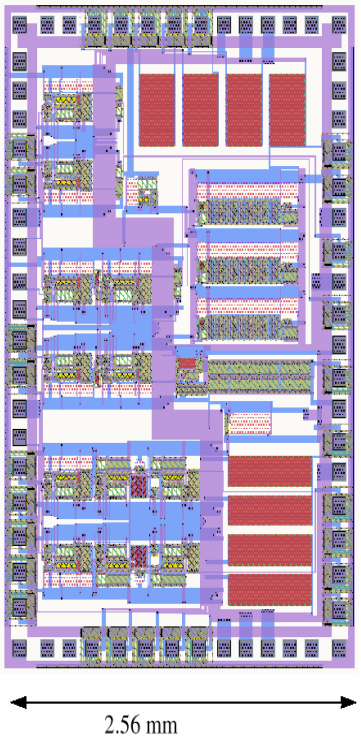
A. Kandasamy, E. O'Brien, P. O'Connor, W. VonAchen, "A monolithic preamplifier-shaper for measurement of energy loss and transition radiation" IEEE Trans. Nucl. Sci. 46(3), June 1999, 150-155

Drift Detector Preamplifier

HP 1.2um version



AMS 1.2um version

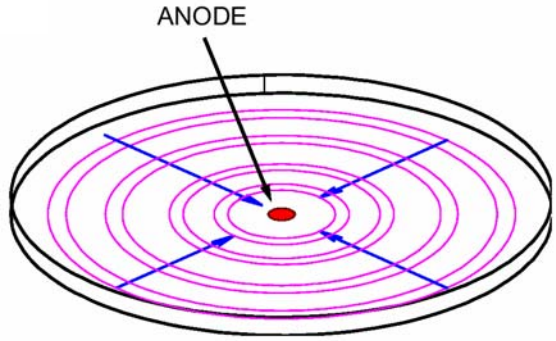


Requirements for 100 eV resolution with a 0.2 pF detector at 1 - 5 μs shaping time:

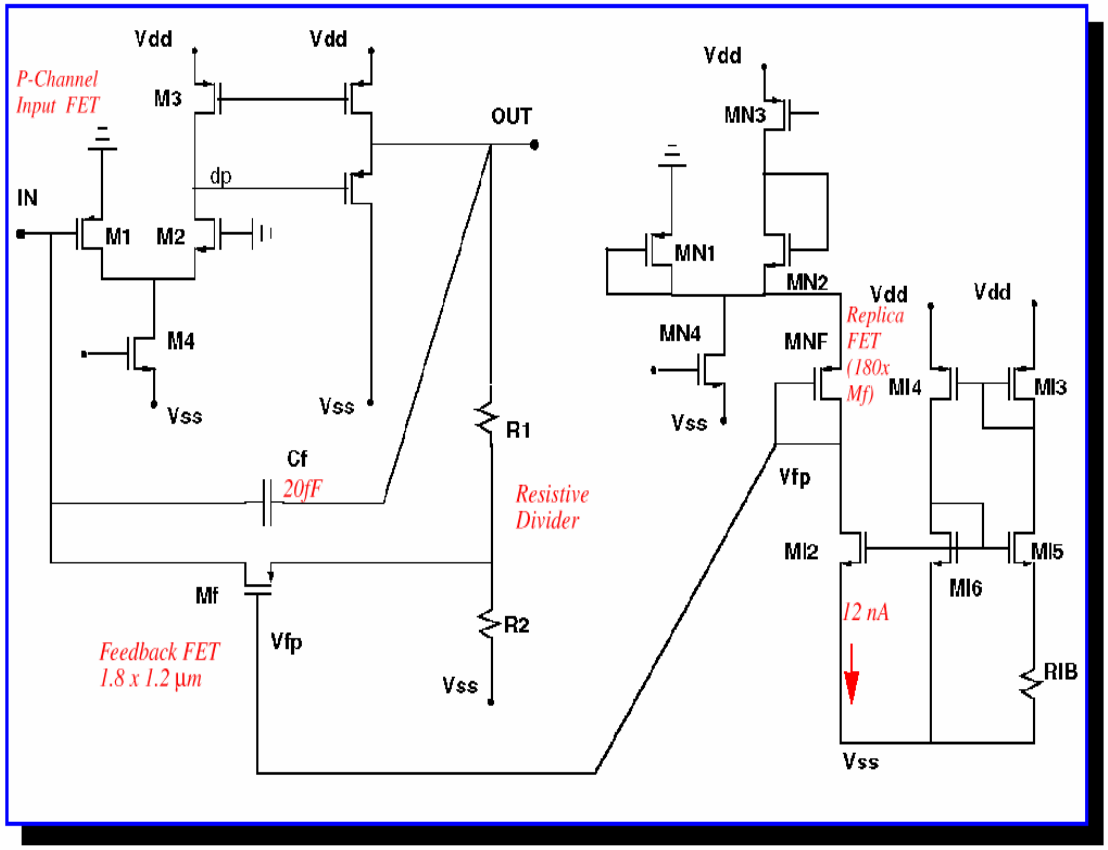
- $I_{leak} < 10$ pA
- $R_F > 3$ GΩ
- $g_m > 0.4$ mS
- $K_F < 1.8 \times 10^{-25}$ J

- Used with ultra-low capacitance silicon drift detector, $C_{det} < 0.3$ pF
- Preamp only, used with external shaper
- Purpose: explore lowest noise possible with CMOS
- Reset system: MOS transistor with special bias circuit to achieve stable, > 100 GΩ equivalent resistance

Detector



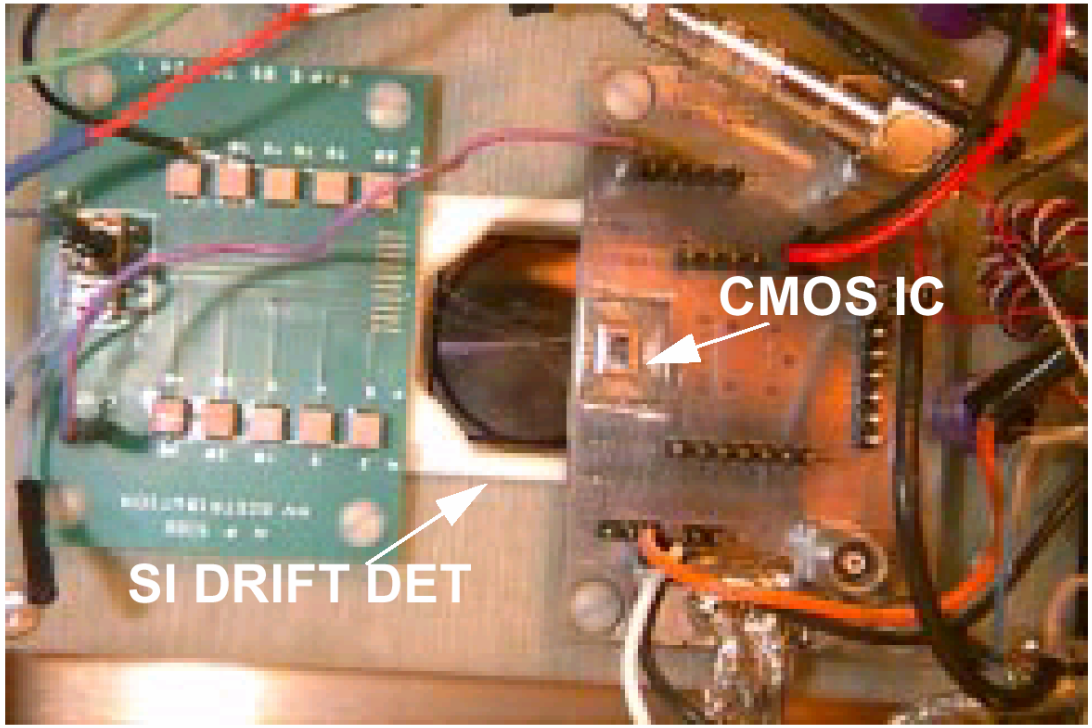
Drift detector preamplifier – simplified schematic



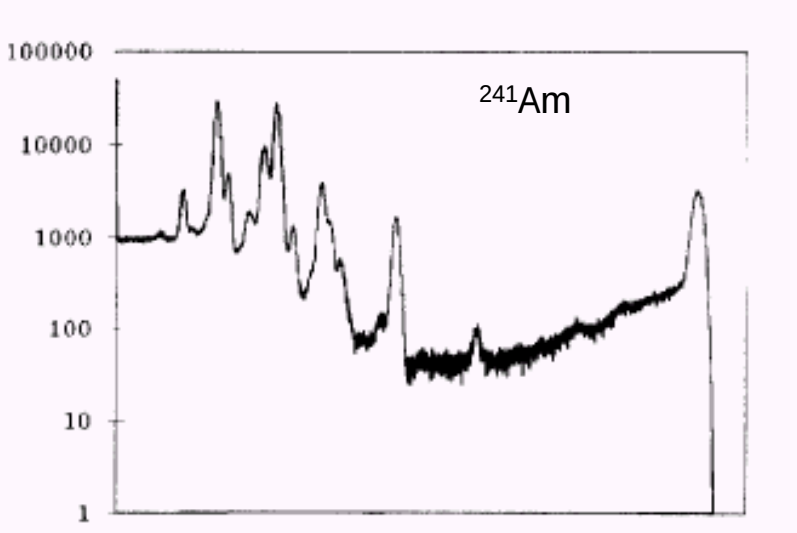
Preamplifier

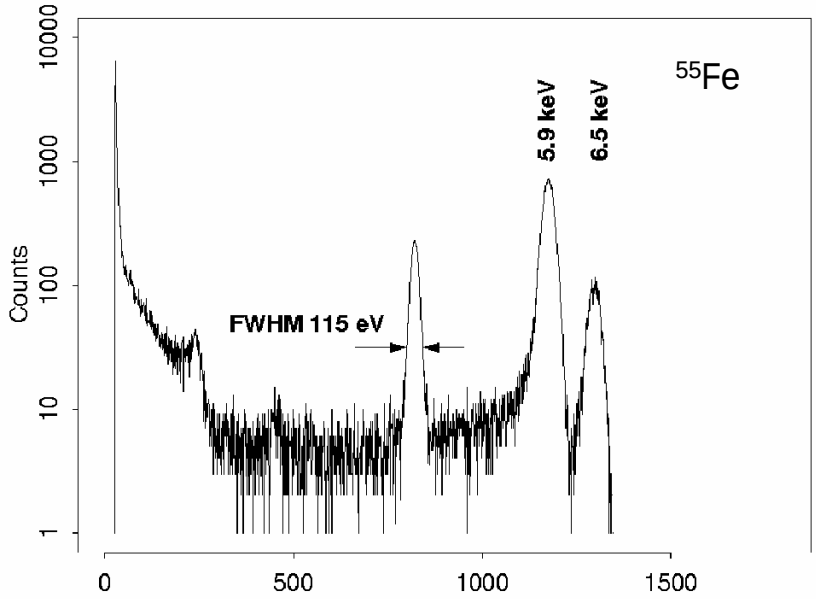
Bias Circuit

Drift Detector & CMOS Preamplifier



Drift detector preamplifier – results

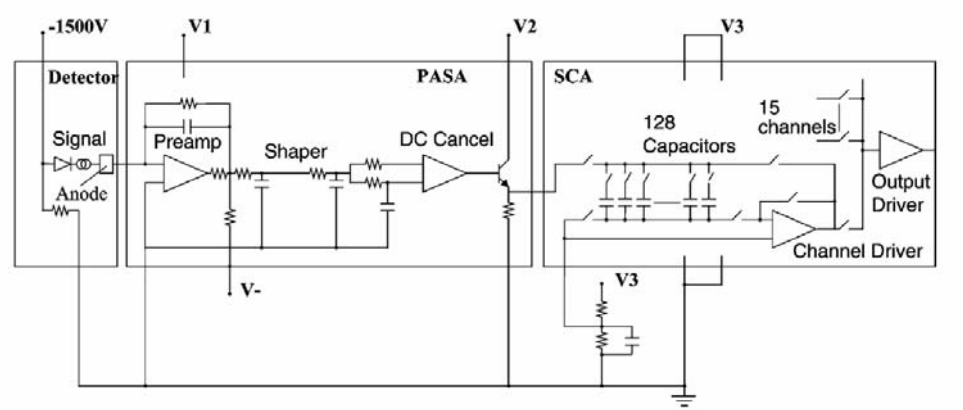


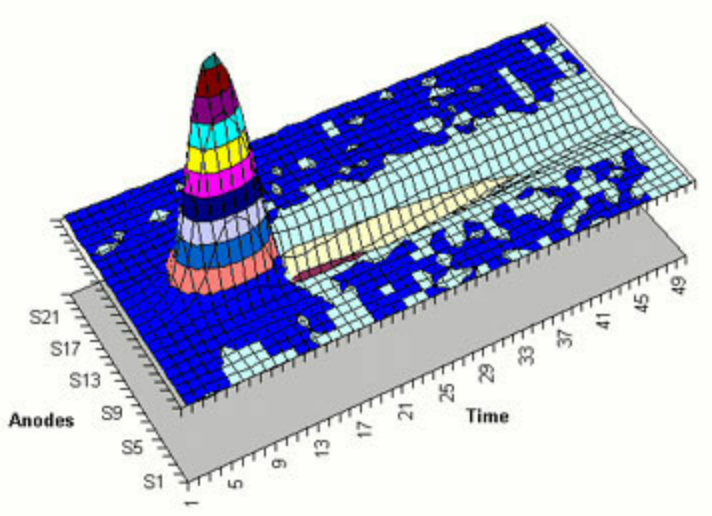


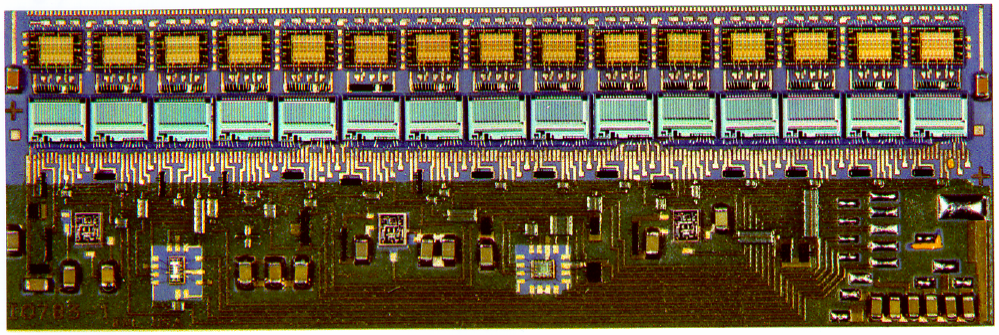
- Spectra of ^{241}Am and ^{55}Fe taken with 5mm Φ Si drift detector and CMOS X-ray preamplifier. Detector and circuit cooled to -75 C.
- External 2.4 μs shaping.
- ENC = 13 e^- rms.
- Noise without detector: 9 e^-

P. O'Connor et.al., "Ultra Low Noise CMOS Preamplifier-shaper for X-ray Spectroscopy", NIM A409 (1998), 315-321

SVT 240-channel Multi-Chip Module







D. Lynn et al., "A 240 channel thick film multi-chip module for readout of silicon drift detectors", NIM A439 (2000), 418 - 426

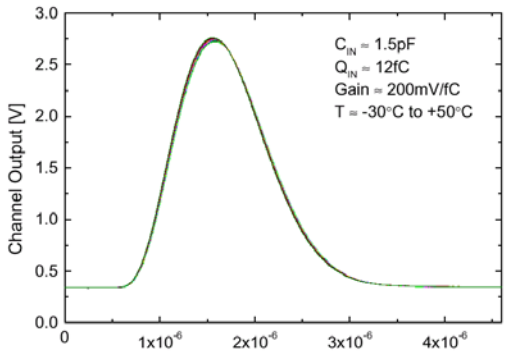
BNL Preamp/Shaper ICs, 1995 - 2001

PROJECT	Hi-res. Spectroscopy	RHIC – PHENIX	RHIC – STAR	LHC – ATLAS	Industry Partnership	NSLS – HIRAX	Units
DETECTOR	Si drift	Time Expansion Chamber	Silicon Vertex Tracker	Cathode Strip Chamber	CdZnTe gamma ray detector	Si Pixel	
Function	Preamp	Preamp/Shaper	Preamp/Shaper	Preamp/Shaper	Preamp/Shaper	Preamp/Shaper/ Counter	
C_{DET}	0.3	30	3	50	3	1.5	pF
Peaking Time	2400	70	50	70	600:1200:2000:4000	500:1000:2000:4000	ns
Gain	10	2.4:12 – 10/25	40:70:90	4	30:50:100:200	750:1500	mV/fC
Power	10	30	3.8	33	18	7	mW/channel
ENC	10	1250	400	2000	100	24	rms electrons
Dynamic Range	1250	4600	700	1900	5600		
Technology	CMOS 1.2 um	CMOS 1.2 um	Bipolar 4 GHz	CMOS 0.5 um	CMOS 0.5 um	CMOS 0.35 um	
Input Transistor	PMOS 150/1.2 um	NMOS 4200/1.2 um	NPN 10 uA	NMOS 5000/0.6 um	NMOS 200/0.6 um	PMOS 400/0.4 um	
Reset Scheme	Compensated PMOS, > 1GΩ	Polysilicon, 75 kΩ	Nwell, 250 kΩ	Compensated NMOS, 30 MΩ	Compensated PMOS	Compensated NMOS	
No. Channels	6	8	16	24	16	32	
Die Size	7.3	15	8	20	19	16	mm^2

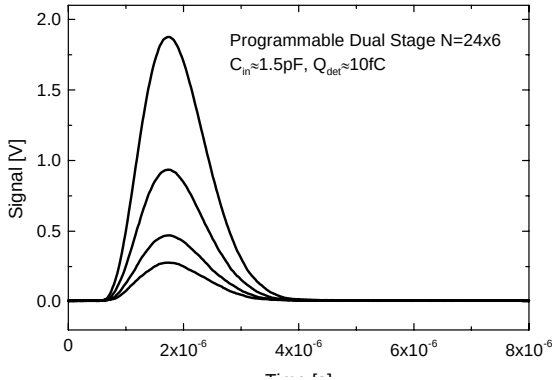
Practical amplifier considerations

- Preamplifier reset
- High order filters
- Programmable pulse parameters
- Circuit robustness:
  - Self-biasing
  - Low-swing,differential I/O
  - Circuits tolerant to variations in
    - Temperature
    - Process
    - Power supply
    - DC leakage current
    - Loading

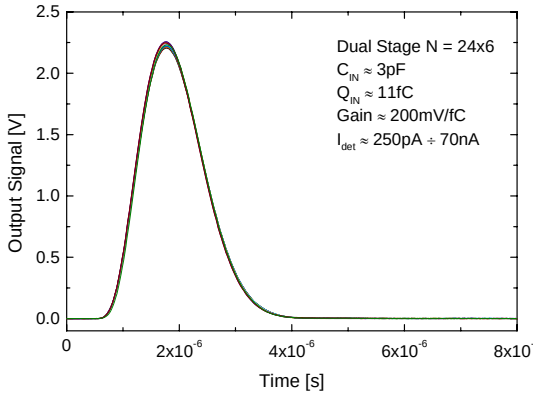
Pulse vs. Temperature



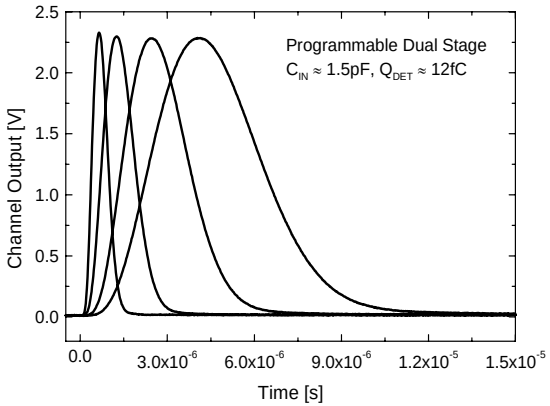
Gain variation



Pulse vs. I_{leak}



Peaking time variation



	I_{leak}	Supply	Temperature	Rate (to GHz)	CIn	Load
Gain	< 0.1%/nA	<0.001%/V	-0.04%/°C	< 0.1%	<0.1%/pF	No slew-rate limit
Baseline	< 0.3mV/nA	<30 µV/V	12 µV/°C	< 8 mV	-	20Ω - 1uF

G. De Geronimo et al., “A generation of CMOS readout ASICs for CZT detectors", IEEE Trans. Nucl. Sci. 47, Dec. 2000, 1857 - 1867

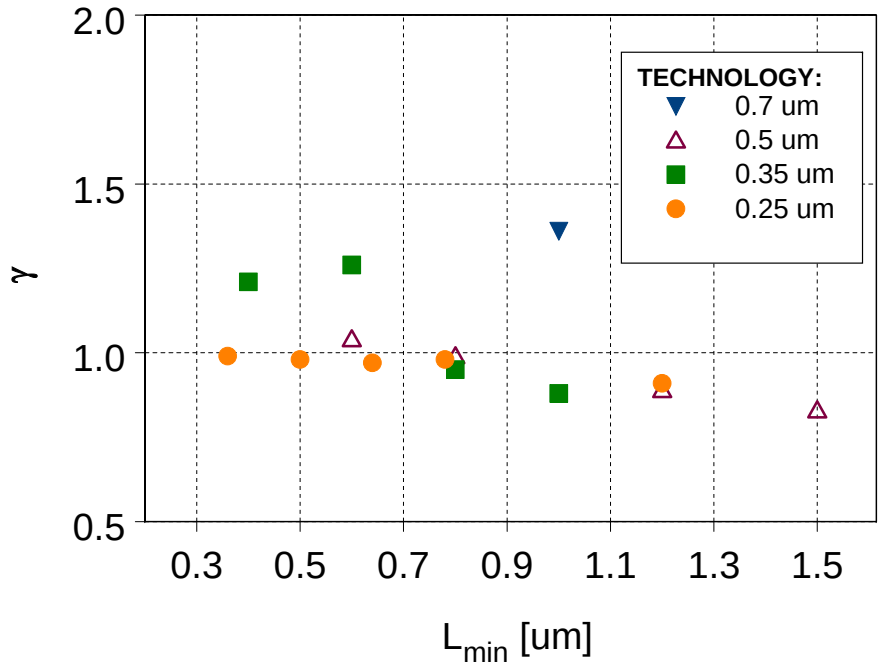
MOS Scaling and Charge Amplifier Design

Scaling issues

- Fundamental device noise mechanisms
  - *Hot electron effects*
  - *New process steps effect on 1/f noise*
  - *Gate tunnelling current*
- Change of the current-voltage characteristics
  - *Increase of weak inversion current*
  - *Mobility decrease*
  - *Velocity saturation*
  - *Drain conductance (device intrinsic DC gain)*
- Power supply scaling

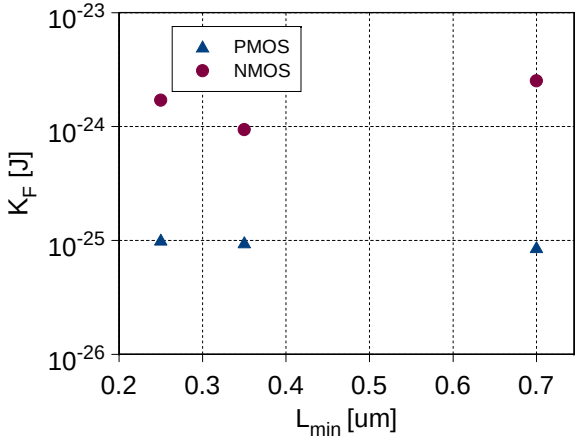
Series white noise

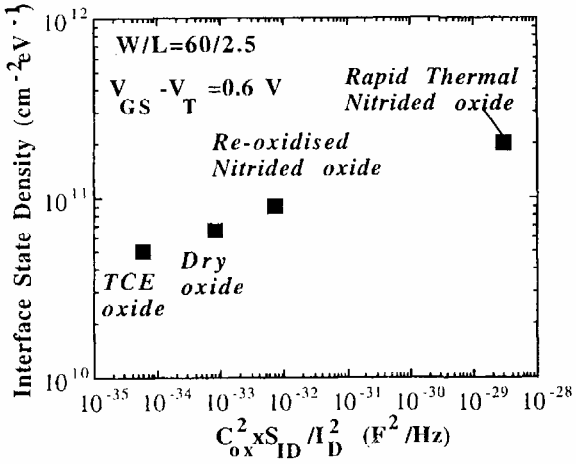
- Parameter γ = gm * Rn
- Some models predict $\gamma >> 1$ for short channel devices
- At moderate inversion and low VDS, γ remains in the range $0.8 < \gamma < 1.4$
- Shallow junctions increase S/D series resistance => noise



1/f noise in submicron CMOS

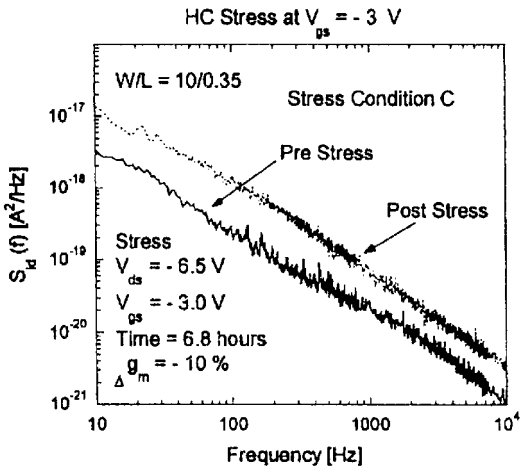
- Processes with n+/p+ poly gates and retrograde wells create surface-channel PMOS – PMOS 1/f noise to become more like NMOS?
- Shallow junctions required for scaled processes limit the thermal budget – hence gate process will have reduced post-oxidation anneal and higher trap density, higher 1/f
- For ultrathin gates new dielectrics with higher trap densities will be used (nitrided, halogenated, H2 annealed)

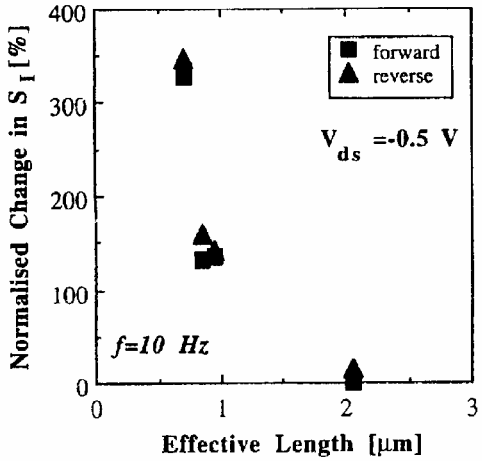




1/f noise and hot carrier stress

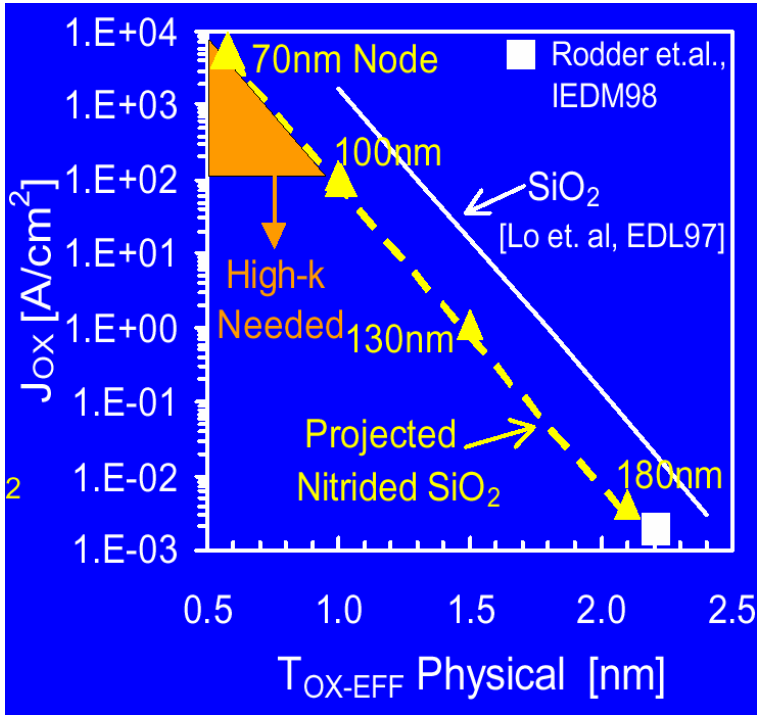
- Hot carrier stress generates new oxide/interface traps.
- 1/f noise more sensitive than change in static parameters:
  - Δg_m *-10%*
  - $\Delta(1/f)$ *+400%*
- Worse for shorter channel lengths
- A device engineered for "acceptable" degradation of V_{th} and g_m may show unacceptable increase in 1/f noise over the same period.
- The operating point of the device will determine the stability of the long-term 1/f noise





Gate tunneling current

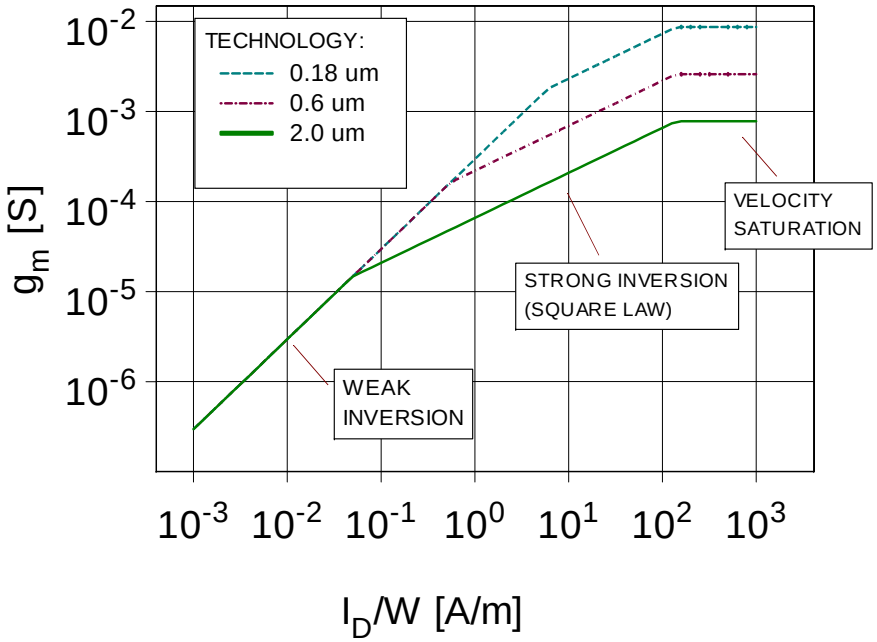
- Gate current expected to increase 100 – 200 x per generation below 0.18 μm
- J_{ox} ~ 100 A/cm^2 projected for L_{min} = 0.1 μm generation with nitrided SiO_2
- Considered tolerable for digital circuits (total gate area per chip ~ 0.1 cm^2)
- Typical CSA input FET would have I_G ~ 1 - 10 μA; ENCp ~ 2000 - 7000 rms e- at 1 μsec



SiO_2 gate leakage current (Lo et al., Electron Dev. Letters 1997)

Departure from square-law characteristics

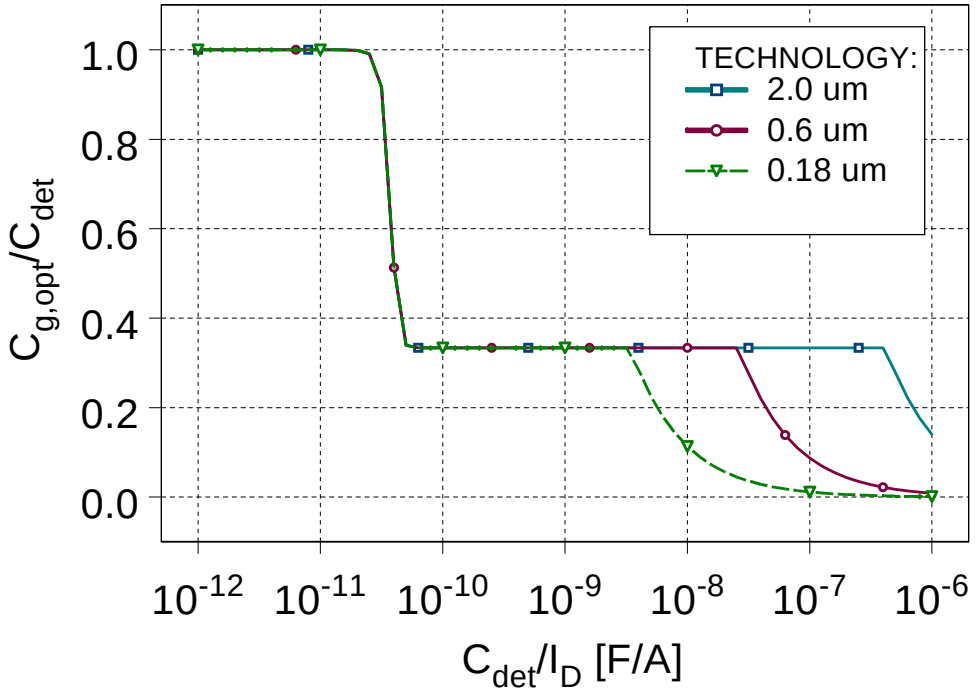
- Submicron devices are less often operated in strong inversion, square-law region.
- Influences behavior of series white thermal noise
- Square-law devices have minimum series noise when $C_{gs} = C_{det}/3$
- For other regions of operation, minimum noise can be for larger or smaller values of C_{gs}



Generalized capacitive matching condition

– Drain current = constant

– Ratio of C_{gs} to C_{det} determined by C_{det}/I_d:

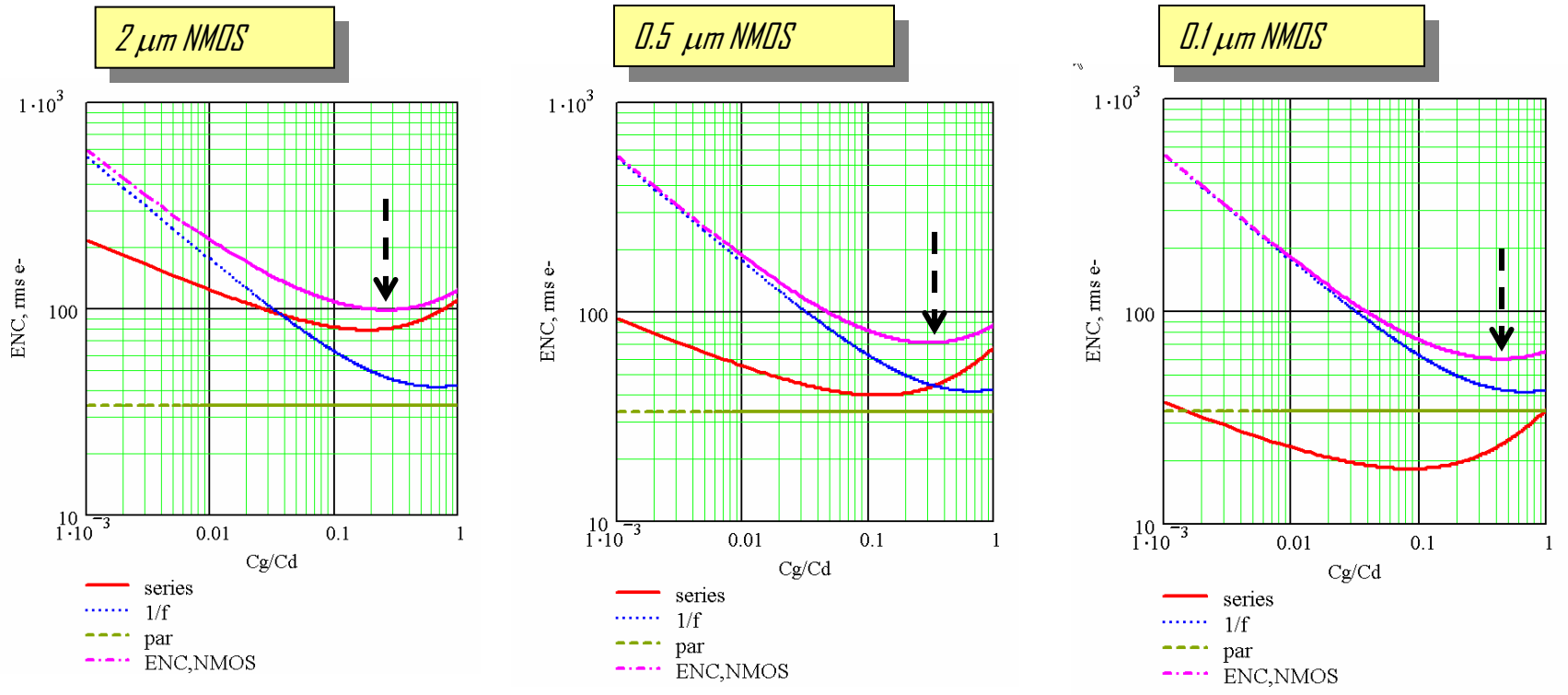


C_{det} / I_D Ratio	Region of operation	Optimum capacitive match
$\frac{C_{det}}{I_D} < \frac{6\mu}{v_{sat}^2}$	Velocity saturated	$C_{gs} = C_{det}$
$\frac{6L^2}{\mu(nkT/q)^2} < \frac{C_{det}}{I_D} < \frac{6\mu}{v_{sat}^2}$	Strong-inversion square-law	$C_{gs} = C_{det} / 3$
$\frac{C_{det}}{I_D} > \frac{6L^2}{\mu(nkT/q)^2}$	Weak inversion boundary	$C_{gs} = \frac{2L^2 I_D}{C_{det}(nkT/q)^2}$

P. O'Connor, G. De Geronimo, "Prospects for Charge Sensitive Amplifiers in Scaled CMOS", NIM-A accepted for publication

Capacitive match vs. scaling – mixed white, 1/f and parallel noise

- C_{det} = 3 pF, t_m = 1 μs, P_{diss} = 1 mW, I_{leak} = 100 pA

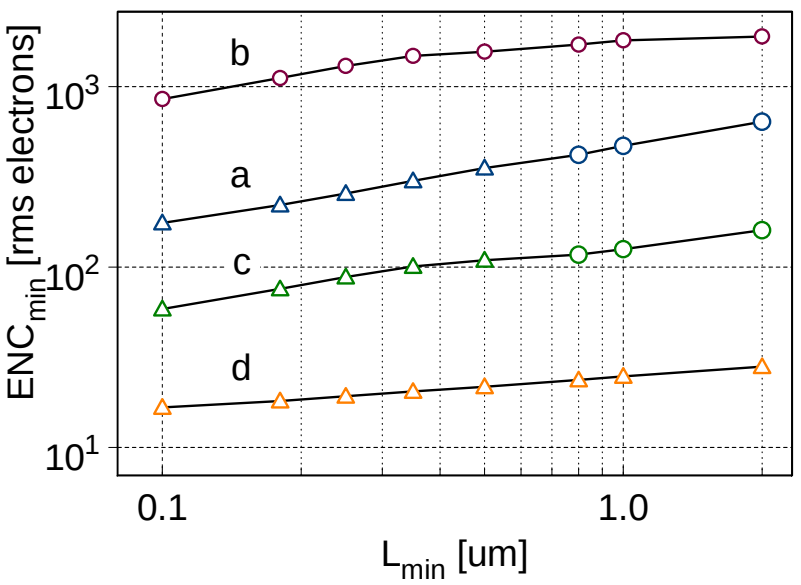


Noise vs. scaling for mixed white, 1/f, and parallel noise

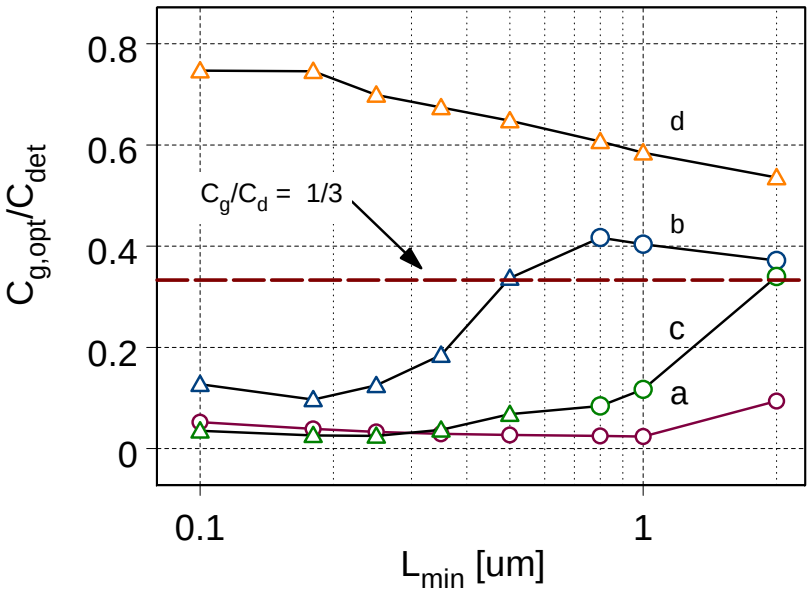
4 detector scenarios for scaling study

System	C_{det}	t_s	P	I_{leak}	Detector	Typical Application
a	30	75	10	.001	Wire Chamber	Tracking, Imaging
b	15	25	0.2	10	Si Strip	Tracking
c	0.3	25	0.02	1	Si Pixel	Tracking
d	3	2500 – 500*	10	0.01	Semiconductor	Spectroscopy
UNITS	pF	ns	mW	nA	-	-

Noise vs. scaling



Optimum gate width vs. scaling



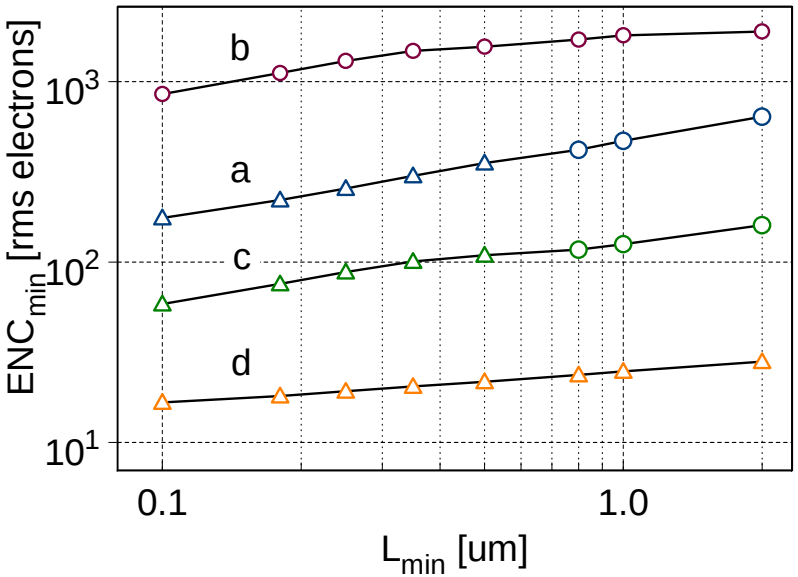
Noise and Power vs. Scaling

4 detector scenarios for scaling study

System	C_{det}	t_s	P	I_{leak}	Detector	Typical Application
a	30	75	10	.001	Wire Chamber	Tracking, Imaging
b	15	25	0.2	10	Si Strip	Tracking
c	0.3	25	0.02	1	Si Pixel	Tracking
d	3	2500 – 500*	10	0.01	Semiconductor	Spectroscopy
UNITS	pF	ns	mW	nA	-	-

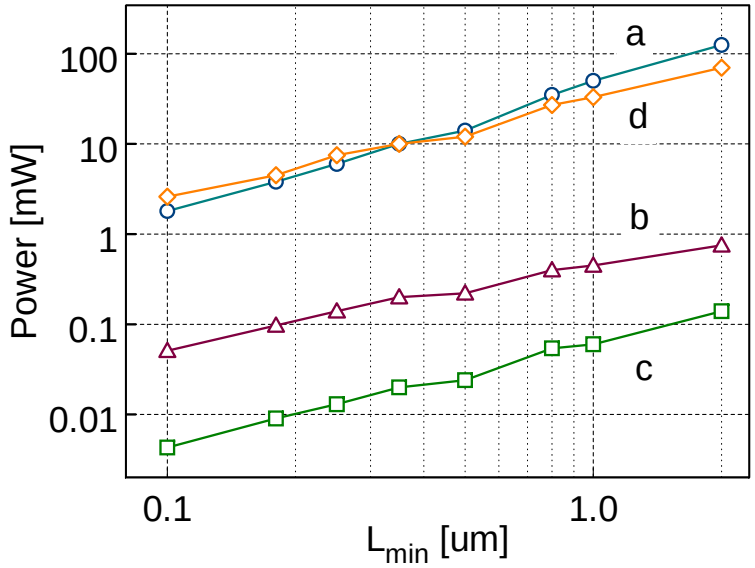
Noise vs. scaling

(power held constant)

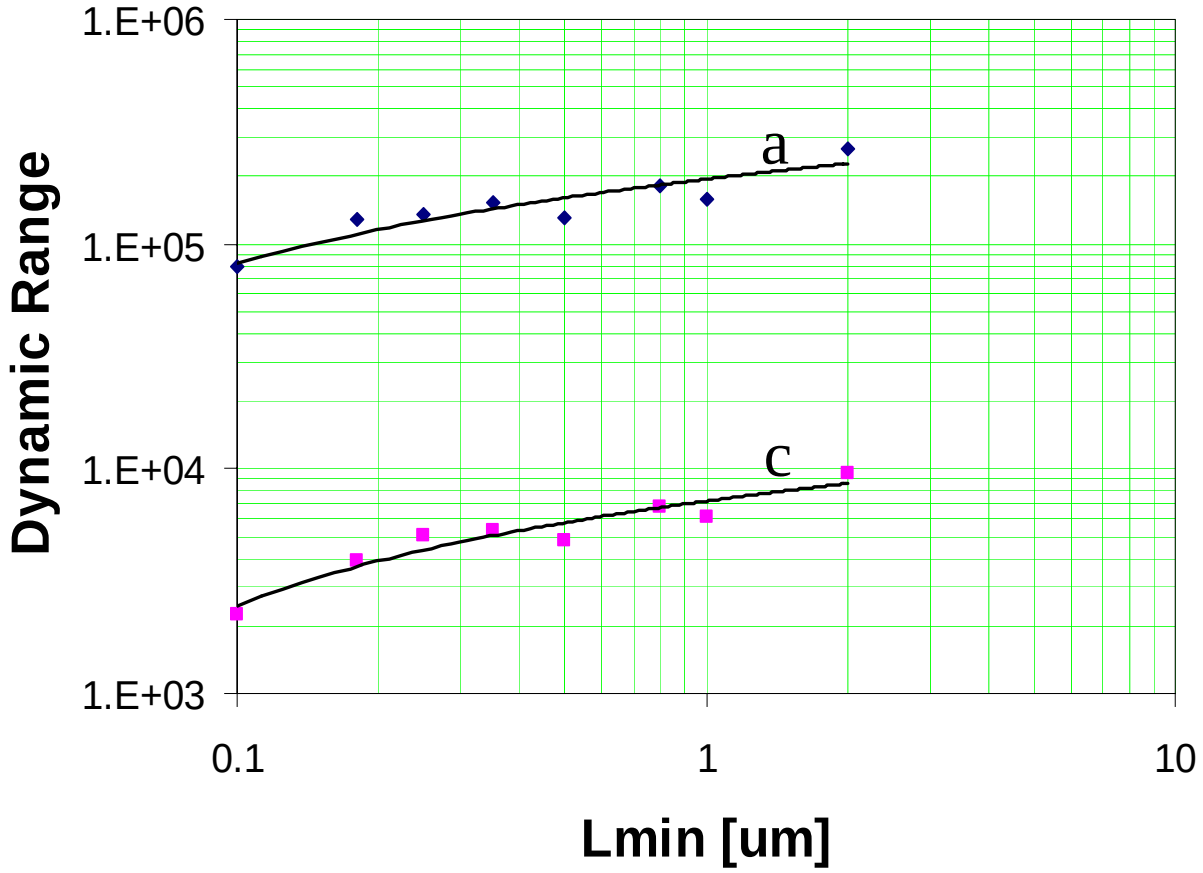


Power vs. scaling

(noise held constant)

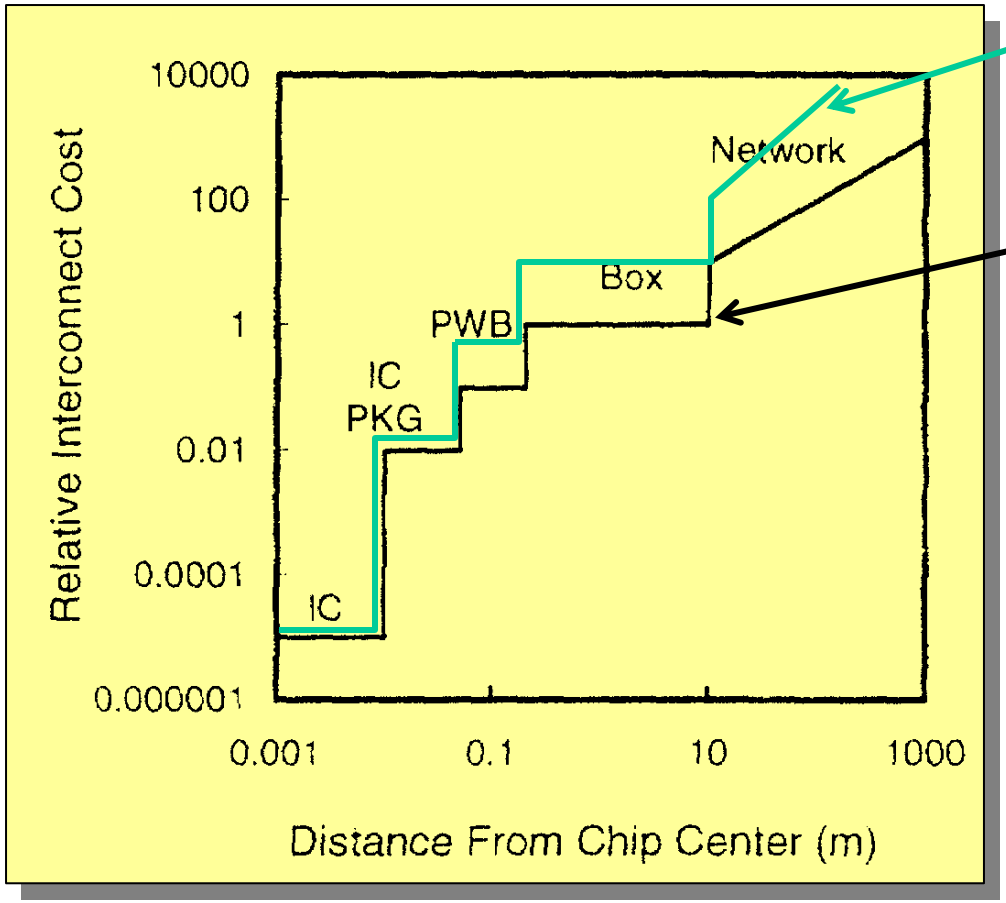


Dynamic Range vs. scaling



Interconnect

Cost of Interconnect



analog

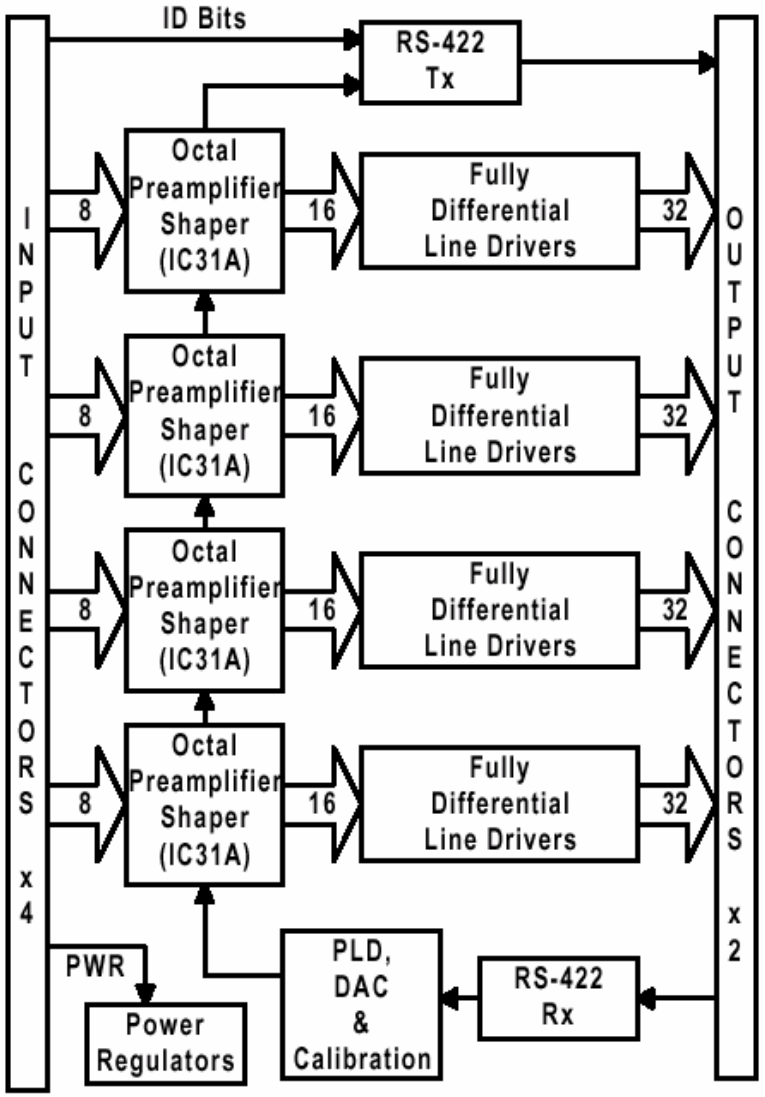
digital

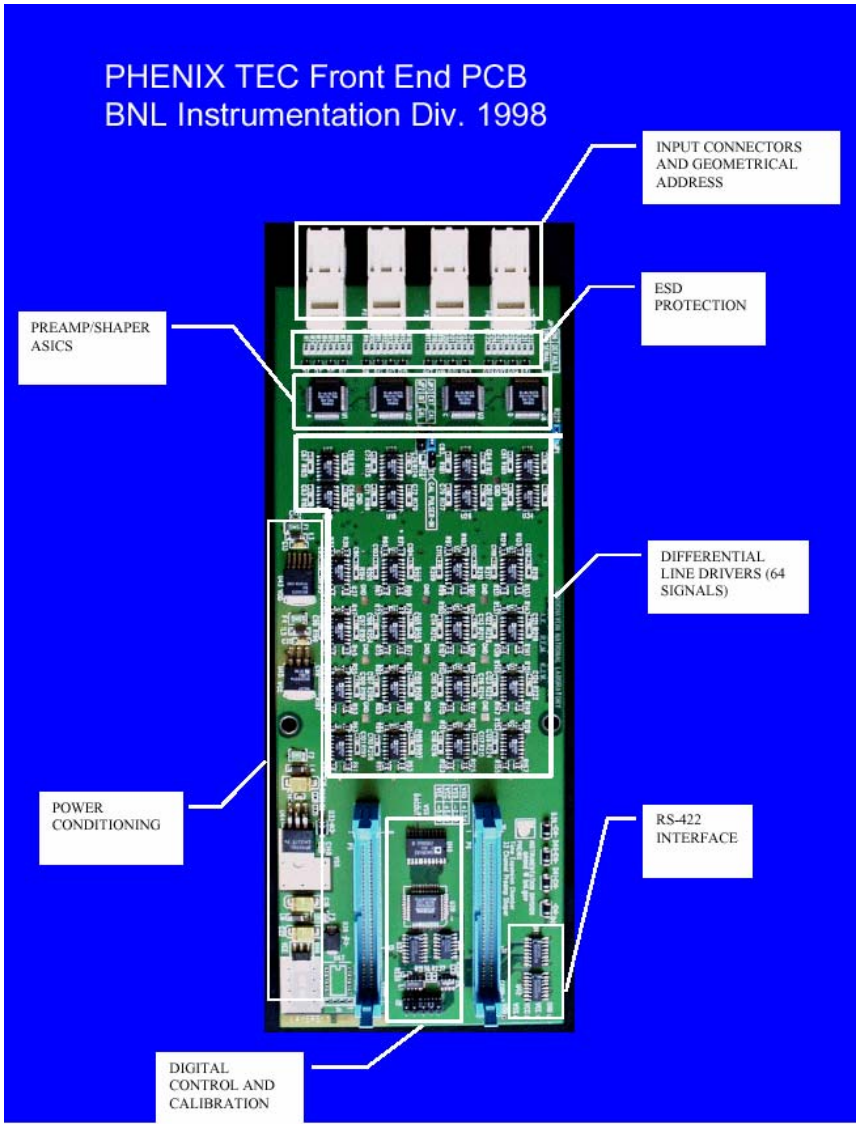
Interconnect issues in monolithic front ends

- Detector – preamplifier
  - *Lowest possible capacitance*
  - *Maintain small form factor*
  - *Ease of assembly*

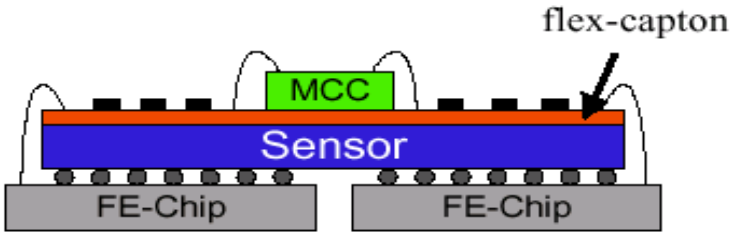
- Front end – ADC
  - *Efficient use of expensive "analog" interconnect*

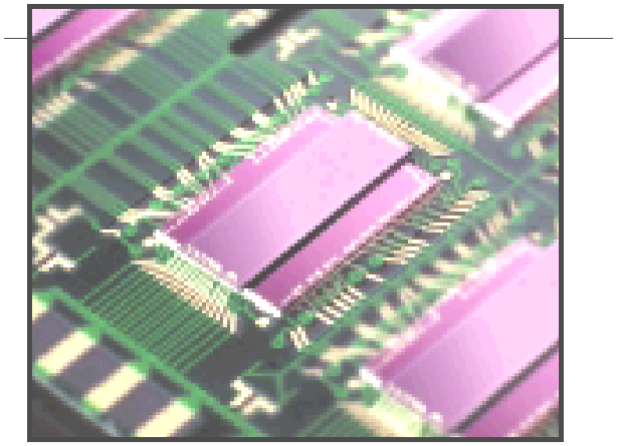
TEC Front-End Card

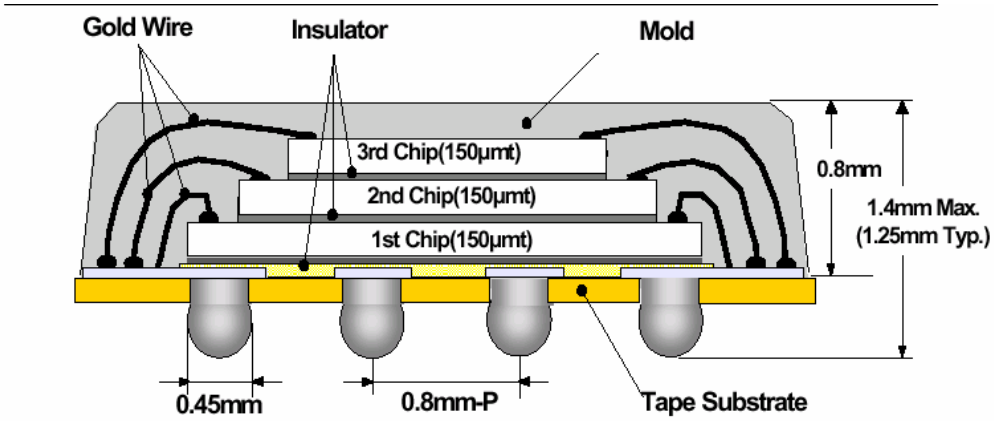




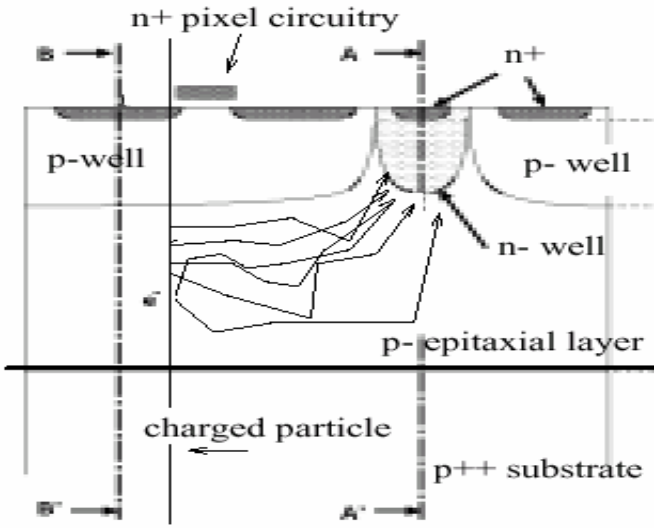
Make the chip a part of the detector

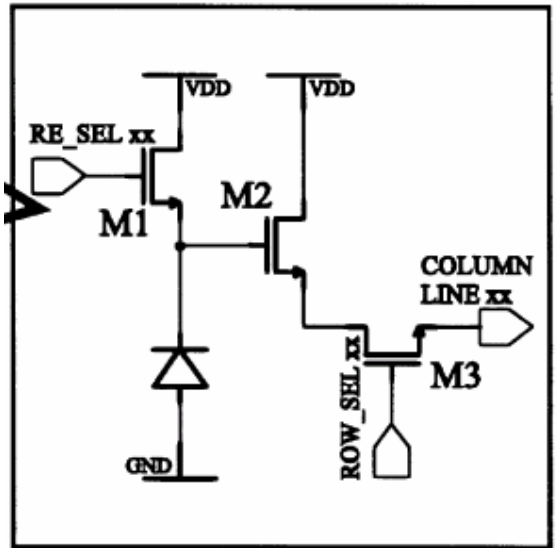


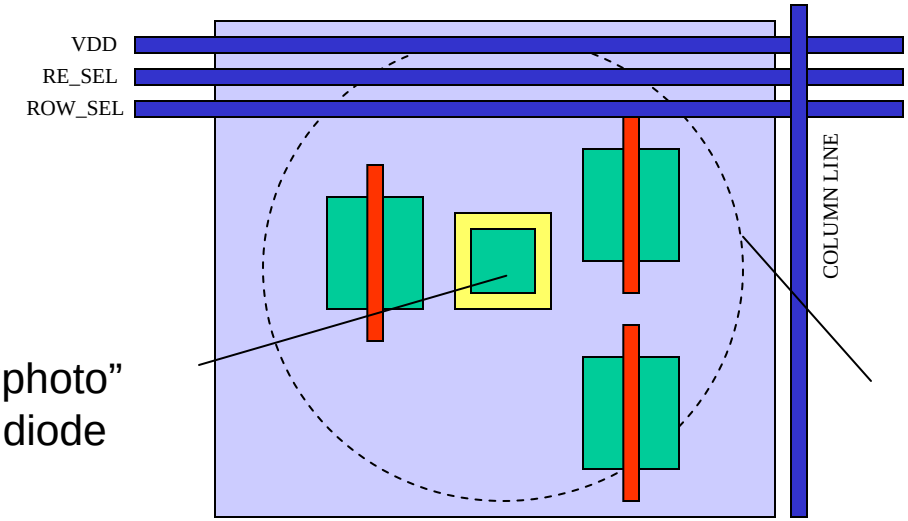




Make the detector part of the chip

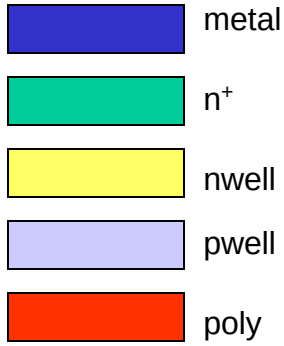






"photo" diode

diffusion isochron

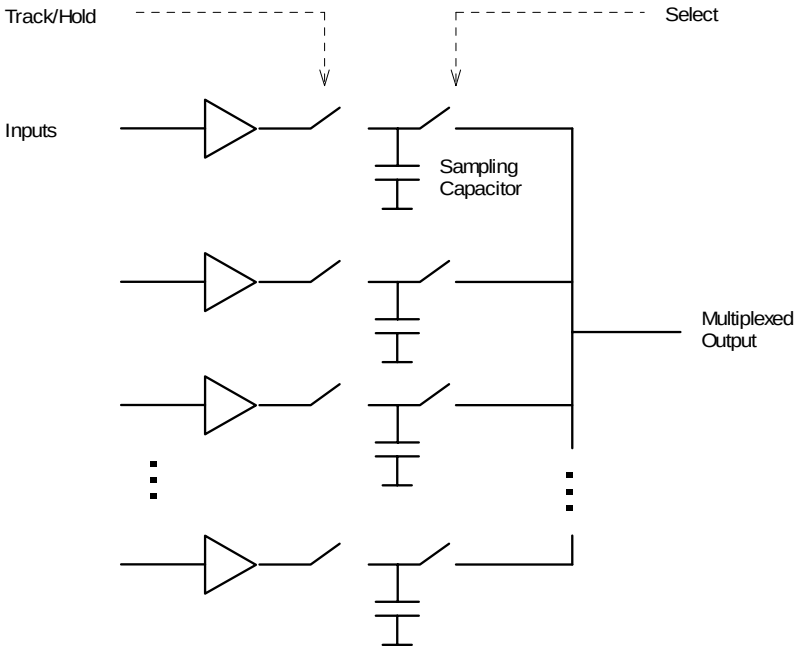


What goes between the preamp/shaper and the ADC?

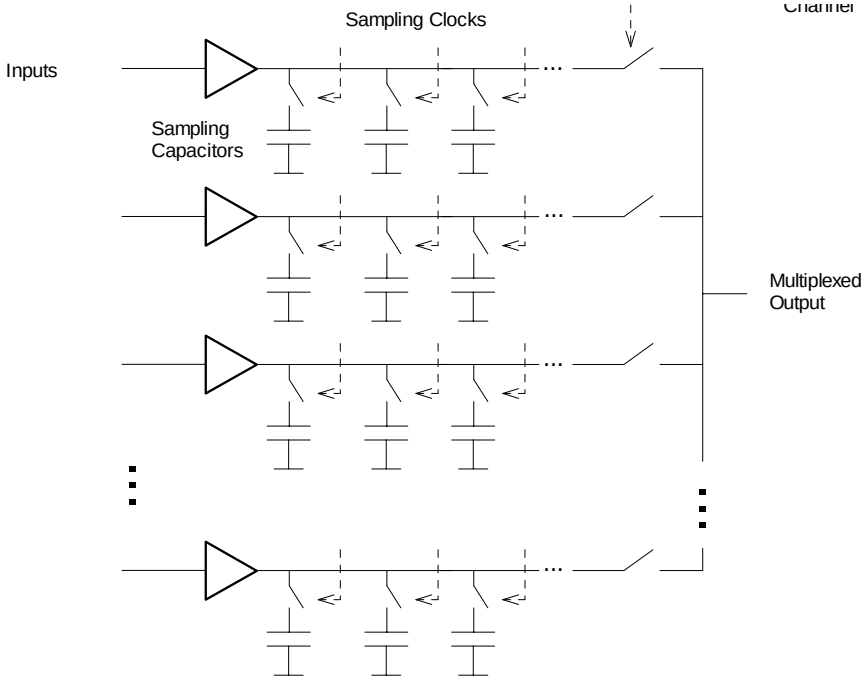
- Experimental needs differ
  - *number of channels*
  - *occupancy*
  - *rate*
  - *trigger*
- Usually, its too expensive to put an ADC per channel
- Anyway the ADC would usually not be doing anything useful
  - *Occupancy < 100%, so no events most of the time in most channels*
- What is the most efficient way to use the ADC(s)?

Analog Sampling and Multiplexing

Track-and-hold
(triggered systems)

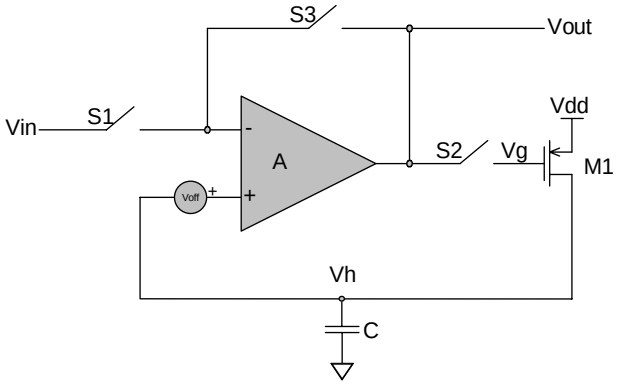


Analog memory
(non-triggered)

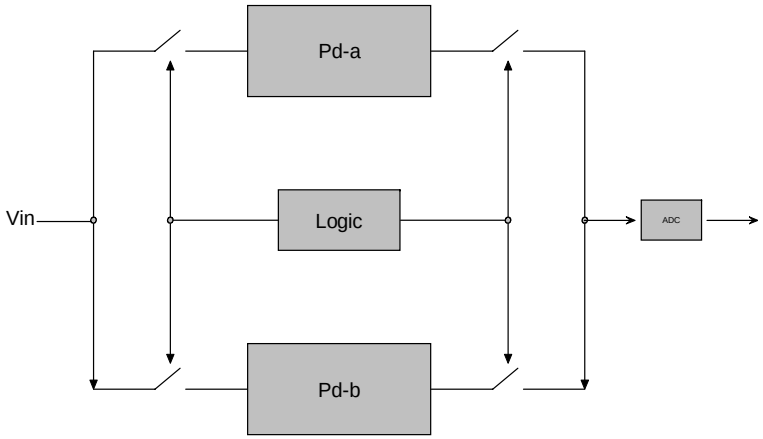


New Peak Detector and Derandomizer

- Self-triggered
- Self-sparsifying
- New 2-phase configuration allows rail-to-rail operation, eliminates offsets
  - *absolute accuracy ~ 0.2%*
  - *to within 300 mV of rails*

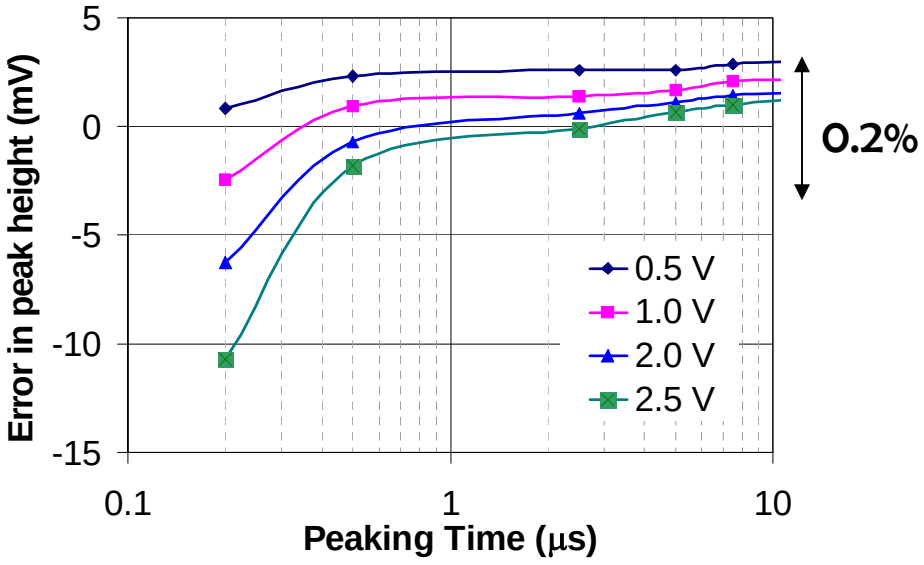


- Two or more peak detectors in parallel can be used to derandomize events
  - *If a second pulse arrives before the readout of the first pulse in Pd-a, it is detected and stored on Pd-b.*

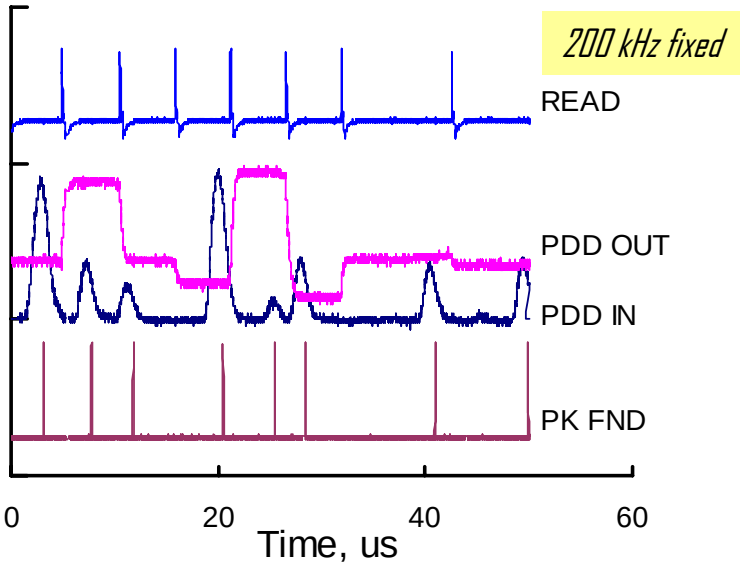


First experimental results

Accuracy of single PD



PD/D response to random pulse train (^{241}Am on CZT)



G. DeGeronimo, P. O'Connor, A. Kandasamy, "Analog Peak Detect and Hold Circuits Part 2: The Two-Phase Offset-Free and Derandomizing Configurations", NIM-A submitted for publication

Conclusions

- Today's CMOS technology can be used to make low noise front ends whose performance is nearly as good as the best discrete units
- In the future, increasing device cutoff frequency and gate oxide quality will help improve noise BUT
  - *Potentially serious increases in 1/f noise and gate current may accompany new process sequences*
  - *Low supply voltage will hamper high dynamic range*
- Increasing attention will have to be paid to interconnect at the technology, circuit, and architecture levels