Capacitive matching for MOSFET Charge-Sensitive Preamplifiers with Constant Current

$$ENC^2 = \frac{1}{2}\, e_n^2\; C_{in}^2\, \Im_1 \tag{1}$$

where

$$\begin{aligned}
C_{in} &= C_{det} + C_{ox}WL \quad \text{is the total input capacitance;} \\
e_n^2 &= \frac{4kTa_n}{g_m} \quad \text{is the input voltage spectral noise density with } a_n \approx 2/3 \text{ for FET;} \\
g_m &= \sqrt{2\mu C_{ox}(W/L)I_d} \quad \text{MOSFET in strong inversion;} \\
&= qI_d/nkT \quad \text{weak inversion;} \\
\Im_1 &= \int_{-\infty}^{+\infty} [h'(t)]^2 dt \text{ is the series noise integral; } h(t) \text{ is the impulse response.}
\end{aligned}$$

with the current I_d, length L, and impulse response $h(t)$ held constant, the optimum size for a device in strong inversion is found from:

$$\begin{aligned}
\frac{d}{dW}(ENC^2) &= \frac{2kTa_n\Im_1}{\sqrt{2\mu C_{ox}I_d/L}}\left\{-\frac{1}{2}\frac{(C_{det}+C_{ox}WL)^2}{W^{3/2}} + \frac{2(C_{det}+C_{ox}WL)C_{ox}L}{W^{1/2}}\right\} \\
&= 0
\end{aligned} \tag{2}$$

$$C_{det} + C_{ox}WL = 4C_{ox}WL$$

We find

$$\boxed{C_{ox}WL = \frac{1}{3}C_{det}} \tag{3}$$

or

$$W_{opt} = \frac{C_{det}}{3C_{ox}L}$$

Large W/I_d ratio eventually leads to weak inversion operation. Then g_m is independent of W so any increase of W degrades the ENC. Taking this into account:

$$W_{opt} = min\left(\frac{C_{det}}{3C_{ox}L}, W_{wi}\right) \text{ where}$$

$$W_{wi} = \frac{2LI_d}{(3kT/q)^2\mu C_{ox}} \text{ defines the boundary of weak inversio}$$

MOS I-V Characteristics

Linear region $V_{DS} < V_{GS} - V_T$:

$$I_D = \mu C_{ox}\frac{W}{L}\left\{(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right\} \qquad (1)$$

Saturation region $V_{DS} > V_{GS} - V_T$:

1. Strong inversion $V_{GS} - V_T > \dfrac{3kT}{q}$:

$$\boxed{\begin{aligned} I_D &= \frac{\mu C_{ox}(W/L)}{2n}(V_{GS} - V_T)^2 \\ \frac{g_m}{I_D} &= \sqrt{\frac{\mu C_{ox}(W/L)}{2nI_D}} \end{aligned}} \qquad (2)$$

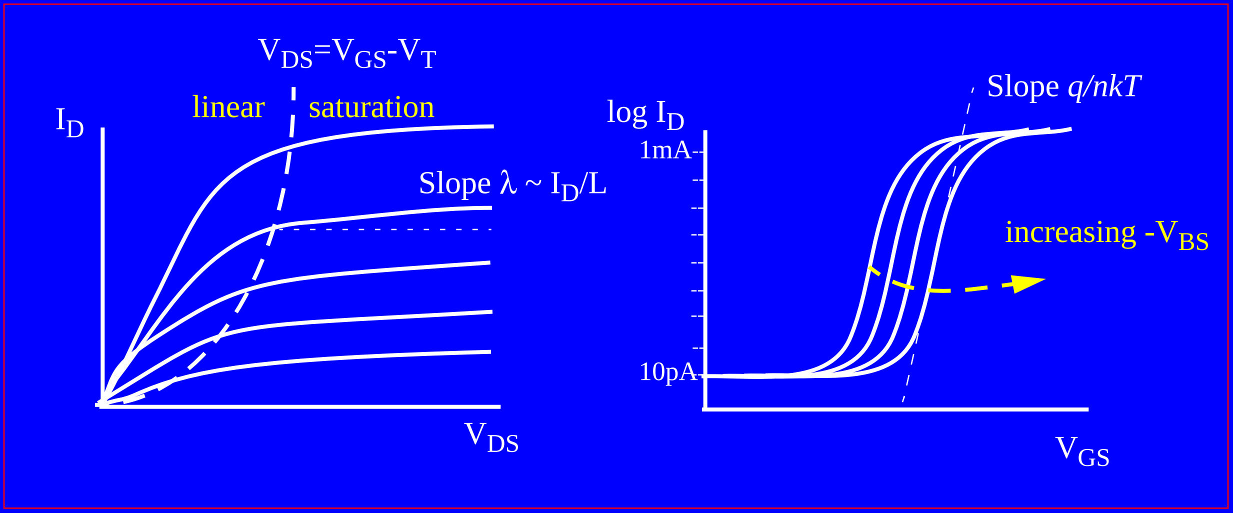
2. Weak inversion $V_{GS} - V_T < \dfrac{3kT}{q}$:

$$\boxed{\begin{aligned} I_D &= I_{D0}\frac{W}{L}\, e^{\left(\frac{qV_{GS}}{nkT}\right)} \\ \frac{g_m}{I_D} &= \frac{q}{nkT} \end{aligned}} \qquad (3)$$

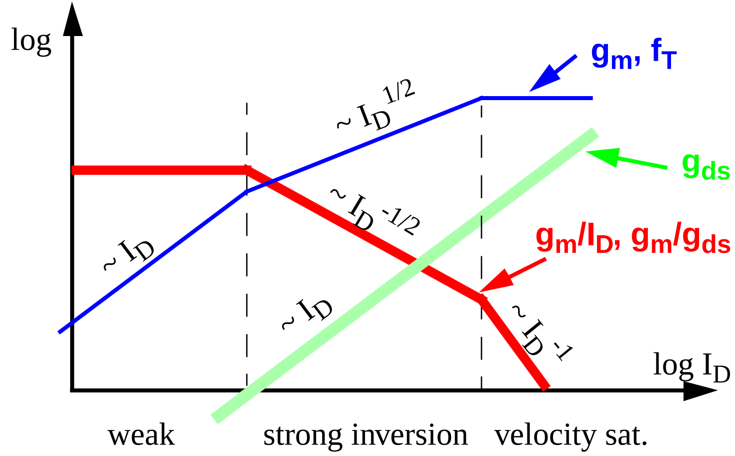
- best g_m/I_D
- poor f_T

Note: *n* is ratio of bottom (JFET)/top (MOS) gate control:

$$n = 1 + \frac{C_{BC}}{C_{GC}} = 1 + \frac{\sqrt{2\varepsilon q N_{SUB}}}{2C_{ox}\sqrt{2(\phi_F - V_{BS})}}$$; typically n~1.2 - 1.5

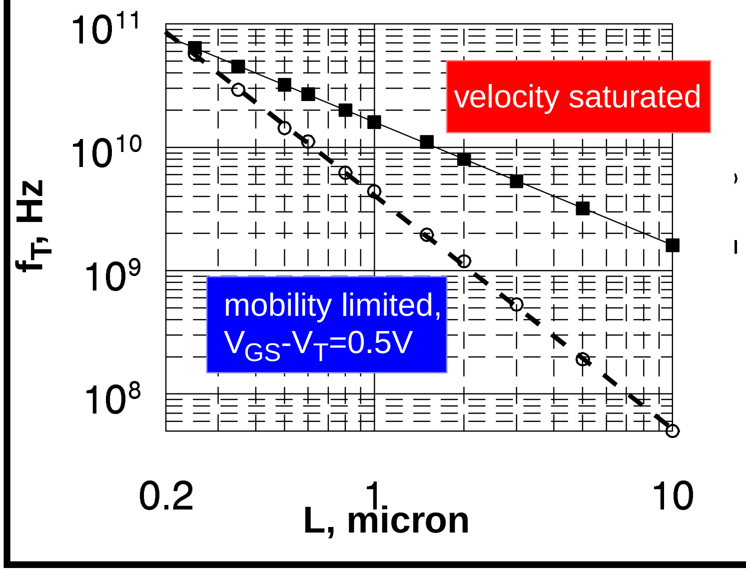


Regions of operation



- weak inversion best for gain
- strong inversion best for high frequency operation

Cutoff frequency



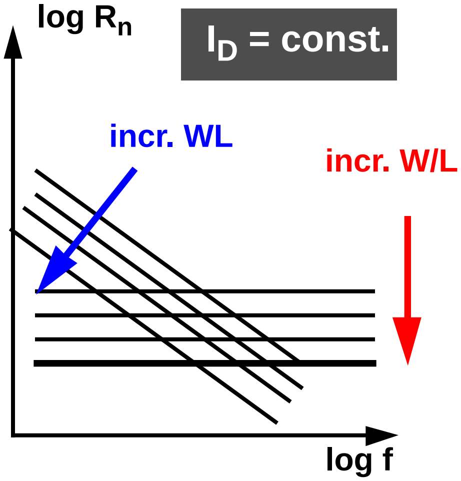
Noise

Drain current thermal noise: $i_n^2 = 8nkTg_m/3$

Flicker noise: $v_n^2 = 4kT\frac{\rho}{WLf}$

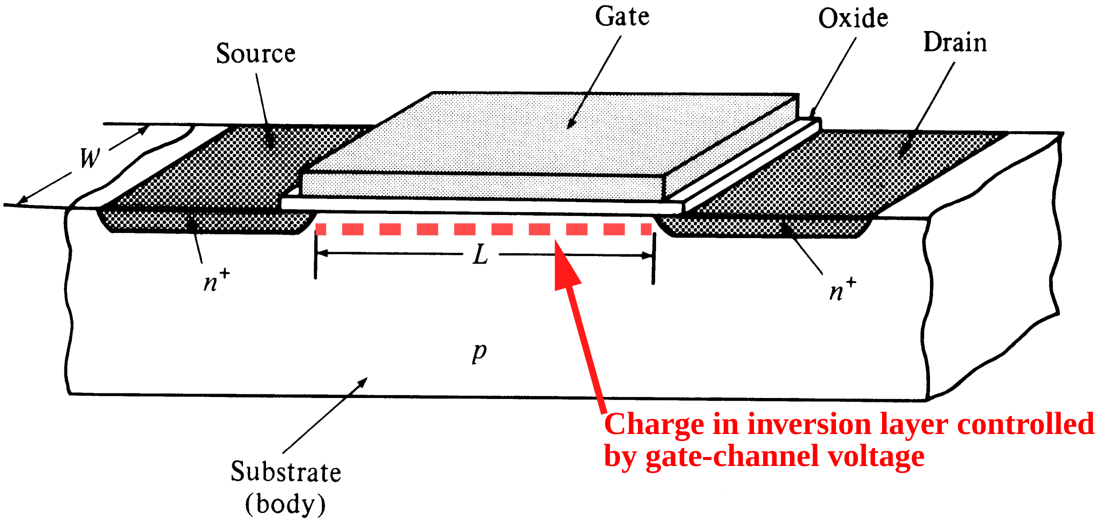
Input-referred noise voltage: $4kTR_n = v_n^2 + \frac{i_n^2}{g_m^2}$

Equiv. input noise resistance: $R_n = \frac{\rho}{WLf} + \frac{2}{3g_m}$

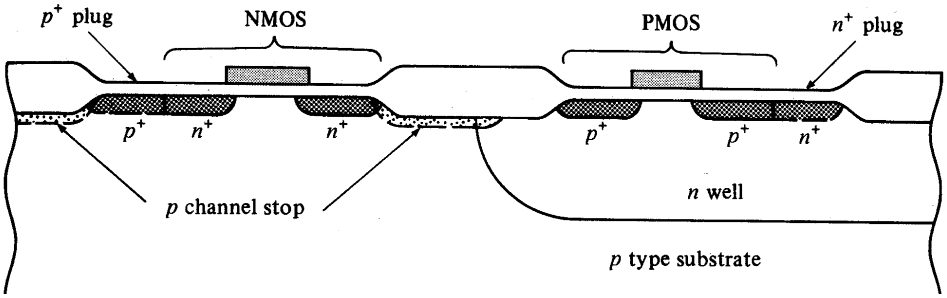


MOS Transistor

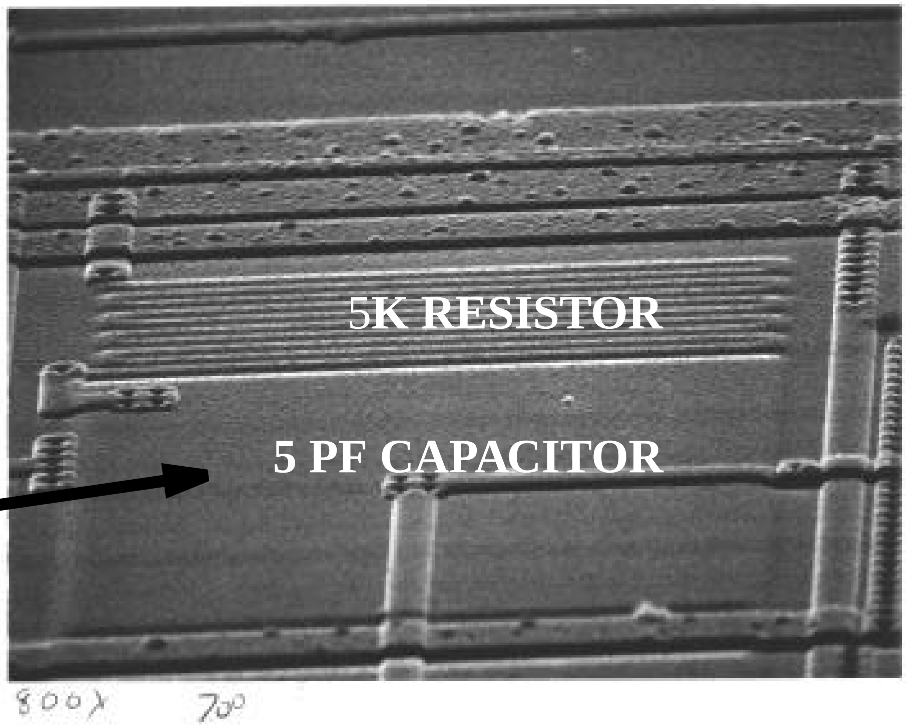
NMOS device



Cross-section of n-well CMOS process

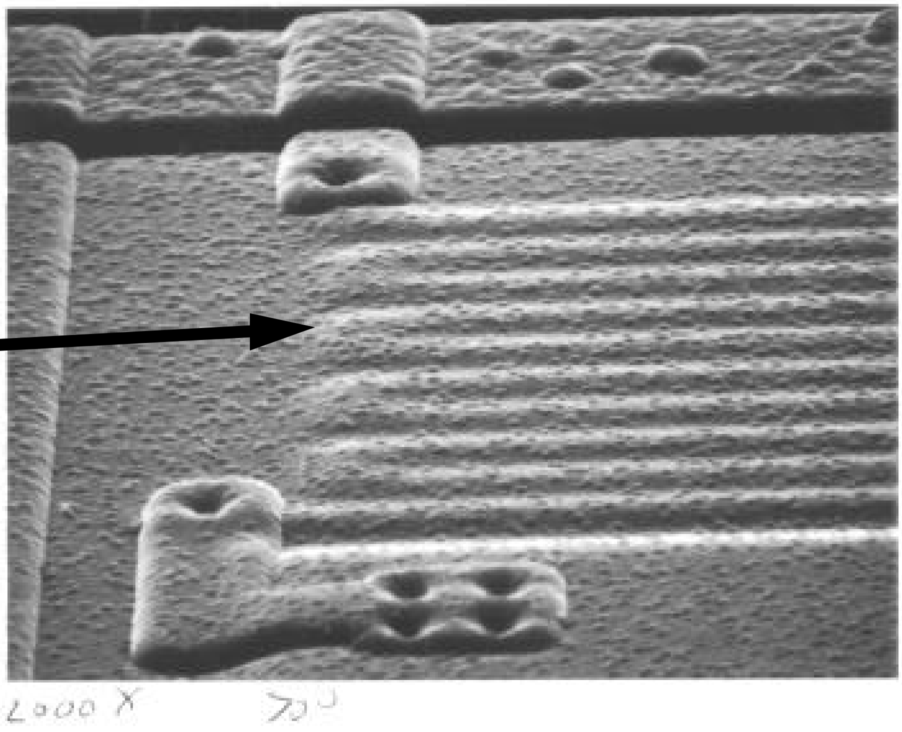


<u>800 X</u>



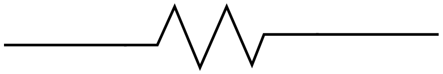
100 x 100 µm

<u>2000 X</u>

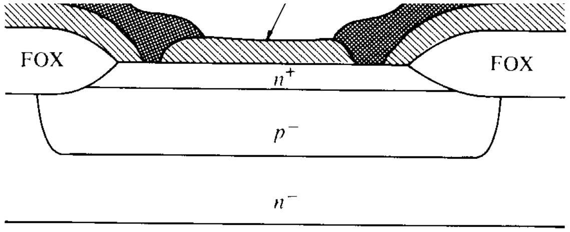


2 µm line/space

Resistors and Capacitors in CMOS Technology

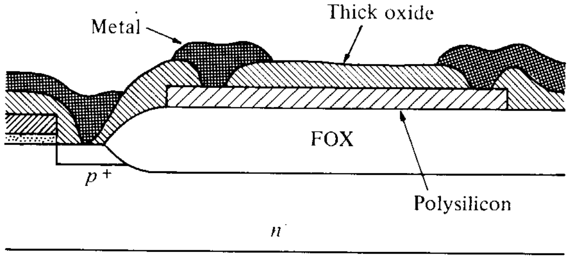


N+ DIFFUSION



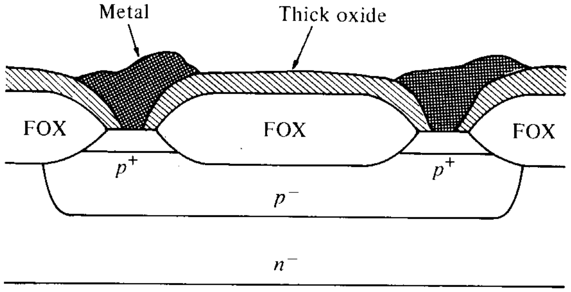
(a)

POLY



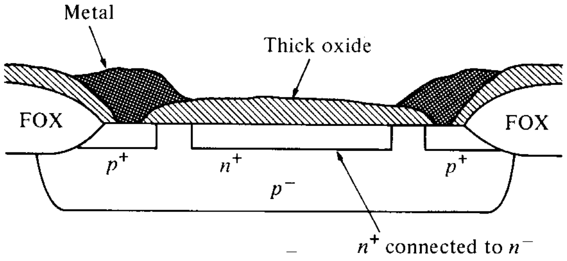
(b)

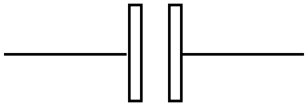
WELL

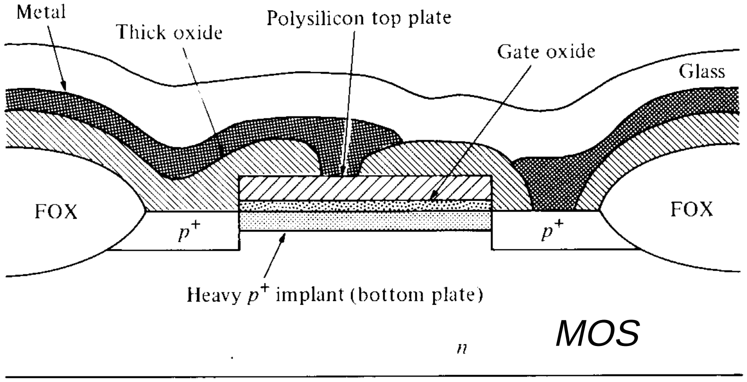


(c)

“PINCHED” WELL
= JFET

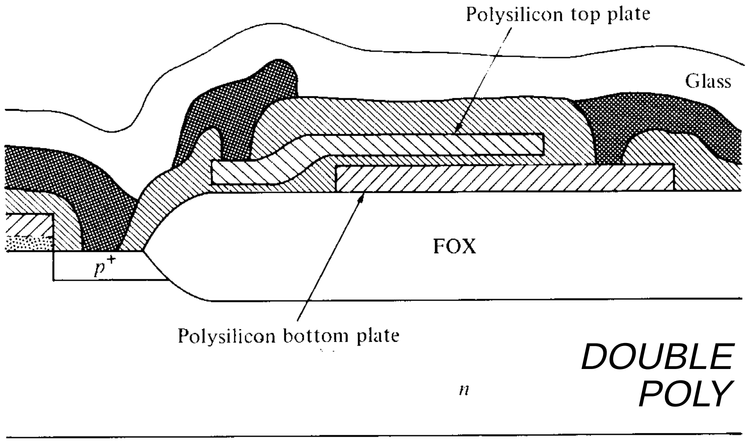






MOS

(a)



DOUBLE
POLY

Resistors

	Component	Range of Values	Absolute Accuracy	Matching Accuracy	Temperature Coefficient	Voltage Coefficient
Discrete	Carbon Composition	1 - 1G	5 -10	5 - 10	1500-5000 ppm/° C	-
	Metal Film	1 - 1G	0.1 - 1	0.1 - 1	25 - 100	5 ppm/V
	Precision Metal Film	1 - 1G	.025 - 1	0.025 - 1	5 - 25	0.1
	Thick Film	1 - 100M	can be trimmed	0.1	> 100	0
Monolithic CMOS	Diffused	10-100	35	2	1500	200
	Poly	30-200	30	2	1500	100
	Ion-implanted	0.5 -2K	5	1	400	800
	Well	1 - 10K	40	2	8000	10,000
	Units	**Ω, Ω/sq**	**%**	**%**	**ppm/° C**	**ppm/V**

Capacitors

	Component	Range of Values	Absolute Accuracy	Matching Accuracy	Temperature Coefficient	Voltage Coefficient
Discrete	Ceramic	$1 - 10^6$	5	5	0 - 30	-
Monolithic CMOS	Poly/poly	0.3 - 0.4	20	0.06	25	50
	MOS	0.35 - 0.5	10	0.06	25	20
	Units	**pf, fF/μm^2**	**%**	**%**	**ppm/°C**	**ppm/V**