Efficient Amplitude and Time Measurement ASIC with Analog Derandomization

…no photon left behind

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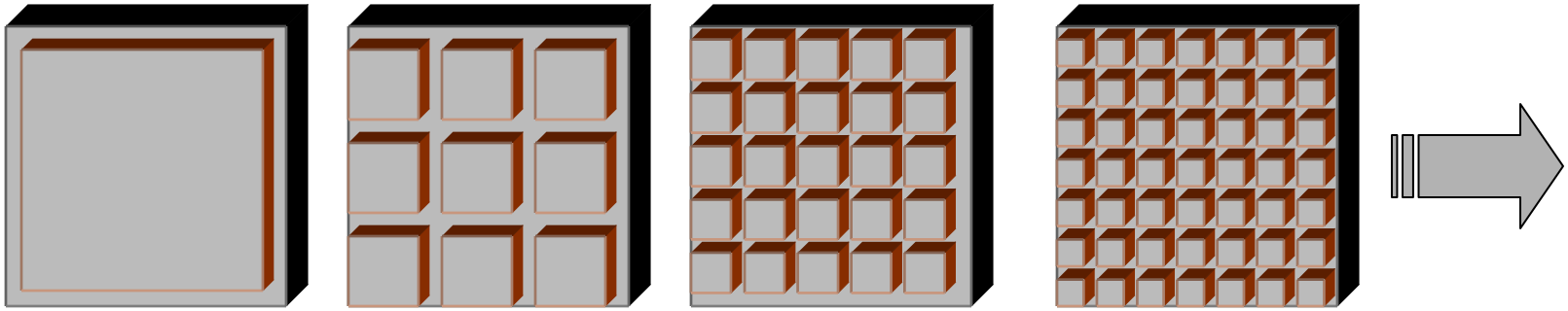
Highly segmented detectors



N=1 *N=9* *N=25* *N=49*

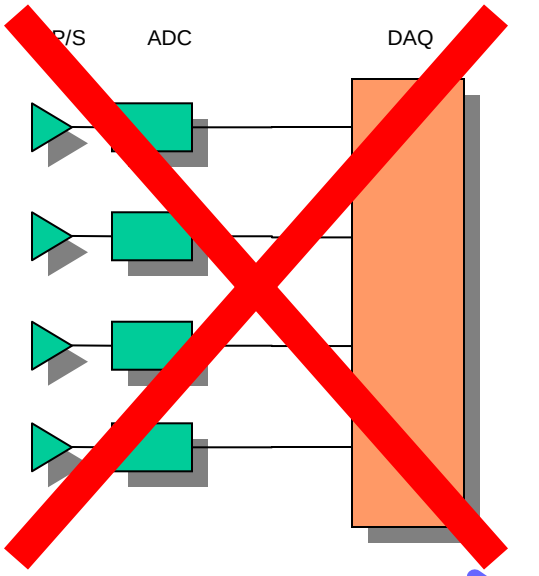
Benefits:

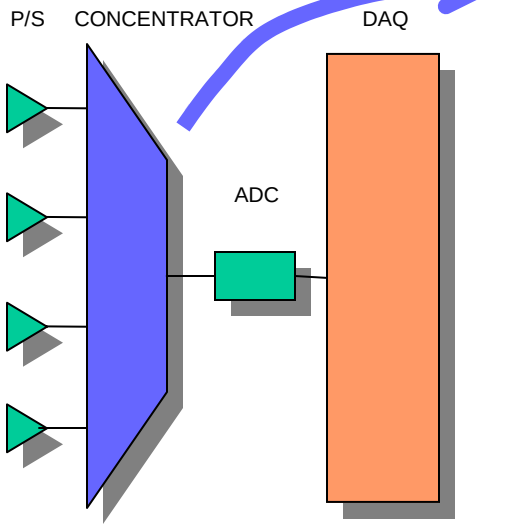
- Position Resolution
  - pixel pitch ~ $1/\sqrt{N}$
- Energy Resolution:
  - C_{DET} ~ 1/N
  - I_{DARK} ~ 1/N
  - Pulse Shaping time ~ N
- Rate capability
  - pileup ~ 1/N

Drawbacks:

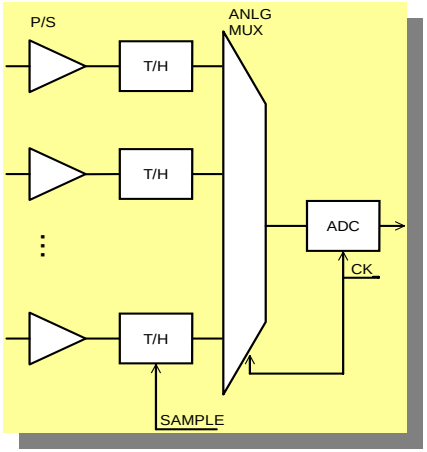
- Interconnect density
  - density ~ N
- Electronics channel count
  - cost ~ N
  - power ~ N

Data-concentrating architectures



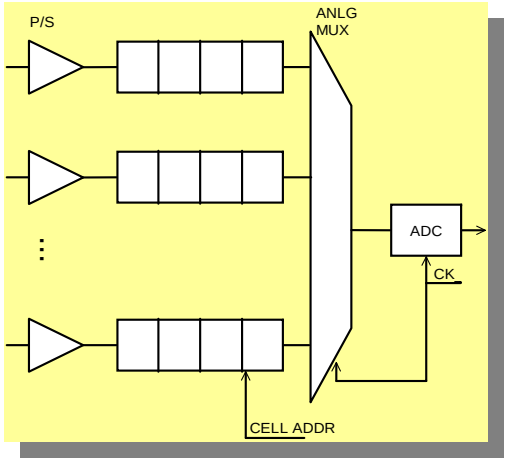


Track-and-Hold + Analog Multiplex



- unbuffered => deadtime
- long readout time
- needs accurate trigger

Analog Memory + Analog Multiplex



- can be deadtimeless
- complex control
- long readout time
- needs trigger + multiple samples

Both:

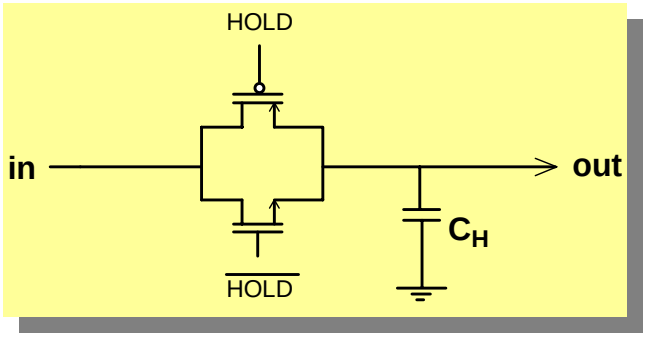
- **buy high integration at the price of efficiency**
- **problems in untriggered systems**

Requirements for fast, efficient multiplexing readout for random pulses

- Self-triggered sampling system
  - independent per-channel triggers
  - negligible time walk
- Sparse readout
  - skip unoccupied channels
- Buffer “memory”
  - analog storage for 4 – 8 events

Candidate sampling/memory cells in CMOS

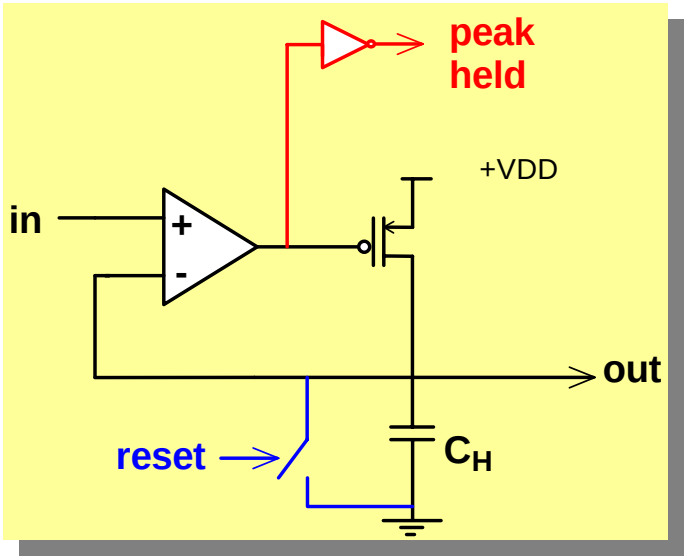
Sample/hold using switched capacitor



- small
- low-power

- timing of hold signal: needs CFD for walk-free operation
- switch charge injection
- poor drive capability: needs output amp

Peak Detector (PD)

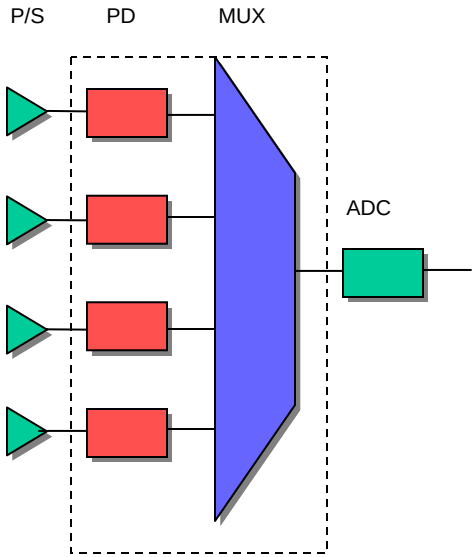


- self-triggered
- timing output
- feedback loop

- deadtime until readout reset
- poor drive capability
- accuracy impaired by opamp offsets, CMRR, slew rate

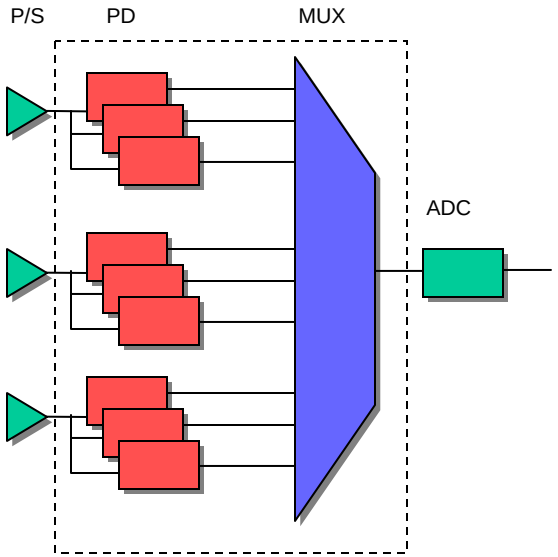
Derandomizing architectures

One PD per channel



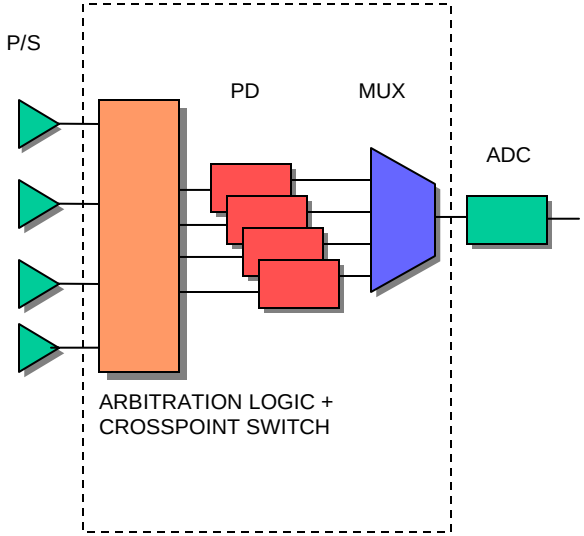
- self-triggering
- unbuffered -> deadtime
- long readout time

Multiple PDs per channel



- self-triggering
- buffered
- long readout time
- high power dissipation
  ($N_{PD} > N_{CHAN}$)

Multiple PDs shared by all channels

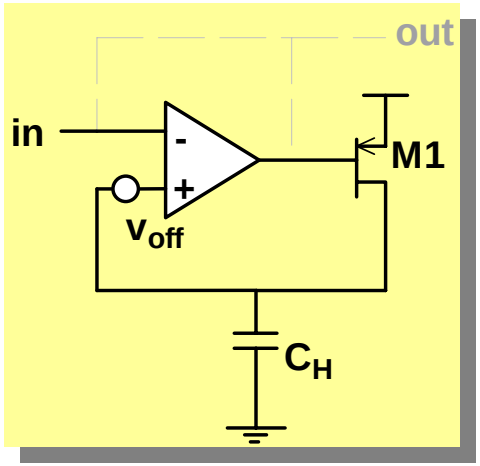


- self-triggering
- buffered
- reduced readout time
- reduced power dissipation
  ($N_{PD} < N_{CHAN}$)

Improved CMOS PD Using Two-Phase Configuration

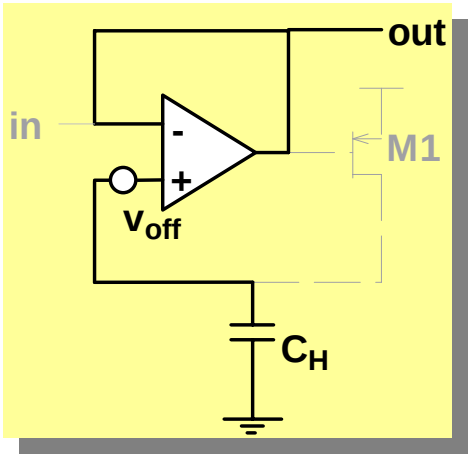
Write phase

- conventional peak detector
- M1: unidirectional current source
- voltage on C_H includes op-amp errors (offset, CMRR)

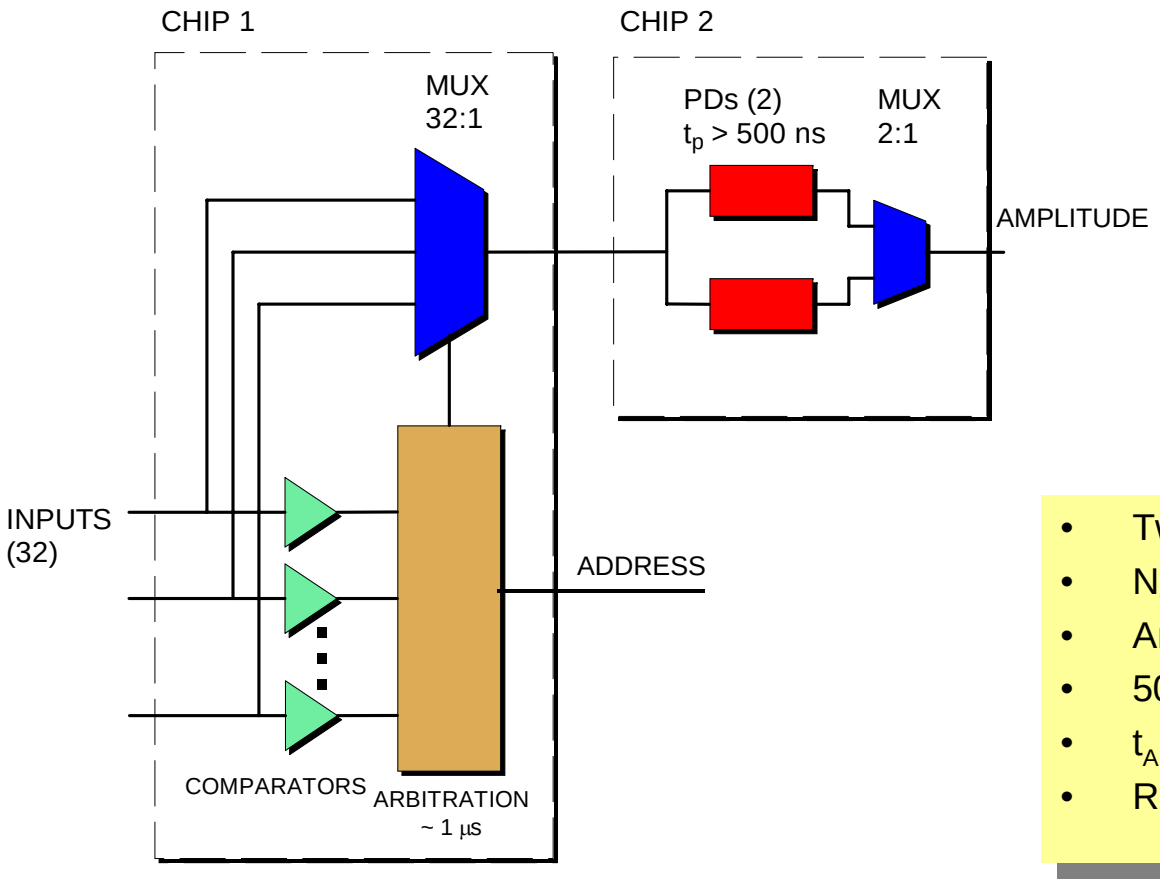


Read phase

- same op-amp re-used as unity-gain buffer
- same CM voltage
- ***op-amp errors cancel***
- enables rail-to-rail sensing
- provides good drive capability

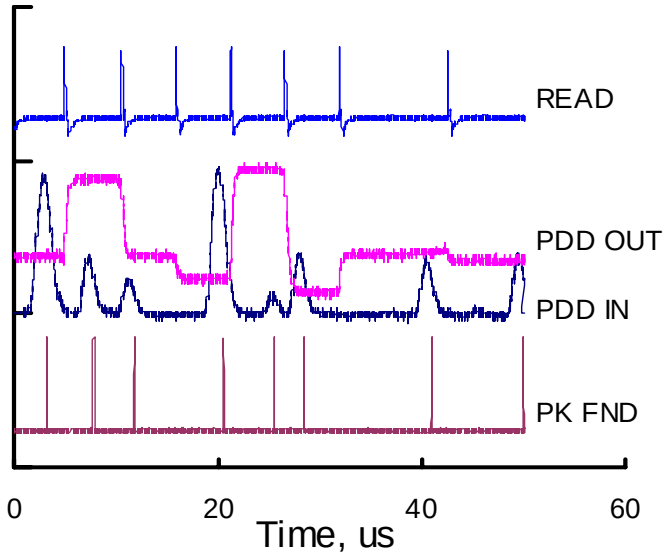


PDD-1 (Spring 2001)

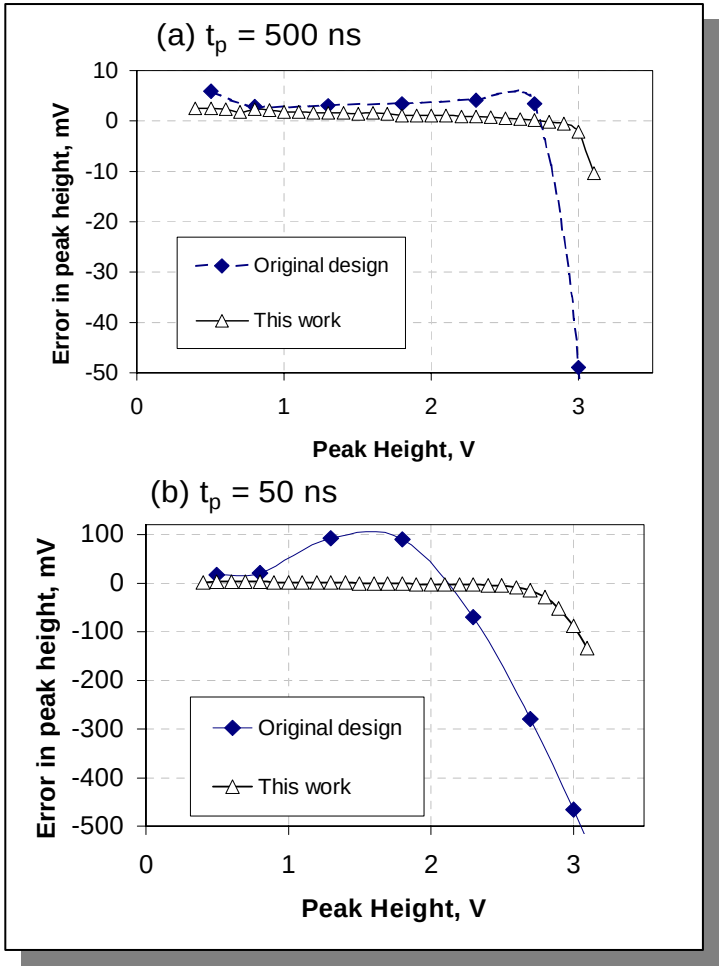


- Two-chip solution
- N_{CHAN} = 32, N_{PD} = 2
- Amplitude + address output
- 500 ns minimum pulsewidth
- t_{ARB} ~ 1000 ns
- Rate capability ~ 200 kHz

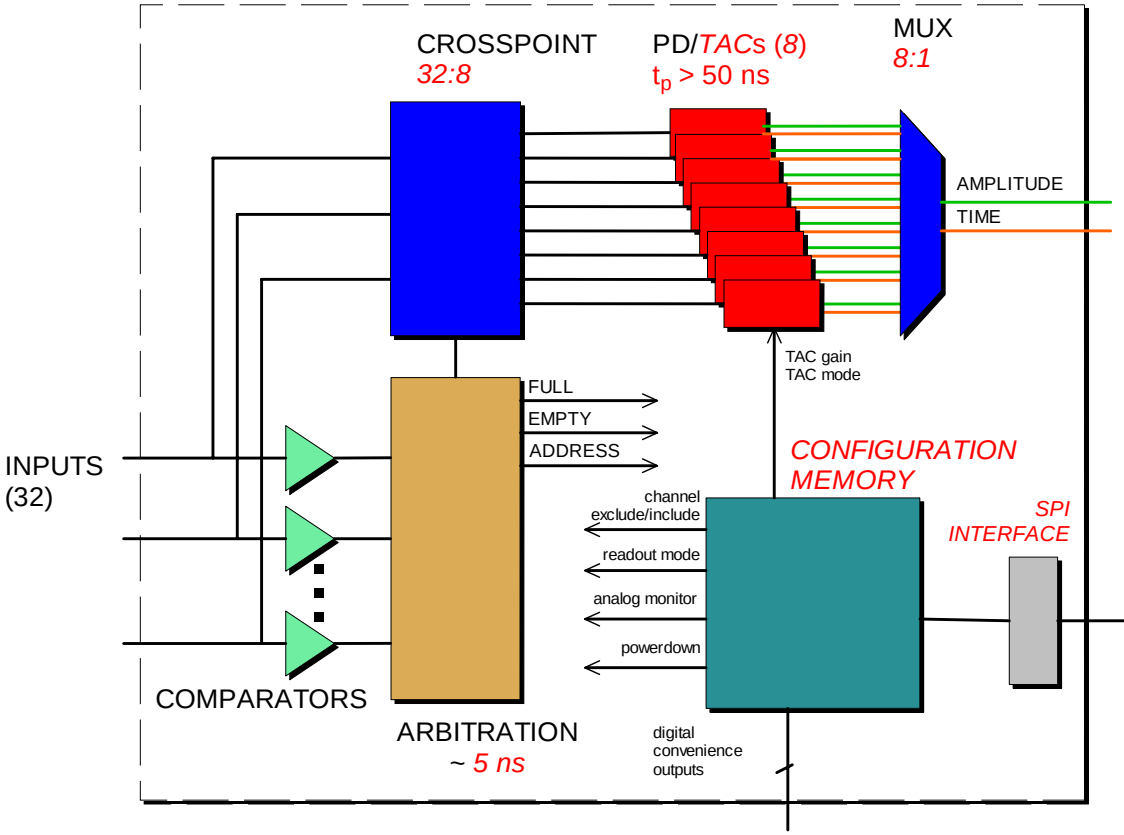
PDD-1: Results



Parameter:	Value: PDD-1 (PDD-2)
Technology	0.35 um CMOS DP4M
Supply voltage	3.3V
Input voltage range	0.3 - 3.0 V
Minimum pulse width	500 (50) ns
Absolute accuracy	0.20%
Linearity	0.05%
Droop rate	250 mV/s
Timing accuracy	5 ns
Power dissipation	3.5 (2.0) mW/chan



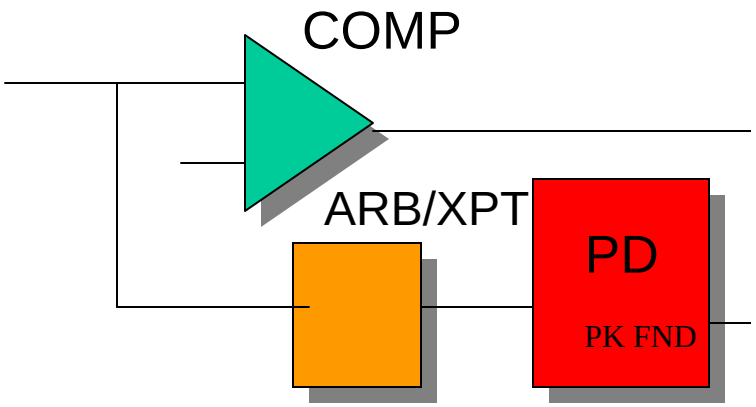
PDD-2 (Fall 2002)



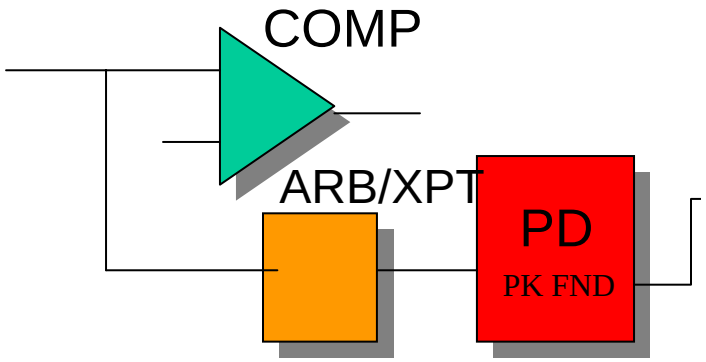
- One-chip solution
- N_{CHAN} = 32, N_{PD} = 8
- Dual-mode TAC
  - risetime
  - time of occurrence
- Amplitude, address, time outputs
- 50 ns minimum pulsewidth
- t_{ARB} ~ 5 ns
- Rate capability ~ 10 MHz
- SPI interface:
  - serial configuration of TAC gain and mode
  - arbitration locking
  - channel exclusion
  - powerdown
  - analog monitor
  - Digital convenience outputs (used for configuring companion amplifier chip)
- FIFO-like control and readout interface

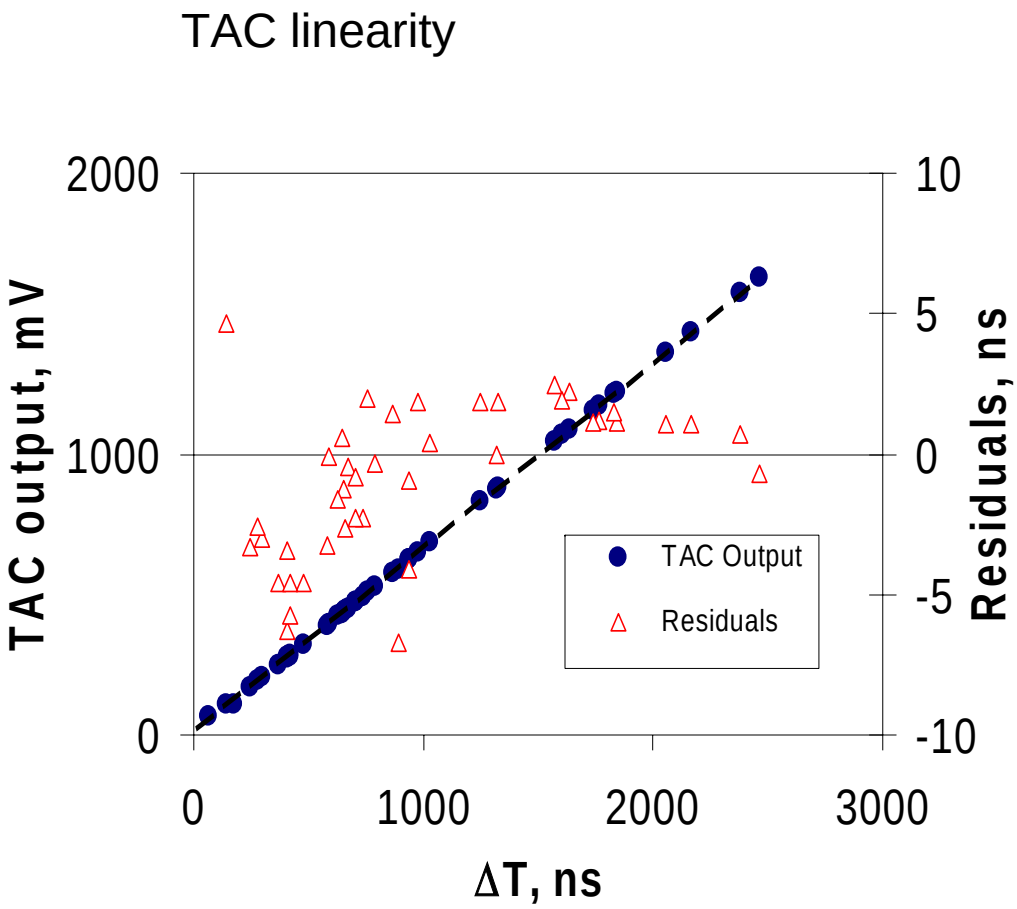
Combined PD/TAC

1. Risetime mode



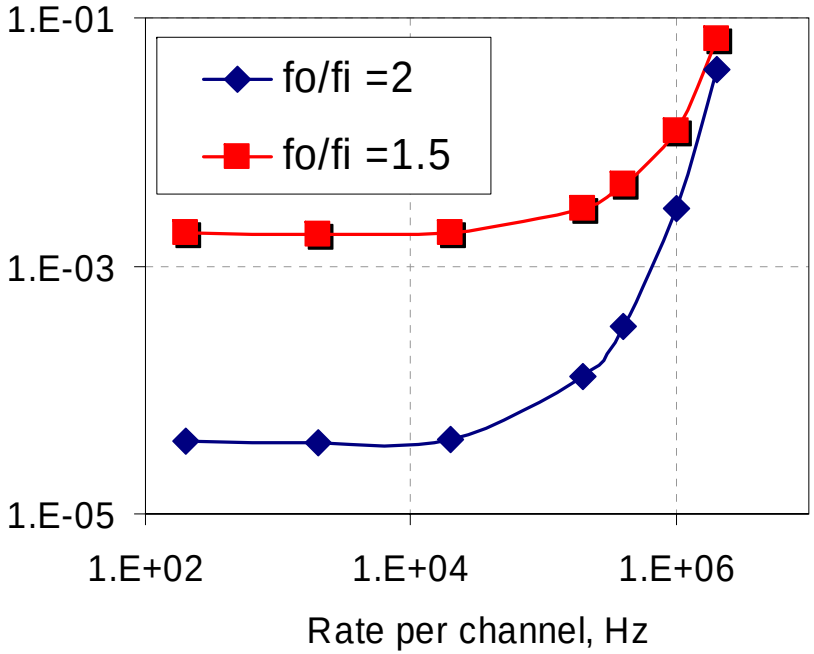
2. Occurrence time mode



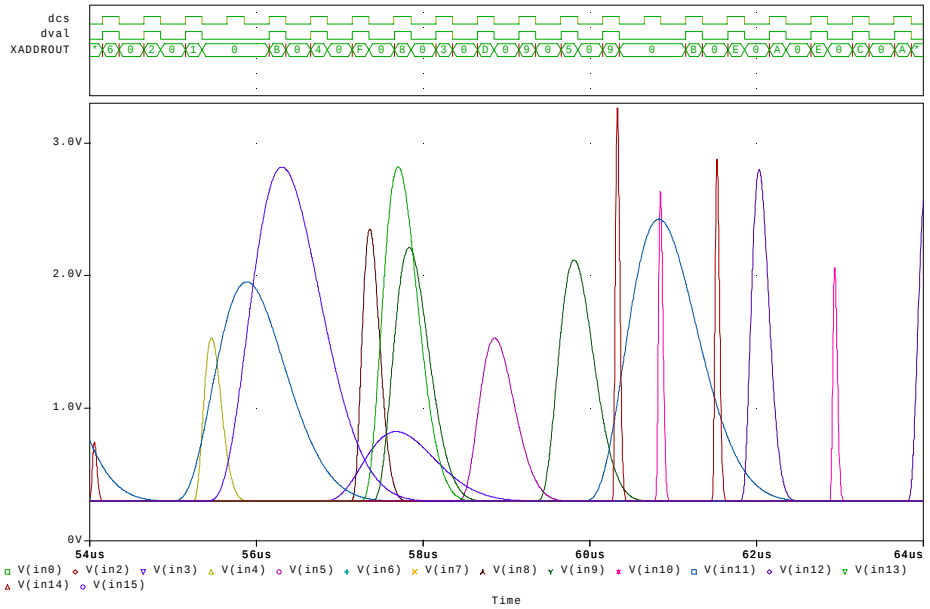


PDD-2: Simulation

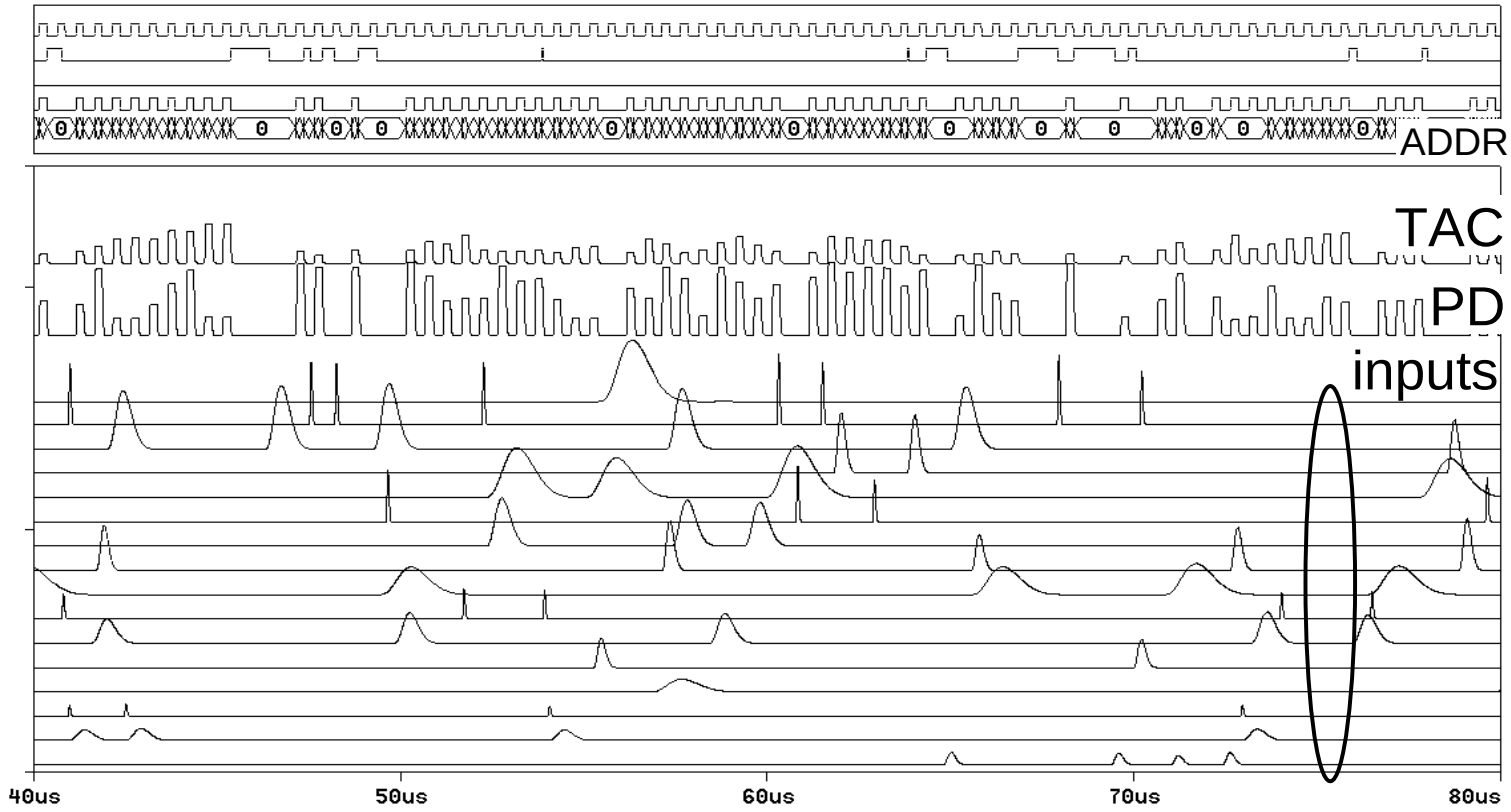
Inefficiency



SPICE simulation



PDD-2: SPICE simulation



1.6 Mcps input rate (16 channels)
2 MHz output clock
Poisson distribution of event times
Variation of pulsewidth, amplitude

Comparison of readout architectures

Architecture	Max. rate	No. digitizations per pulse	Example: N_{CH}=32, f_{mux}=5 MHz, N_{SAMP}=3, 1-ε = 99%	
			R_{max}	N_{dig}
Track/Hold + Mux	$\frac{f_{MUX} \cdot F(\varepsilon,1)}{N_{CH}}$	N_{CH}	23 kHz	32
Analog pipeline + Mux	$\frac{f_{MUX} \cdot F(\varepsilon,N_{BUF})}{N_{CH} \cdot N_{SAMP}}$	$N_{CH} \cdot N_{SAMP}$	52 kHz	96
PDD-2	$f_{MUX} \cdot F(\varepsilon,N_{PD})$	1.2 ~ 2	3.3 MHz	1

f_{MUX}	Analog multiplexer rate
N_{CH}	No. of channels/chip
N_{BUF}	No. of buffer cells in pipeline
N_{PD}	No. of peak detectors in PDD
N_{SAMP}	No. of pipeline samples read out per pulse
$F(\varepsilon,N)$	Poisson factor to get inefficiency ε given N buffer locations: For ε = 1%, F(ε,1) ~ 0.15, F(ε,8) ~ 1

Summary

- New architecture for efficient readout of multichannel detectors
  - *Self-triggered and self-sparsifying*
  - *High efficiency at high concentration ratio*
- Based on new 2-phase peak detector combined with dual-mode TAC
  - *High absolute accuracy (0.2%) and linearity (0.05%), timing accuracy (5 ns)*
  - *Low power (2 mW)*
- Peak detector – derandomizer (PDD-1) with 2-event buffer demonstrated:
  - *First step towards data-driven analog FIFO readout*
  - *Rate capability improvement over present architectures*
- PDD-2 (in design):
  - *Accepts pulses down to 50 ns peaking time*
  - *Crosspoint switch and 8-event buffer for high efficiency*
  - *TAC for simultaneous amplitude, time, and address measurement*