ATLAS CSC Electronics

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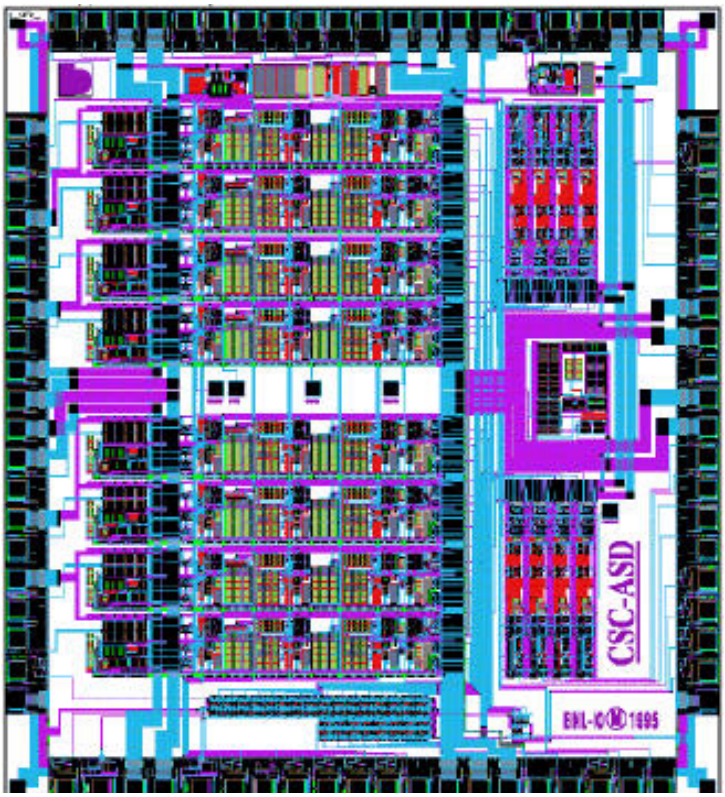
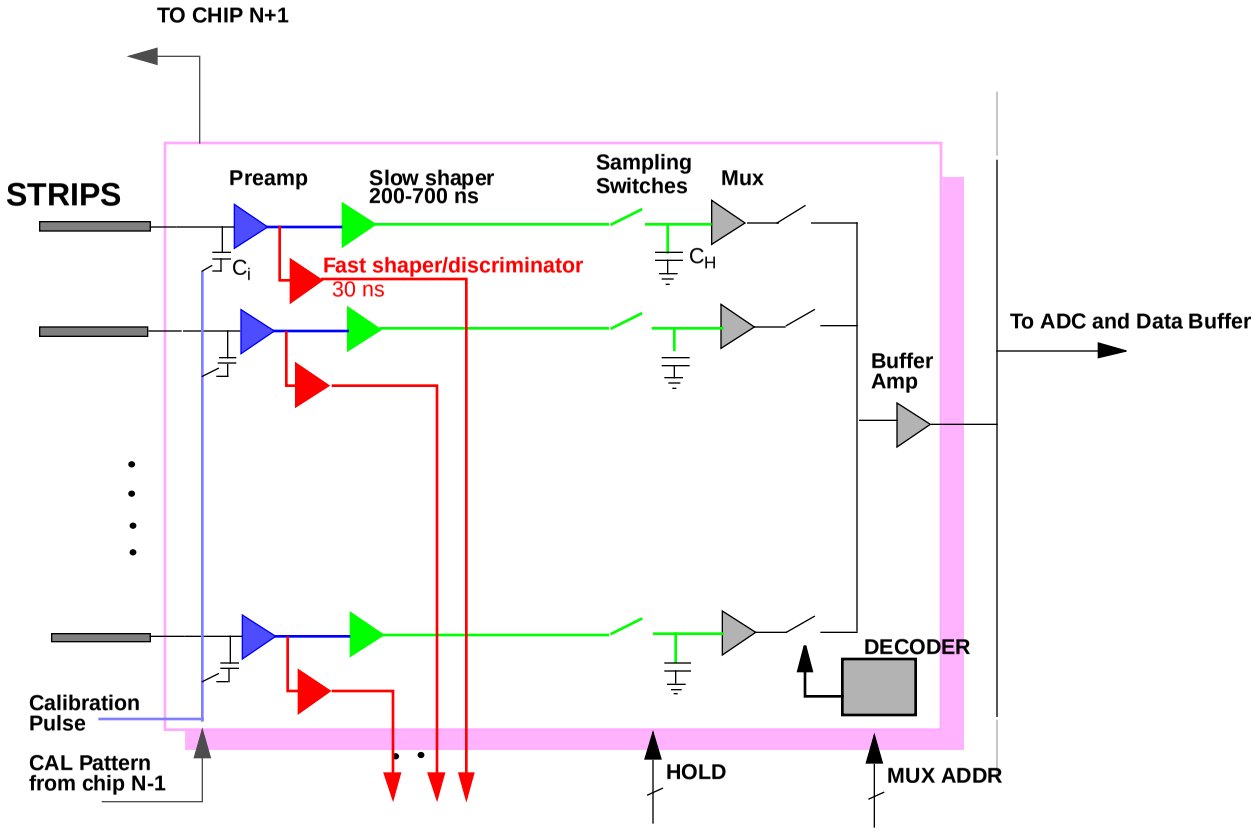
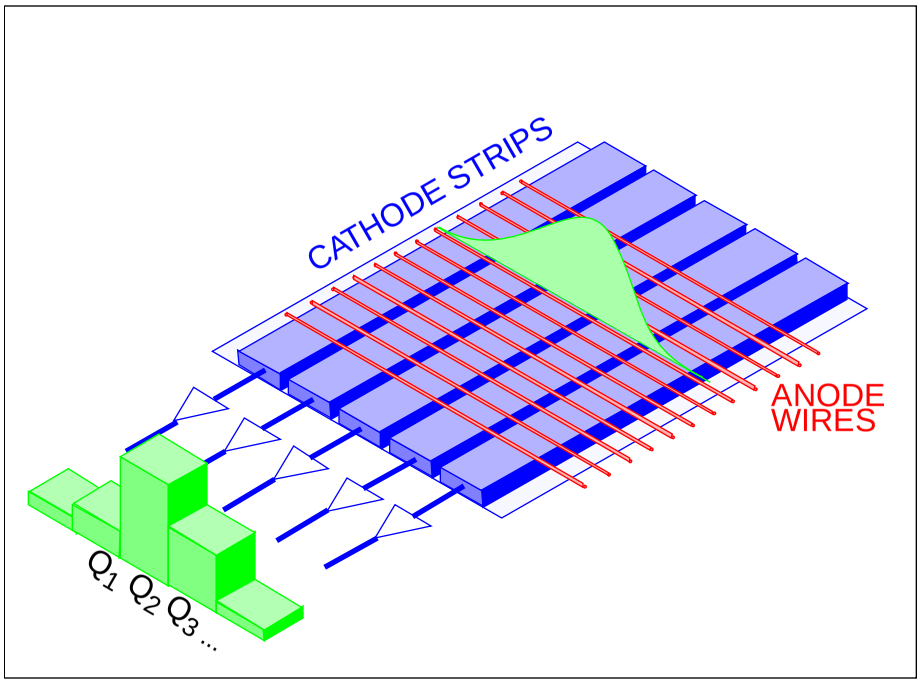
NAME	IC34
LAYOUT (20:1 SCALE)	
EXPERIMENT	ATLAS
SUB-DETECTOR	CATHODE STRIP CHAMBER (MUON ENDCAP)
C_{DET} RANGE	40 - 150 PF
CIRCUIT	CALIBRATION, AMPLITIDE (PREAMP/SHAPER, TRACK+HOLD, MUX), TIMING(CONSTANT FRACTION DISCRIMINATOR)
NO. CHANNELS	8
CHIP SIZE	4.75MM X 5.29MM
PACKAGE	84-PIN CERAMIC J-LEADED CHIP CARRIER
GAIN	5 - 20 MV/FC, PROGRAMMABLE IN 4 STEPS
PULSE SHAPE	BIPOLAR SEMIGAUSSIAN WITH 130 - 550 NSEC PEAKING TIME, PROGRAMMABLE IN 4 STEPS
SIGNAL	TO 250 FC
NOISE	1800 ELECTRONS R.M.S. (WITH FASTEST SHAPING, C_{DET} = 65 PF)
POWER	70 MW/CHANNEL
COMMENT	FACILITATES DATA-DRIVEN READOUT ARCHITECTURE (NO ANALOG PIPELINE)

Track-and-Hold Readout Electronics -- Front End ASIC



- Similar to AMPLEX
- Preamp sized for high capacitance
- 2 μm CMOS
- Fast shaper/discriminator on each channel
- Digitally programmable gain and shaping time

Cathode Strip/Pad Chambers

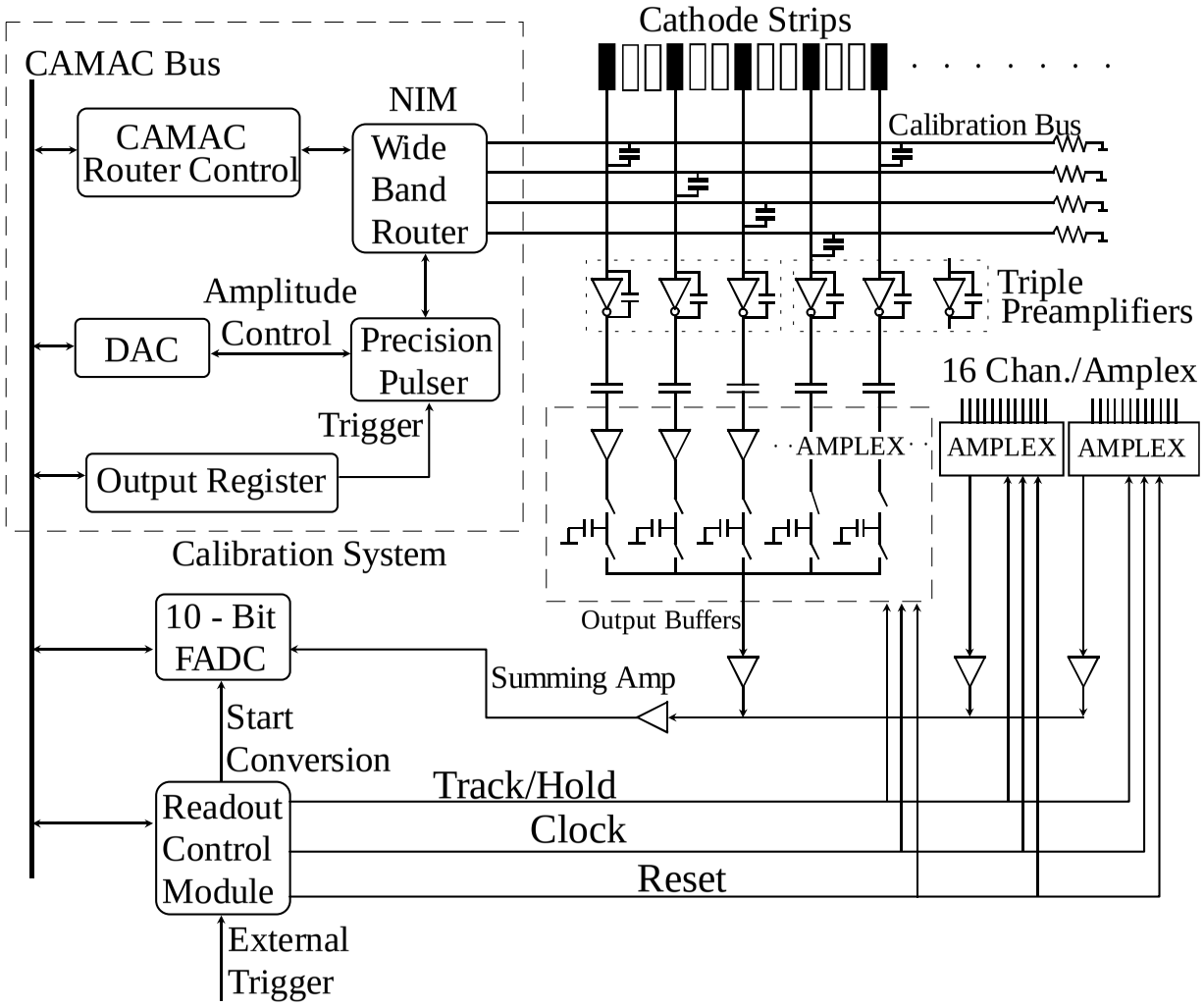


- Follow up on Development for SSC/GEM
- Currently in the design of CMS, ATLAS, and PHENIX
- Under Consideration in LHC-B

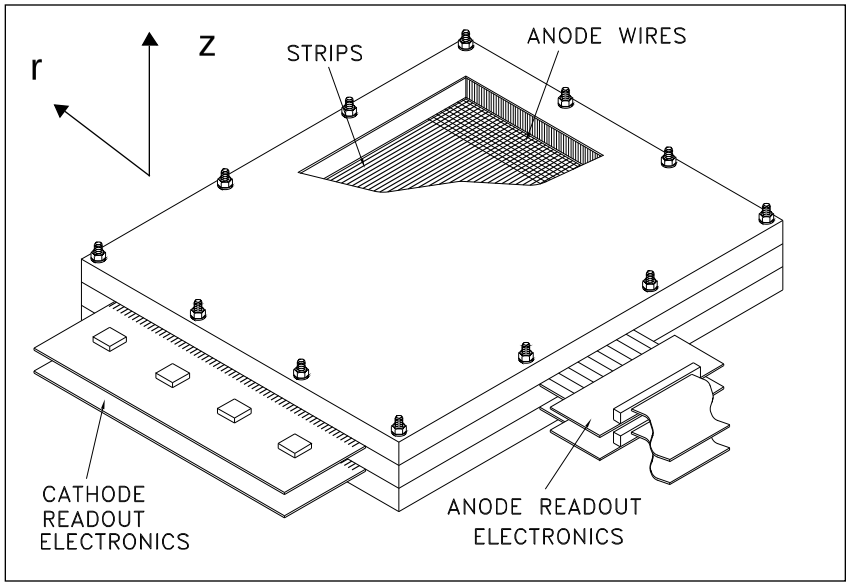
PROPERTIES

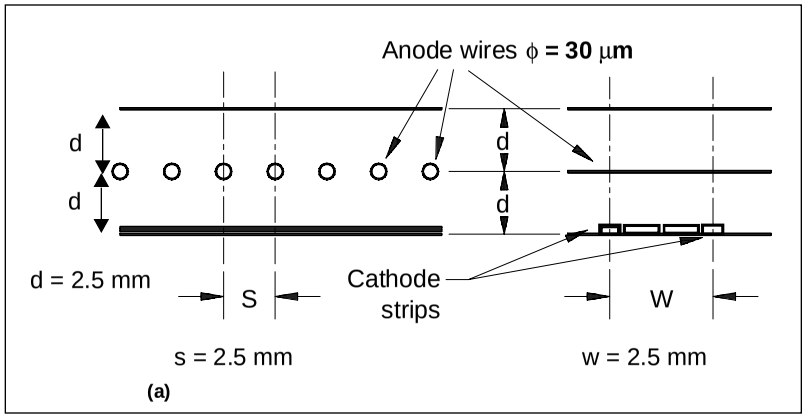
- High Resolution for momentum reconstruction (~ 50 mm)
- Transverse coordinate (~1mm - 1cm)
- Timing (~ 4 ns)
- Trigger primitives
- Almost arbitraty segmentation of cathodes
- Measured sensitivity to:
  - neutrons ~10^{-4}
  - photons ~10^{-2}

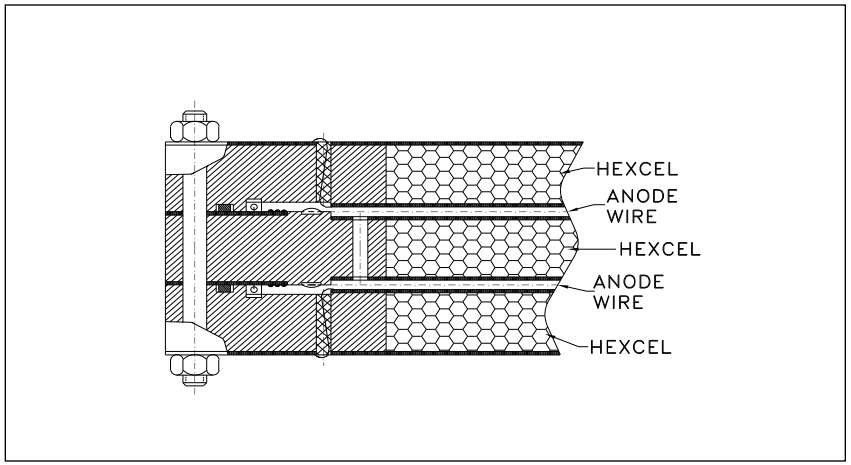
RD5 Data Acquisition System

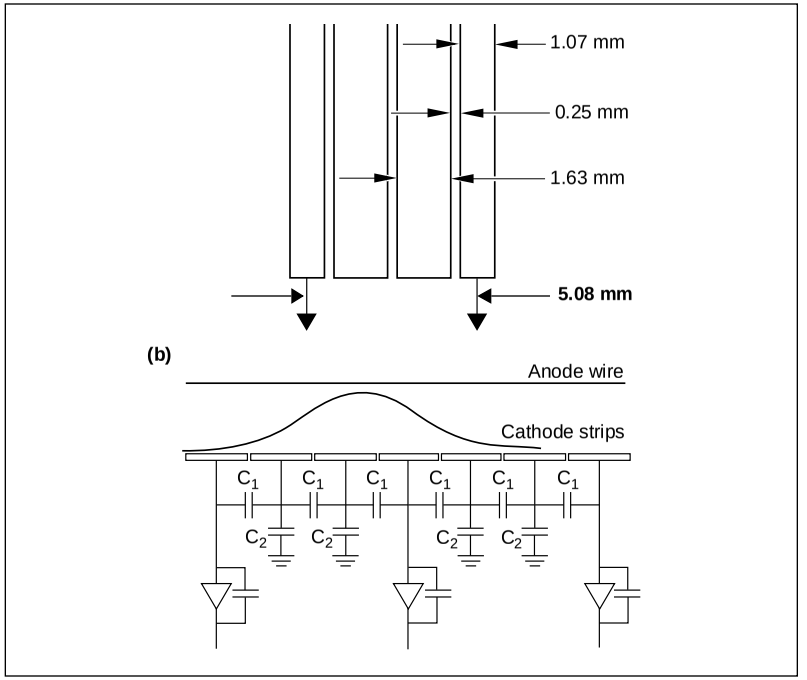


Chamber Construction

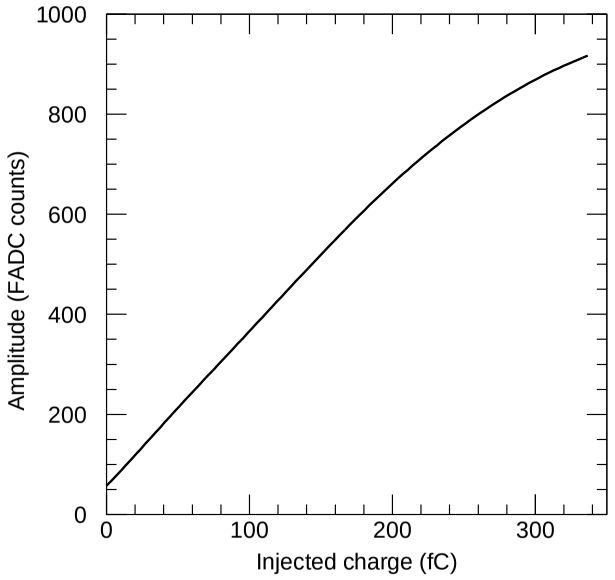


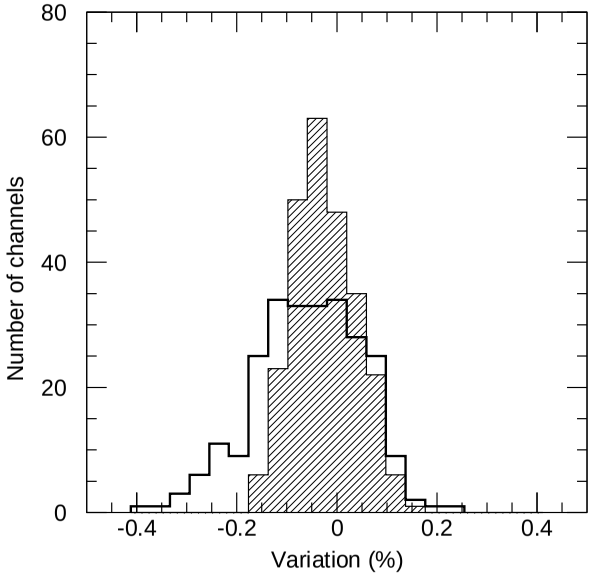






Calibration





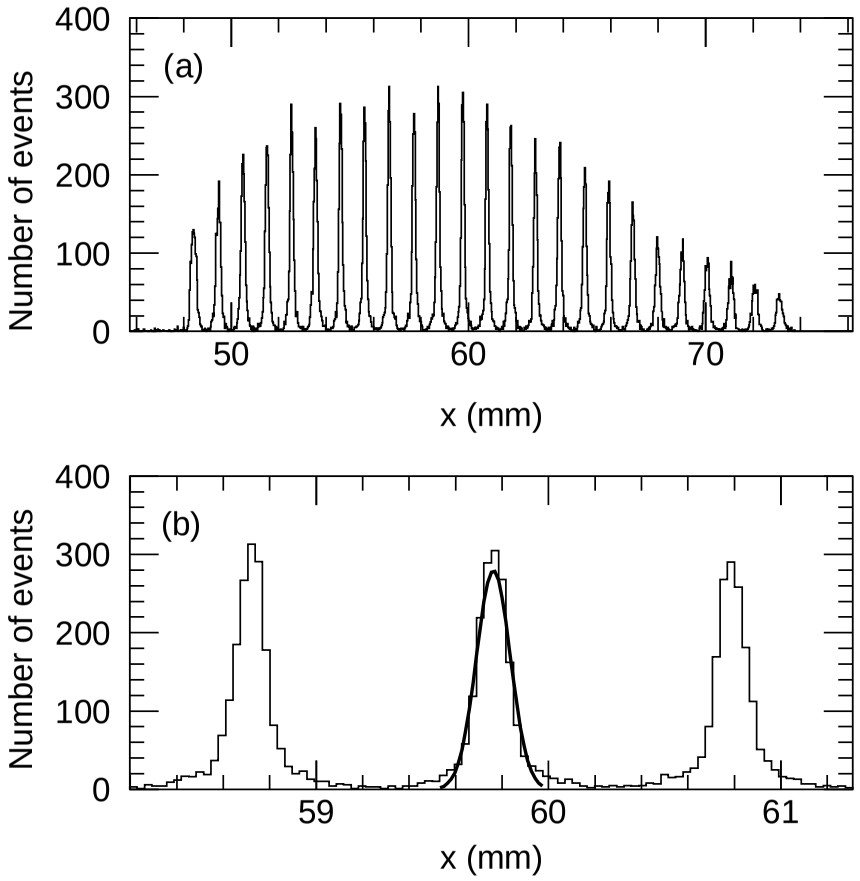
Procedure:

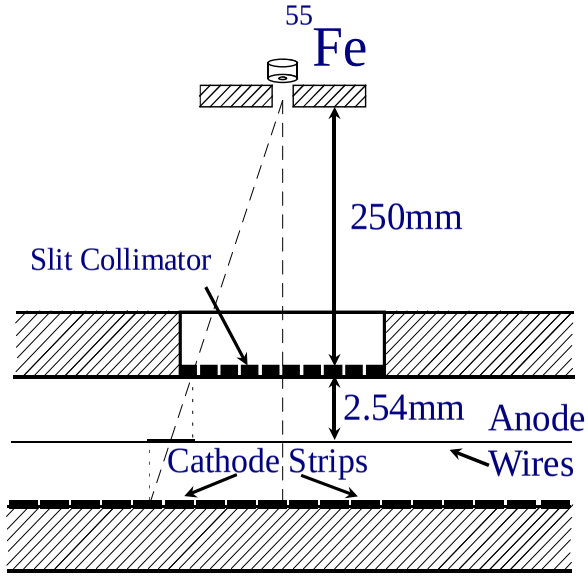
- 0.7pF, 1% tolerance capacitors on every channel
- groups of every 4th channel pulsed at a time
- polynomial fit
- corrected for capacitor variations by second "individual" calibration with same capacitor on every channel
- track-and-hold delay skew held to < 20 ns
- cross-talk correction for channels within a chip

Difference between expected and measured charge:

shaded histogram: just after the calibration
open histogram - one day after the calibration

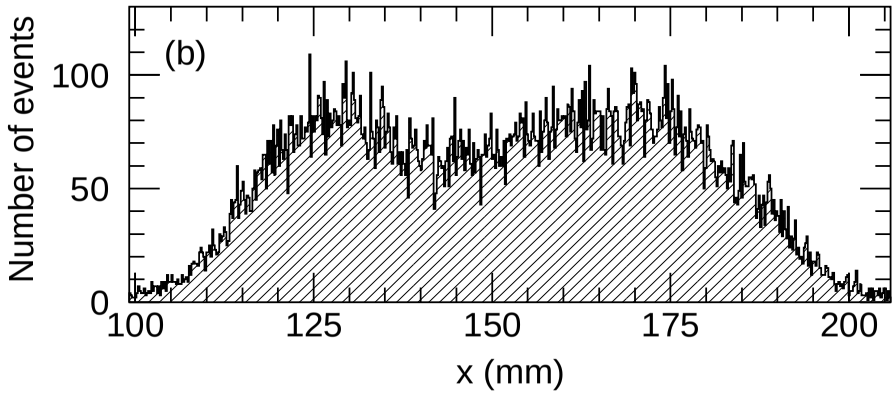
^{55}Fe Results



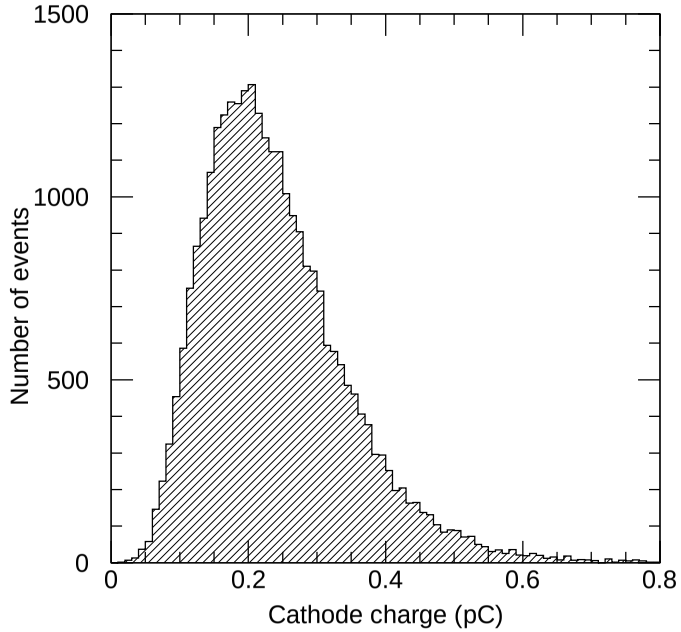


X-ray position spectrum from slit collimator (corrected for parallax)

Measurements with High-Energy Muons



Beam Profile

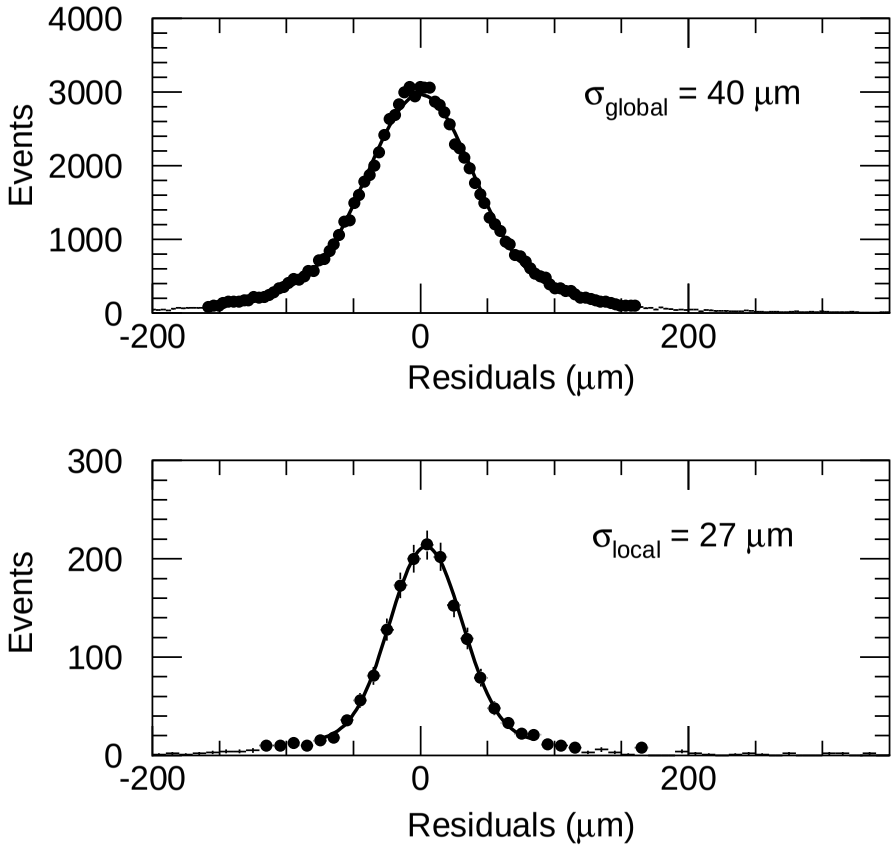


Charge Distribution

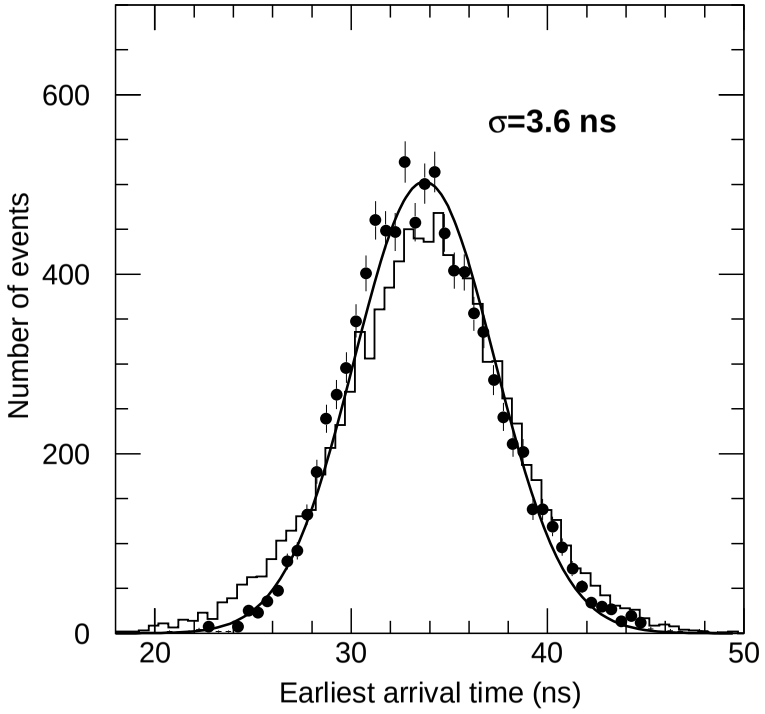
RD5 Results

Measurements with High-Energy Muons

Position Resolution



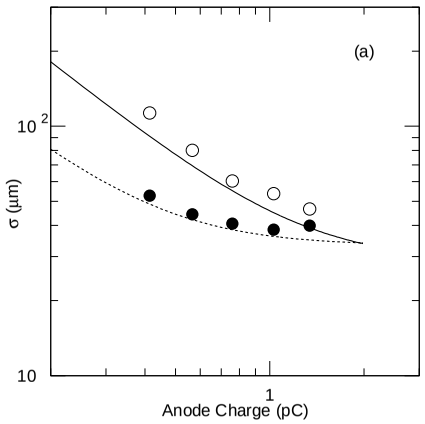
Time Resolution



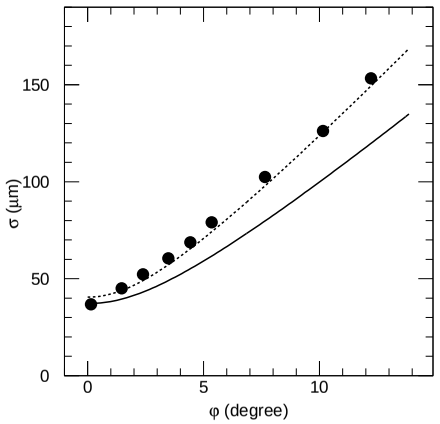
RD5 Results

Measurements with High-Energy Muons

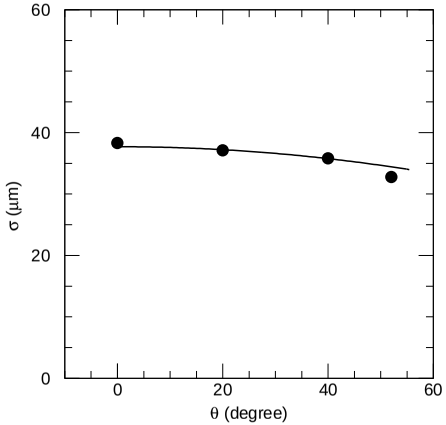
Position Resolution



vs. Anode Charge



vs. Beam-to-Wire Angle

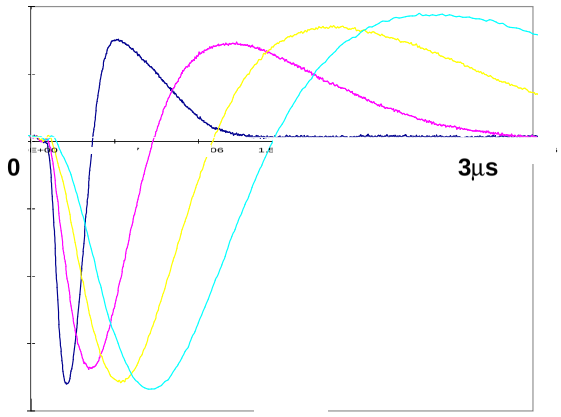


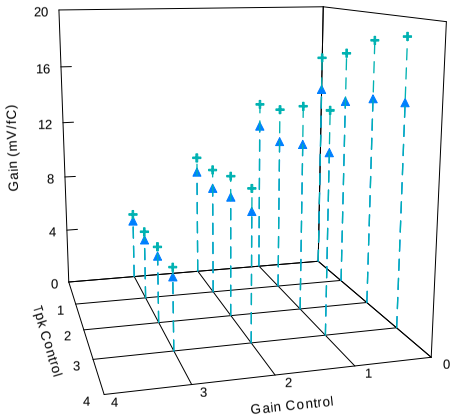
vs. Beam-to-Strip Angle

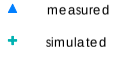
RD5 Results

CMOS Track-and-Hold IC Results

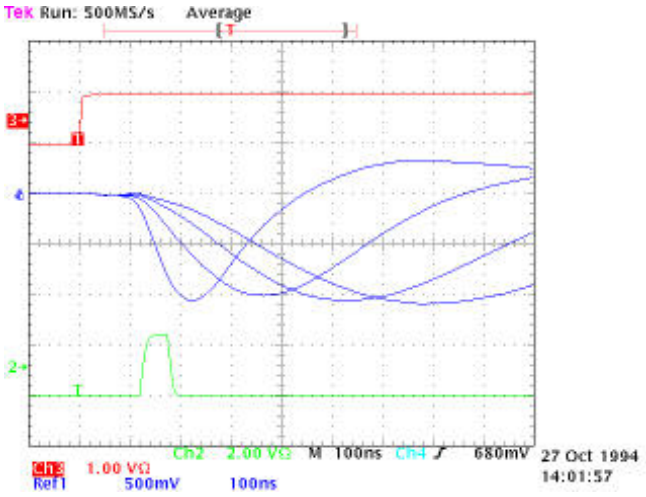
Gain and Shaping Time Control

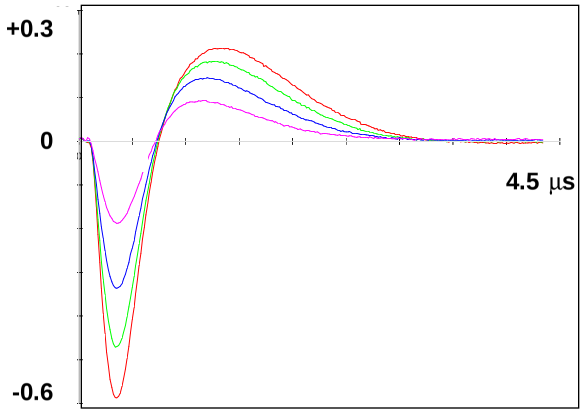


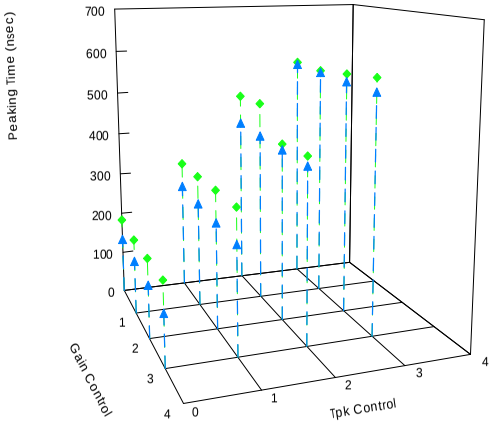


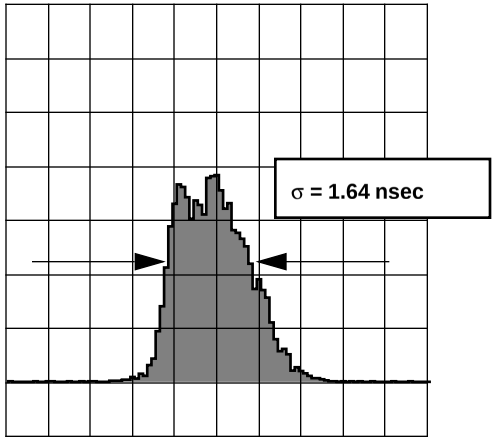


Discriminator





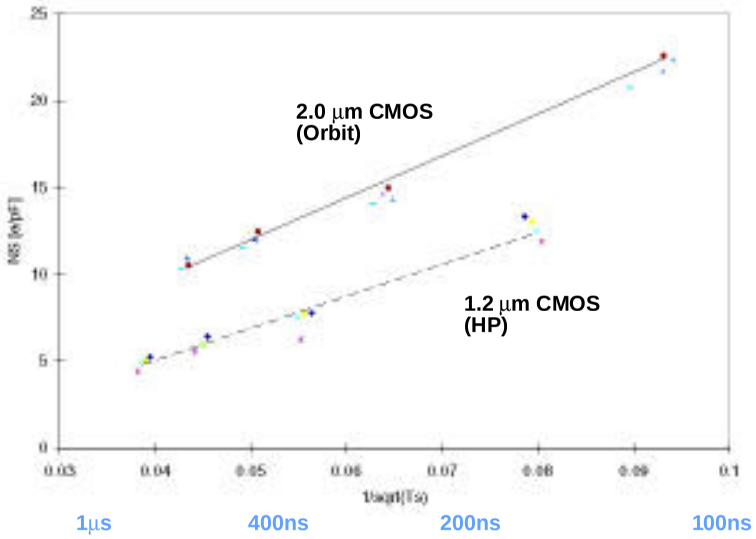


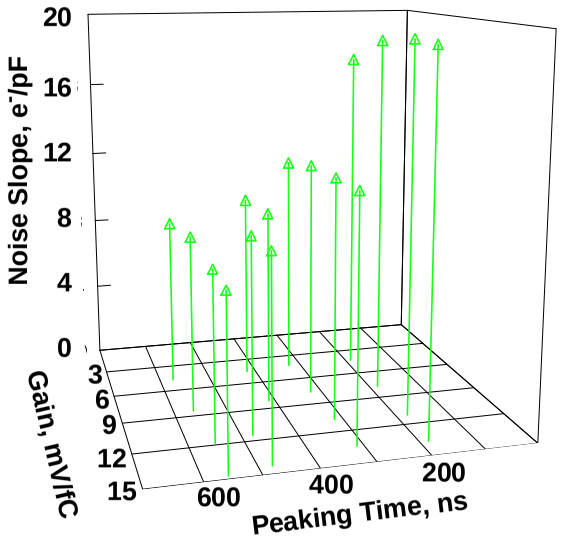


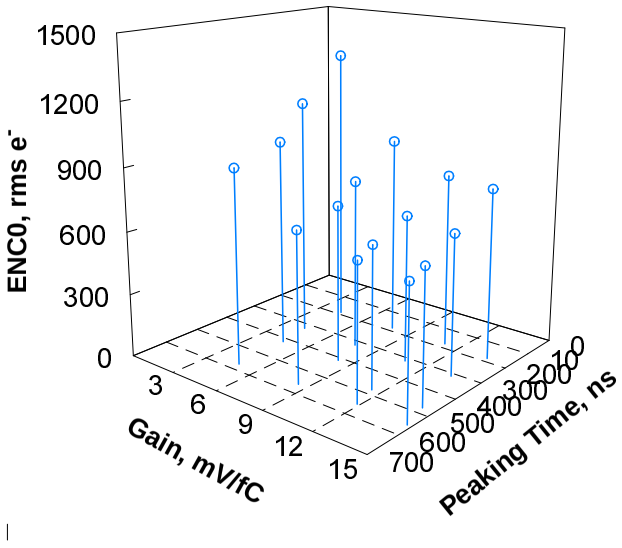
1 nsec/div HOR

CMOS Track-and-Hold IC Results

Noise



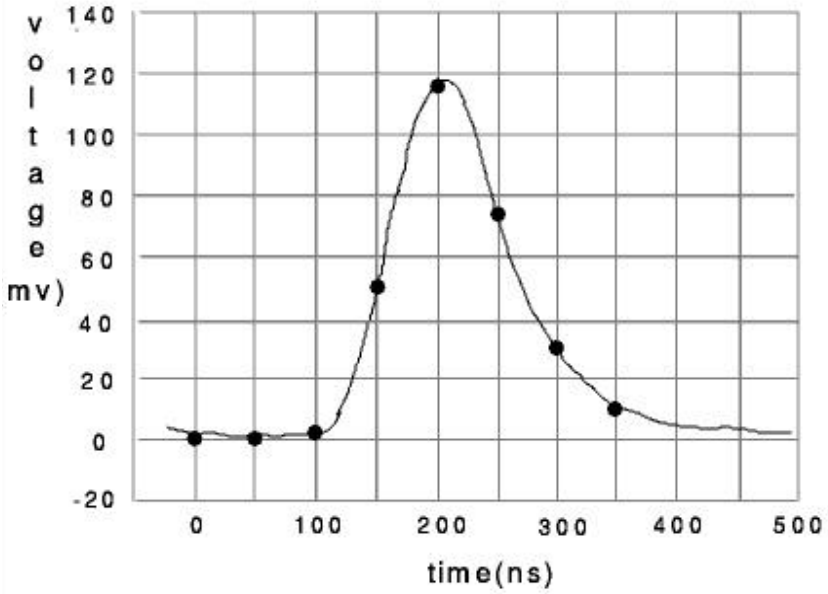




$$ENC = ENC_0 + NS*C_{DET}$$

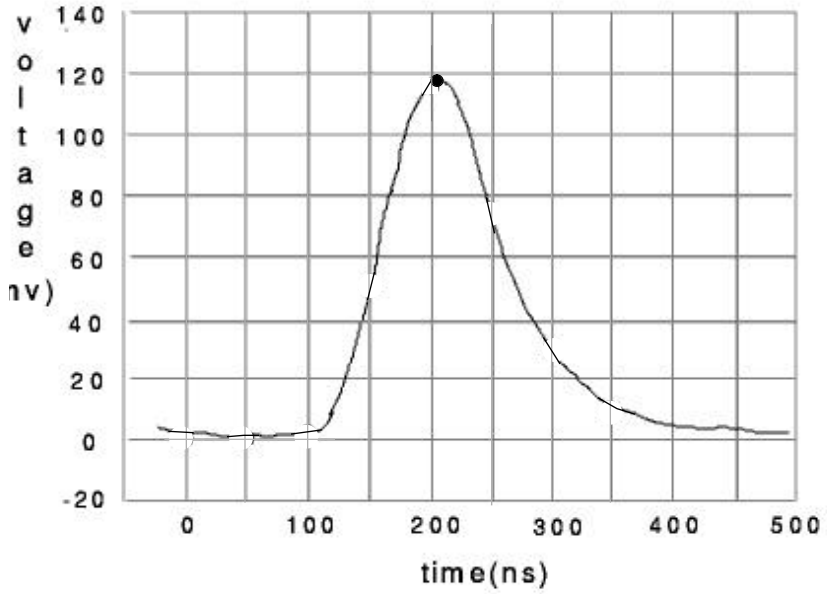
Sampling Architectures

Clock-Driven Sampling



- waveform samples continuously written to capacitor array
- 5-10 samples read out
- can be deadtimeless
- no discriminators required
- deconvolution of overlapping pulses possible (?)

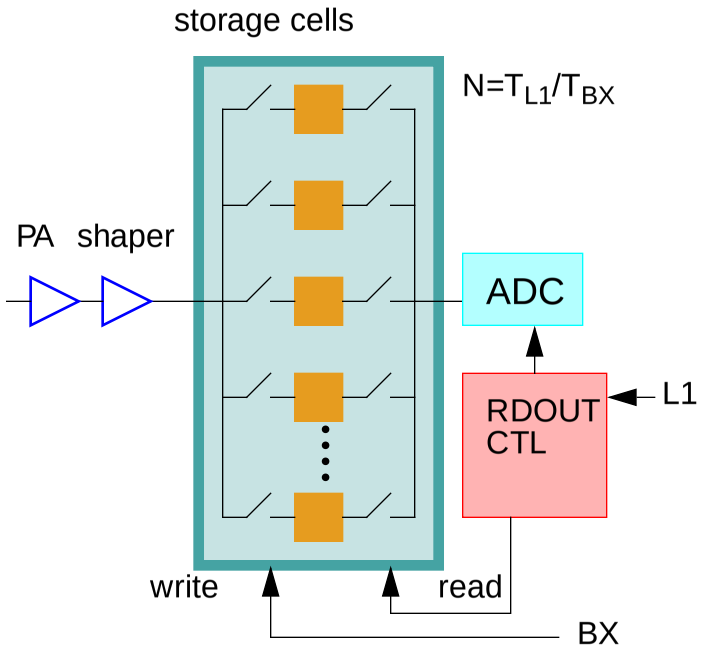
Data-Driven Sampling



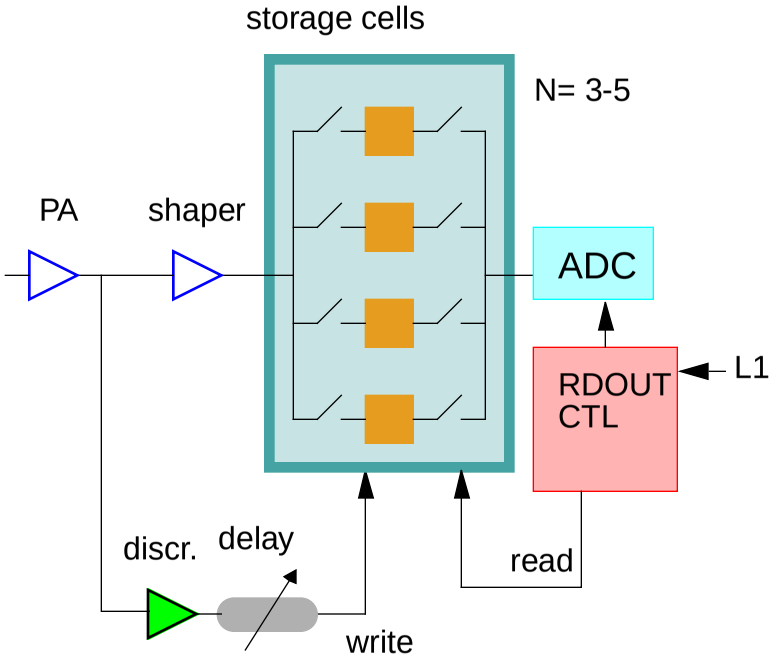
- only one sample per strip is written and read
- exactly at the peak
- strip is dead until after L1 latency + readout time
- discr. outputs required; can also be used to form local track segments for readout sparsification

Sampling Architectures

Clock-Driven Sampling

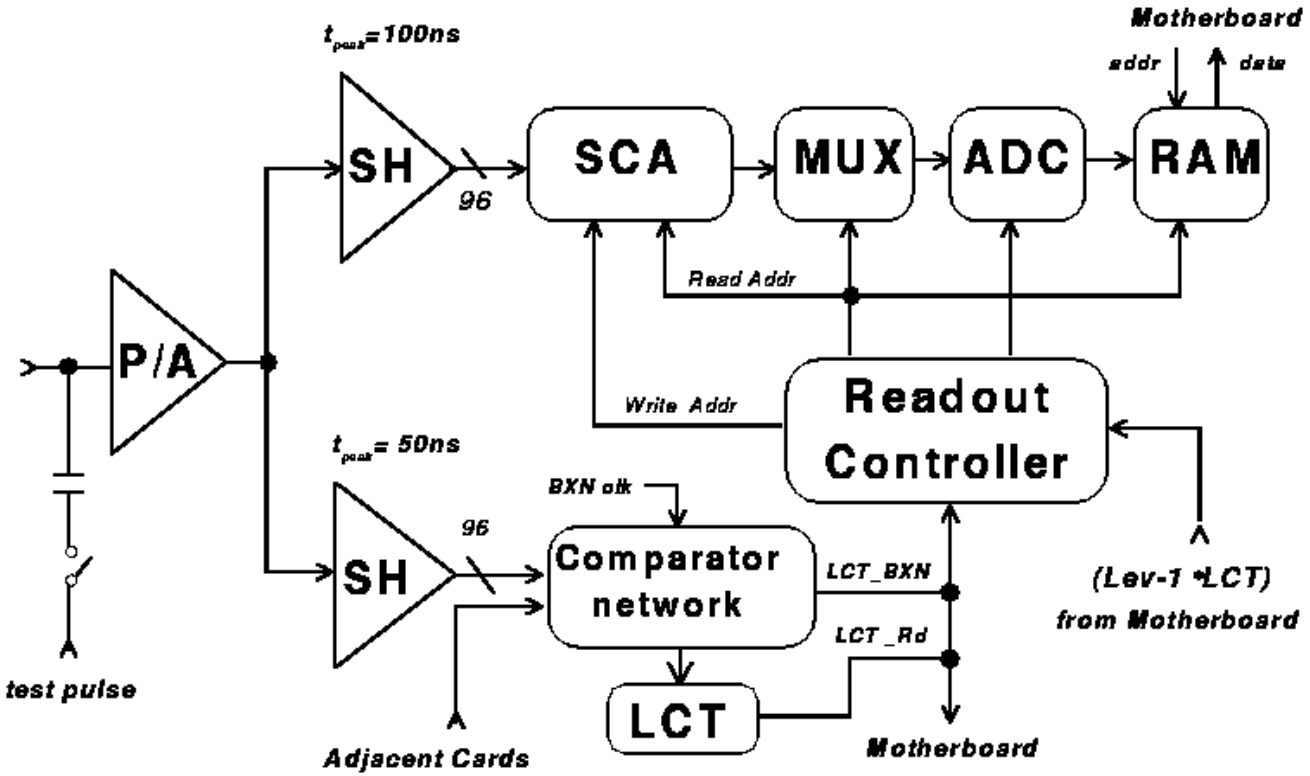


Data-Driven Sampling

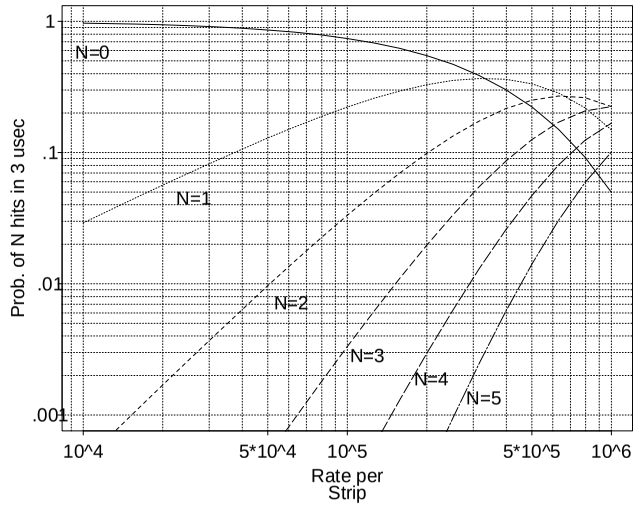


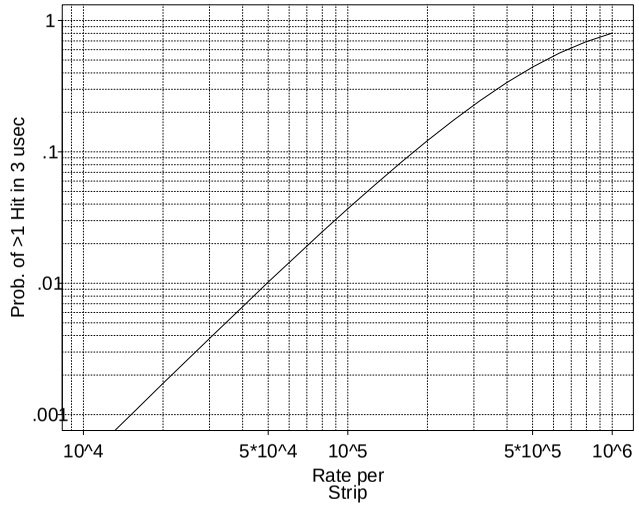
Sampling Architectures

CMS Clock-Driven Sampling Architecture



Adopting GEM Design to ATLAS





Rates in ATLAS are 10-100 times higher than at SSC =>

1. The shaping time has to be shortened
2. The inefficiency of the data-driven architecture with a single storage location has to be considered.

SHAPING TIME: to avoid pileup $T_s < (1/20)x(1/rate)$

For SSC: $T_s \sim$ **700 nsec**
For ATLAS: $T_s \sim$ **100 nsec**

Shorter shaping time causes degradation in S/N:

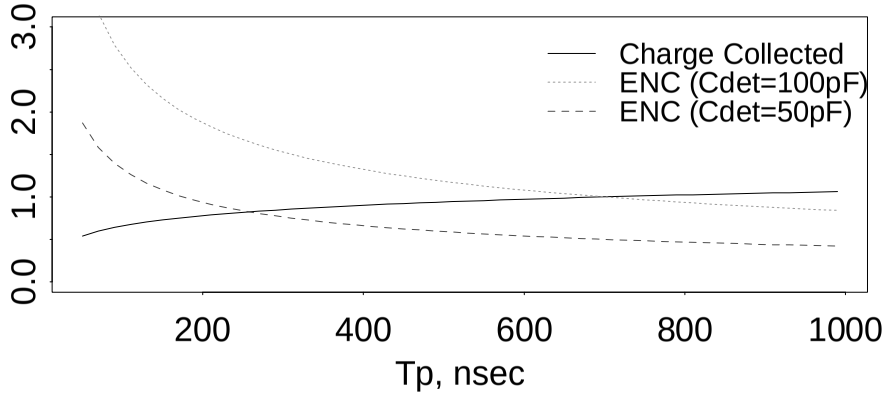
1. Signal is reduced by ballistic deficit:
   $Q_{coll} \sim \ln(1+T_s/t_0)$
2. Series ENC increases as
   $ENC \sim 1/\sqrt{T_s}$

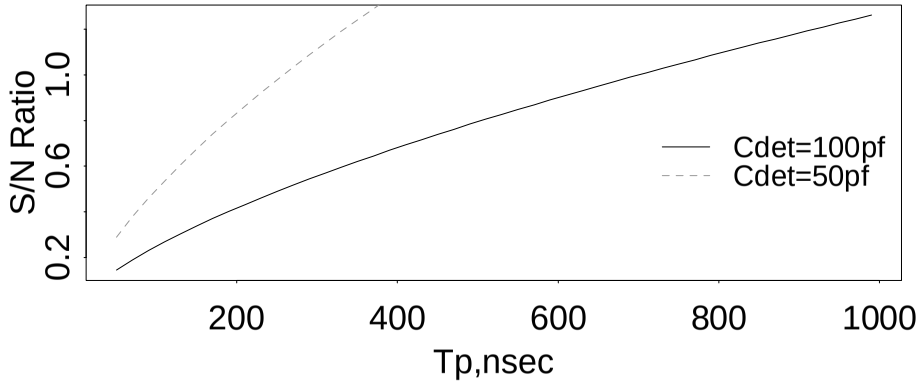
INEFFICIENCY: for strip rates > ~ 50 kHz, probability of more than one hit per L1 latency is significant.

Two solutions:

1. Clock-driven sampling with SCA
2. Data-driven but with multiple storage locations

Effect of Shaping Time on S/N Ratio





Data Rate

Flux	1.5 kHz/cm^2
Strip Area	.5 x 50 = 25 cm^2
Strips/hit	5
Samples/strip	10
Bits/sample	20
Precision channels/chamber	768
L1 Rate	10 kHz
Beam Crossing Rate	40 MHz

Data rate per chamber = $1.5 \times 10^3 \times 25 \times 5 \times 10 \times 20 \times 768 \times 10^5 / 40 \times 10^6$ = 72 Mbits/sec

No. Chambers per endcap: 32

Data rate per endcap = $72 \times 10^6 \times 32$ = 2.3 Gbits/sec

References

1. G. Bencze et. al., “Position and Timing Resolution of interpolating cathode strip chambers in a test beam”, NIM A 357 (1995) 40-54
2. V. Gratchev et. al., “Double Track Resolution of Cathode Strip Chambers”, submitted to NIM
3. E. Beauville, et. al., “AMPLEX - “, Nucl. Instr. and Meth. A 288 (1990) 157
4. P. O’Connor, “Low-Noise CMOS Signal Processing IC for Interpolating Cathode Strip Chambers”, IEEE Trans. Nucl. Sci., 42(4), Aug. 1995, 824-829
5. P. O’Connor, “Monolithic Front-End IC’s for Interpolating Cathode Pad and Strip Chambers for GEM”, Proc. Third Int’l. Conf. on Electronics for Future Colliders, Chestnut Ridge, NY May 1993, 167-178
6. T. Ferguson, et. al., “Front-End Electronics for CMS Endcap Muon Chambers”, Design Document Version 2.0, July 1996