CMOS preamplifiers for multi-channel detectors

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1. Charge-Sensitive Amplifiers in Scaled CMOS

2. Charge Amplifiers Optimized for High Resolution

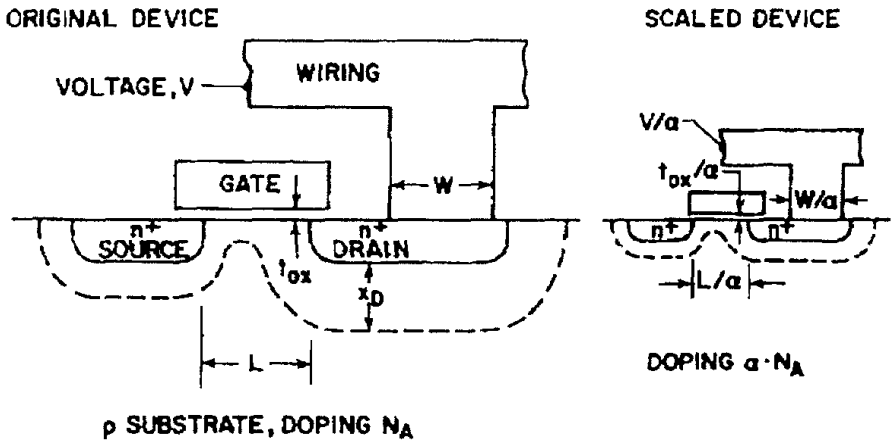
3. Efficient Architecture for Multichannel Readout

CMOS Scaling

Driven by digital VLSI circuit needs

Goals: in each generation

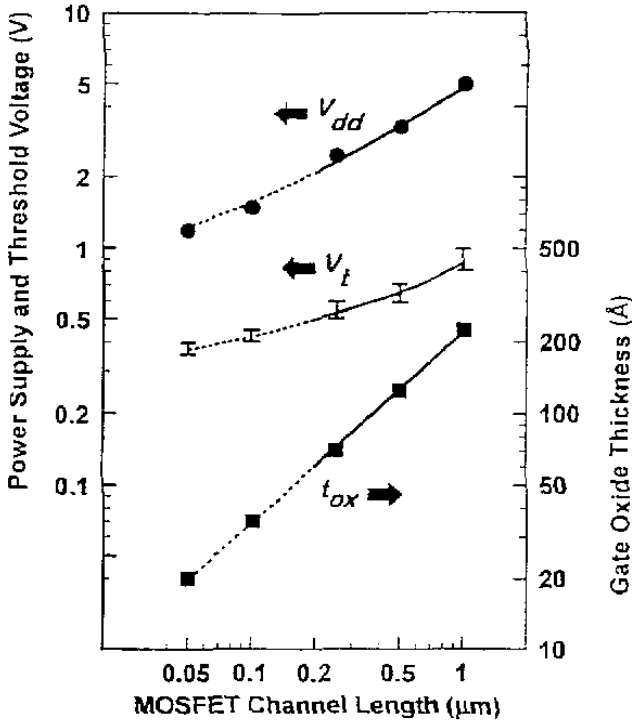
- 2X increase in density
- 1.5X increase in speed
- Control short-channel effects, threshold fluctuations
- < 1 failure in 10^7 chip-hours



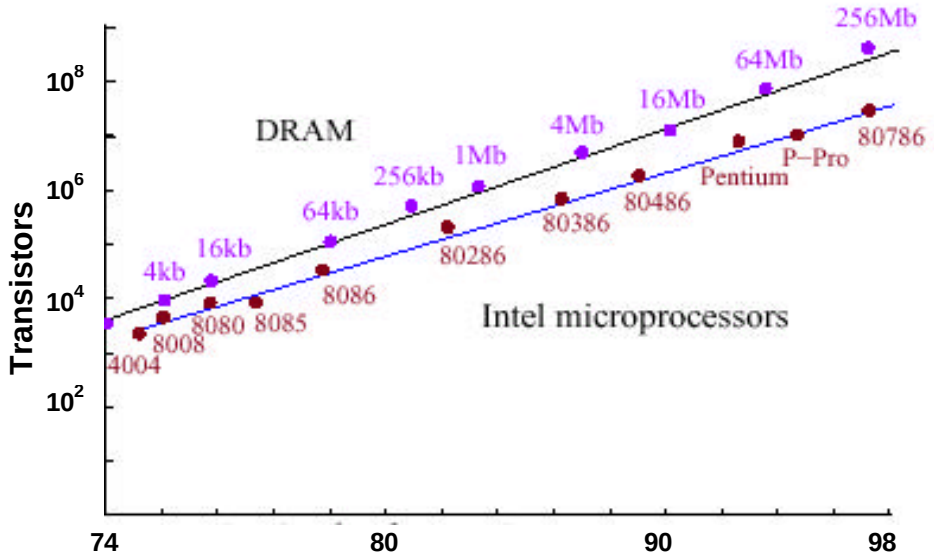
Rules:

- all dimensions scaled by factor λ
- electric field kept constant by reducing voltages
- doping density increased

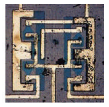
Technology Roadmap



Year	1997	1999	2001	2003	2006	2009
Feature size (μm)	0.25	0.18	0.15	0.13	0.10	0.07
Supply (V)	2.5	1.8	1.6	1.5	1.2	0.9
Tox (nm)	5.0	4.0	3.3	2.8	2.2	2.0
Vth (mV)	500	470	440	420	400	370
Nsub (10^{16}/cm^3)	3.4	5	6	7	10	20
Xj (μm)	0.1	0.07	0.05	< .05	<.05	<.05
10^6FETs/cm^2	8	14	16	24	40	64
Interconnect (meters/chip)	820	1500	2200	2800	5100	10000

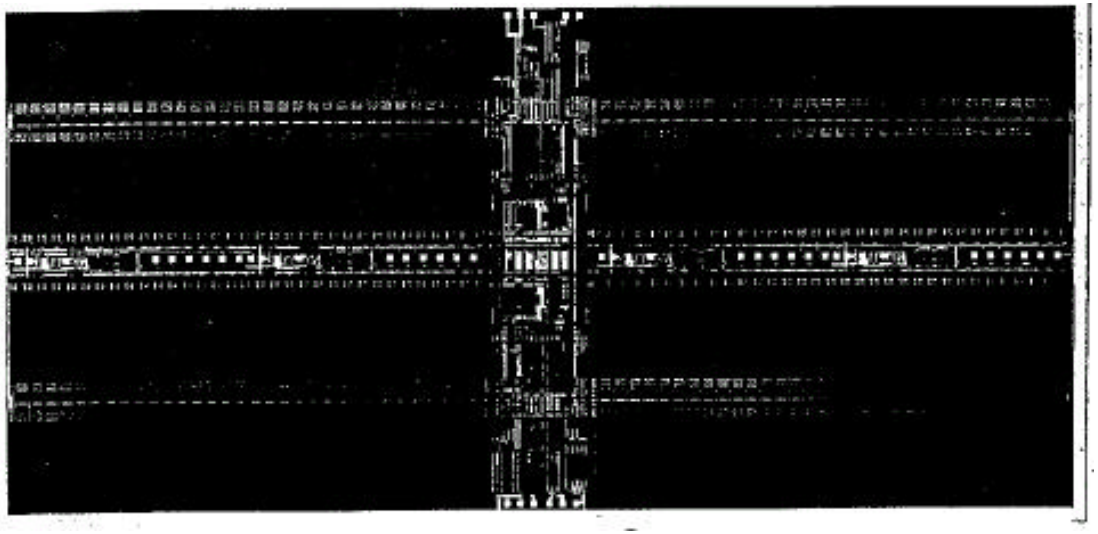


Memory Scaling



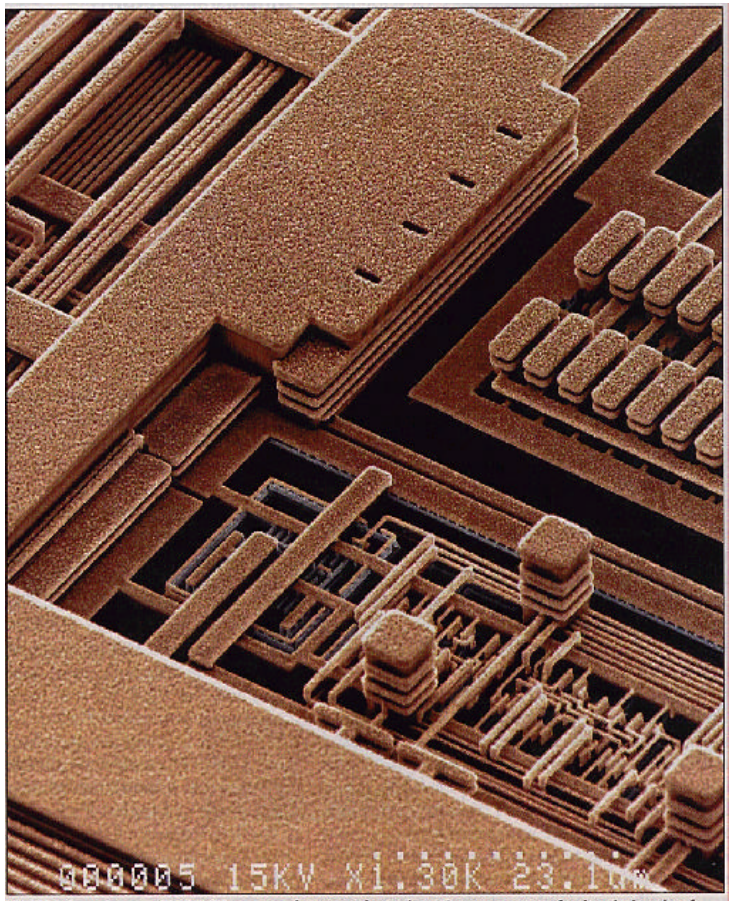
2b
2.3 mm^2
1960s

64 kb
26 mm^2
1980sh

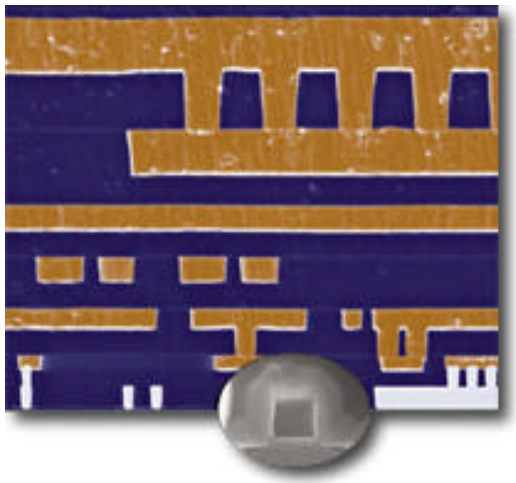


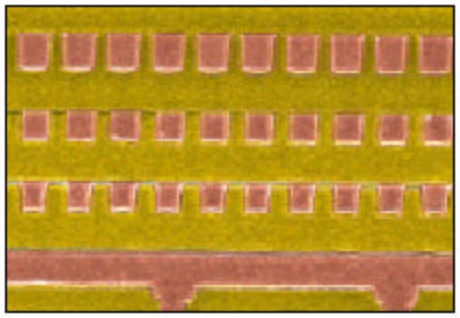
64 Mb
198 mm^2
1990s

IBM Cu-11 Process (Blue Logic)



[1] IBM Corp.'s new CMOS 7S process for manufacturing ICs uses copper for its six levels of interconnections, and has effective transistor channel-lengths of only 0.12 µm. It is the first commercial fabrication process to use copper wires [see "The Damascus connection," p. 25].





Section showing Cu-11 copper and low-k dielectric process.

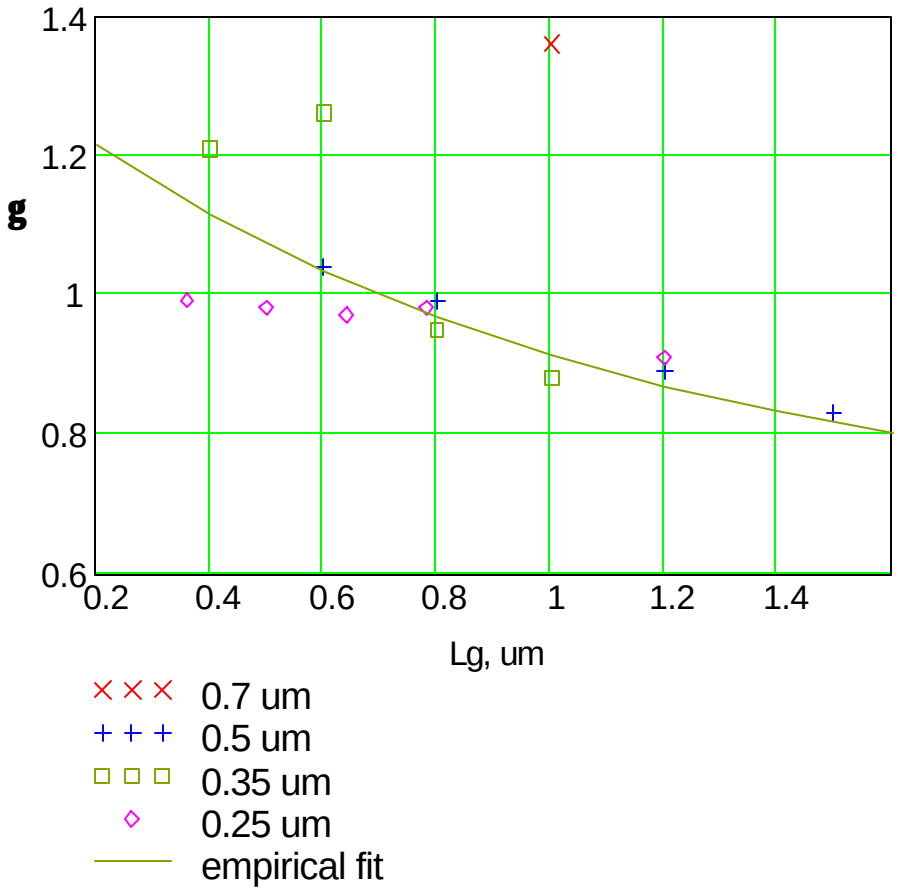
- L_{eff} =0.08 µm, L_{drawn} =0.11 µm
- Up to 40 million wireable gates
- Trench capacitor embedded DRAM with up to 16 Mb per macro
- Dense high-performance,comp lable SRAMs
- Power supply:1.2 V with 1.5 V opt on
- I/O power supply:3.3 V(dual oxide option)/
- 2.5 V(dual oxide option)/1.8 V/1.5 V
- Power dissipation of 0.009 µW/MHz/gate
- Gate delays of 27 picoseconds (2-input NAND gate)
- Seven levels of copper for global routing
- Low-k dielectric for high performance and reduced power and noise
- HyperBGA (flip chip):2577 total leads

White series noise

- **Parameter $\gamma = g_m * R_n$**
- **Long channel** g = 1 linear; 1/2 weak inversion; 2/3 strong inversion
- **Short channel γ: difficult to model**
- **High γ (γ = 2 – 4) reported in experimental submicron NMOS devices**
- **Strong increase in γ at high V_{DS}, high I_D/W**
- **Recent results on submicron CMOS at low V_{DS}, I_D/W:**

  $0.8 < \gamma < 1.35$

- **Shallow junctions increase S/D series resistance => noise**



ENC scaling -- white series noise

strong-inversion square-law:

L' -> λ L
VDD' -> λ VDD

$$ENC^2 = x \cdot kTC_{\det} \cdot \frac{1}{t_m} \cdot L\sqrt{\frac{C_{\det} V_{DD}}{mP}}$$

ENC_{min}' -> $\lambda^{3/4}$ ENC_{min}

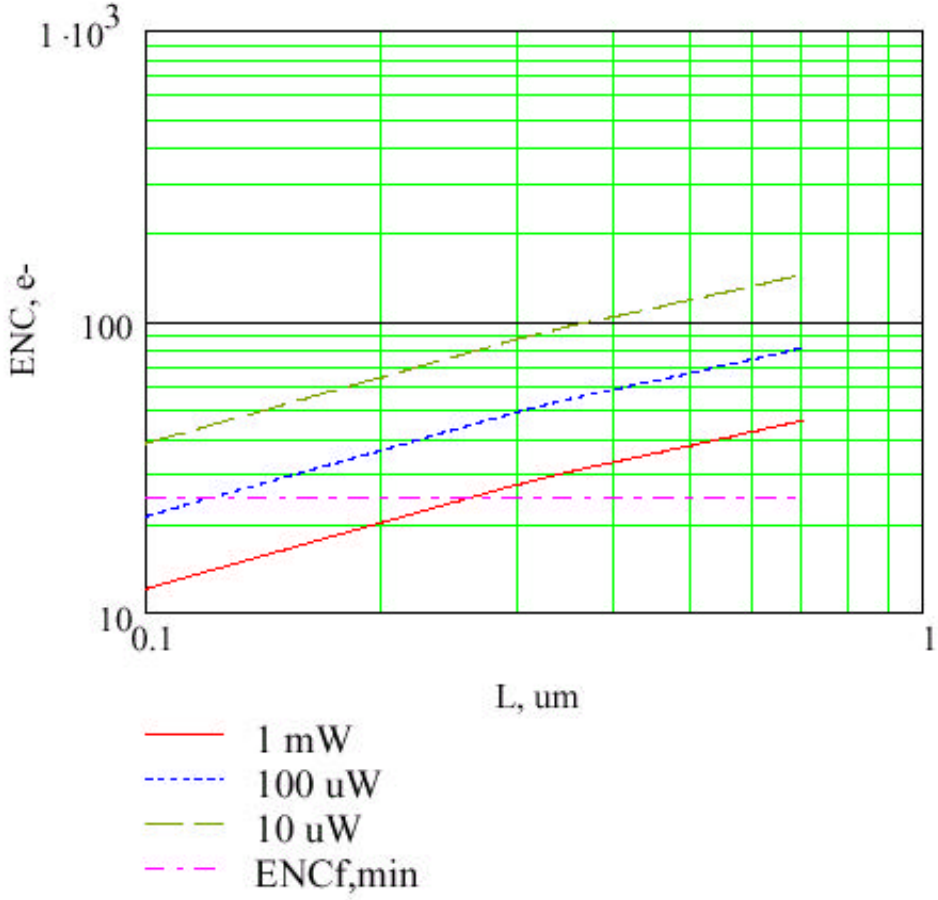
23% improvement in ENC per generation

velocity-saturated:

$$ENC^2 = x' \cdot kTC_{\det} \cdot \frac{1}{t_m} \cdot \frac{L}{v_{sat}}$$

ENC_{min}' -> $\lambda^{1/2}$ ENC_{min}

16% improvement in ENC per generation



Conditions: Cdet = 2 pF, tm = 500 ns

Power scaling

Power required to achieve a given ENC

1. FET in strong-inversion square-law:

$$P = x^2 \cdot \frac{(kT)^2 C_{\text{det}}^3}{t_m^2} \cdot \frac{L^2 V_{DD}}{m \cdot ENC^4}$$

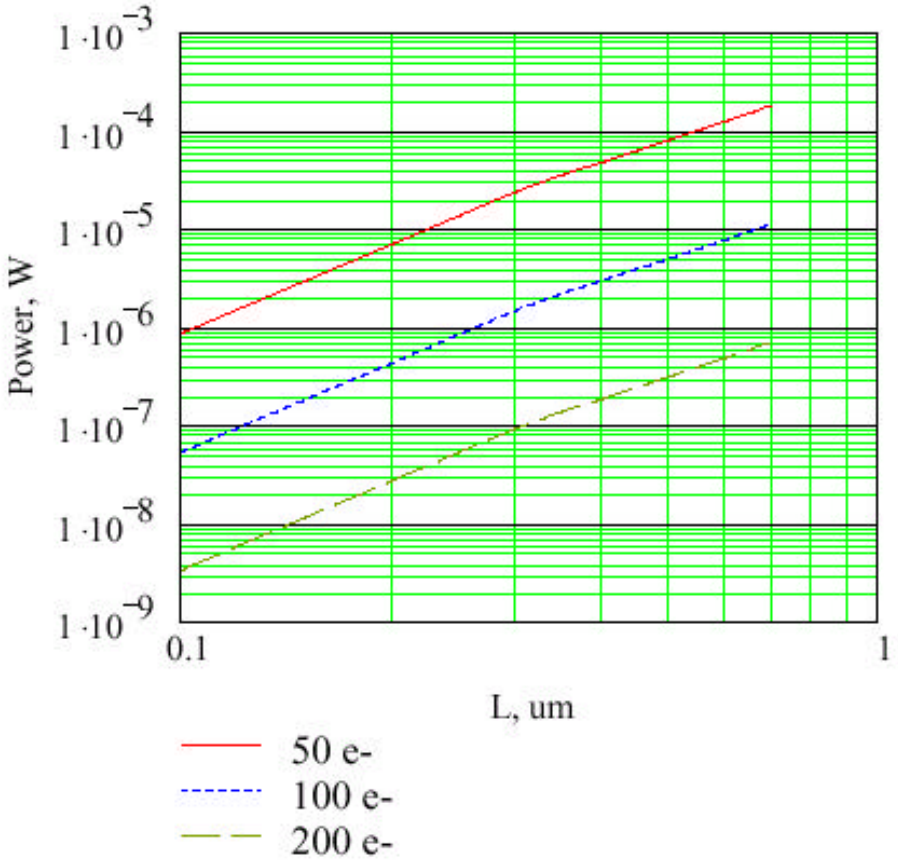
:

P' -> λ^3 P

66% decrease/generation

2. FET in velocity saturation:

Independent of l



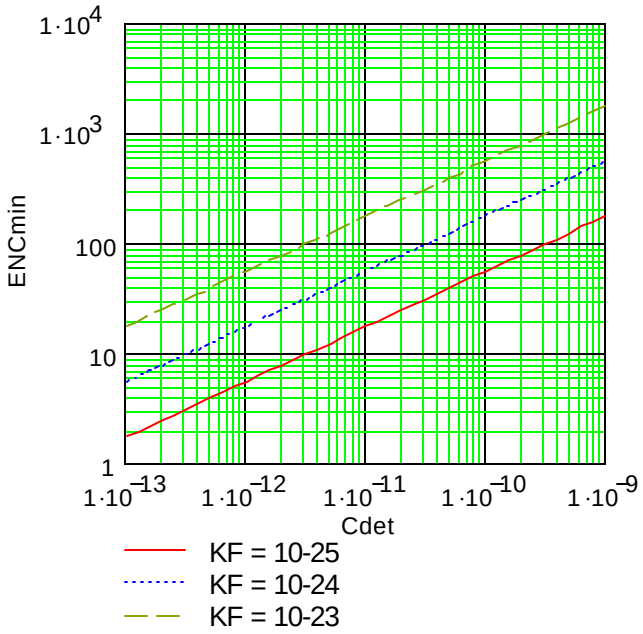
Conditions: C_{det} = 2 pF, t_m = 500 ns

1/f noise

1. **1/f sets the min. achievable ENC for the technology:**

$$\mathrm{ENC}_{\mathrm{f,min}} = 2\sqrt{a_2 K_F C_{\mathrm{det}}}$$

$$\text{where } e^2_{\mathrm{n,f}} = \frac{K_F}{C_{ox} W L f}$$



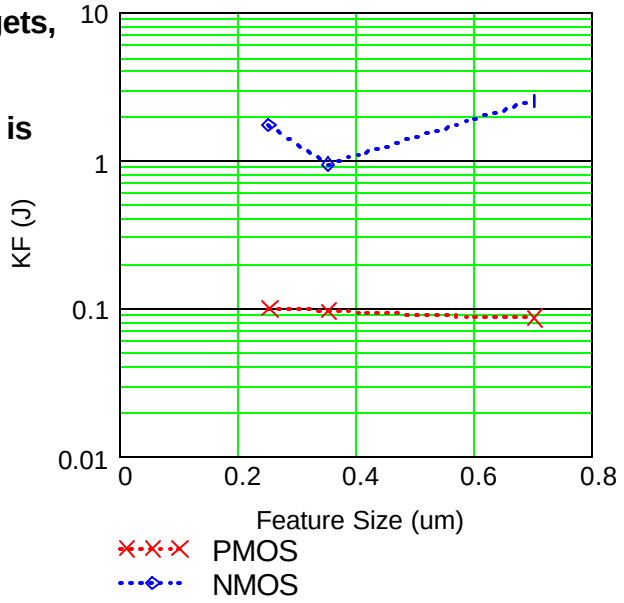
Minimum ENC vs. detector capacitance

2. **Technology generations below 0.25 mm with n+/p+ poly gates will have high PMOS 1/f noise (surface channel device).**

3. **Advanced processes require ultrathin gate dielectrics and low thermal budgets, resulting in oxides with higher trap densities.**

4. **Hot-carrier stress generates new oxide/interface traps. Low frequency noise is much more sensitive to HC stress than static parameters:**

   - **Dgm -10%**
   - **D(1/f) +400%**



Measured 1/f noise coefficient for several submicron CMOS processes

Beyond scaled CMOS

1. CMOS scaling can be expected to continue until the 0.07μm - 1.5 nm - 1V (Lg - tox - Vdd) generation.
2. Further scaling will not improve the transistor properties for digital applications:

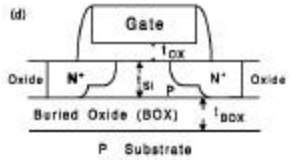
   gate current > 1 A/cm^2

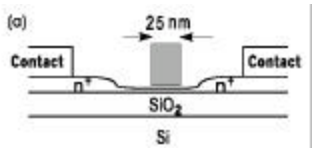
   S/D junction resistance too high

   no increase in current drive with further scaling

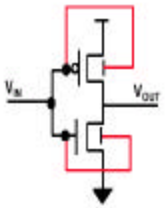
3. Modifications to the basic bulk MOSFET:

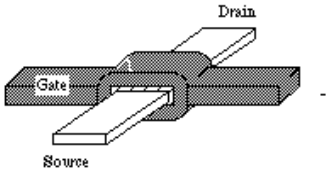
   SOI devices





   Top- and bottom-gated device





   Si_x-Ge_{1-x} channels

   High - ε gate dielectric

4. Nanoscale devices

Charge Amplifiers Optimized for High Resolution

0.5 µm CMOS, 3V supply

C_{det} ~ 1 - 4 pF, I_{leak} ~ 1 - 100 nA, t_m ~ 200 - 4000 nsec, gain ~ 30 - 200 mV/fC

Continuous reset implemented by compensated nonlinear pole-zero cancellation

- *adapts to wide range of leakage current*
- *no change of pulse shape*
- *stable to process/temperature/supply variation*
- *minimum parallel noise*
- *no adjustment by user*

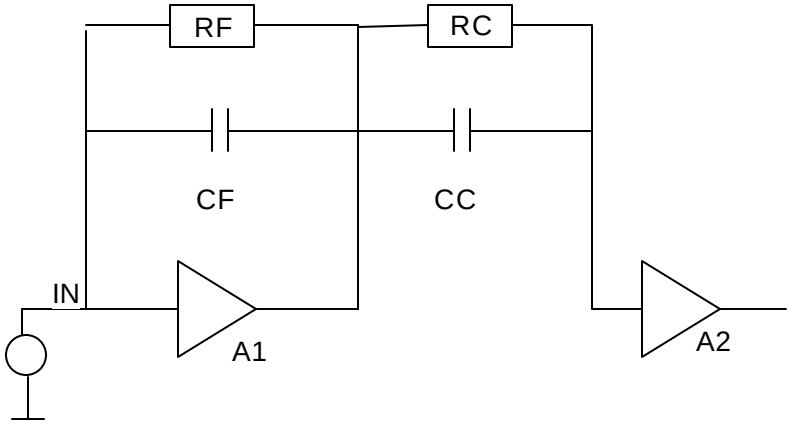
High-order shaping with complex poles, active-RC sections

Adjustable peaking time and gain; both bipolar and unipolar shaping

Rail-to-rail Class AB output stages

4 - 16 amplifiers/chip

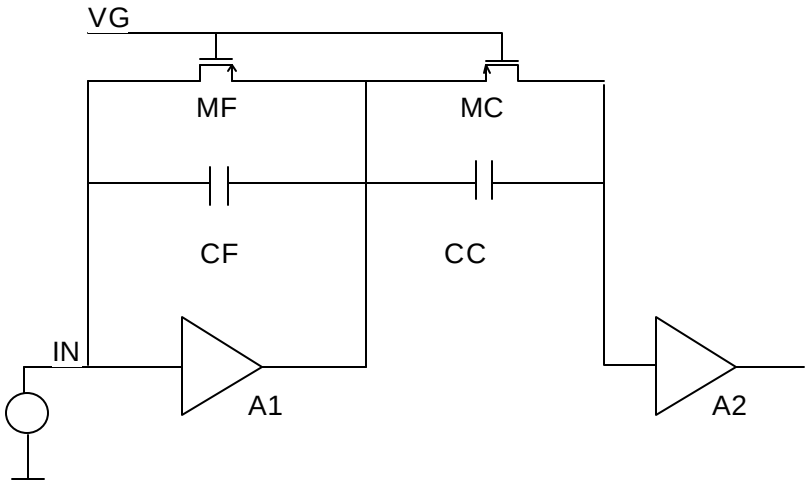
Nonlinear Pole-Zero Compensation



Classical

$RF \cdot CF = RC \cdot CC$

Zero created by RC,CC cancels pole formed by RF, CF



IC version

$CC = N \cdot CF$

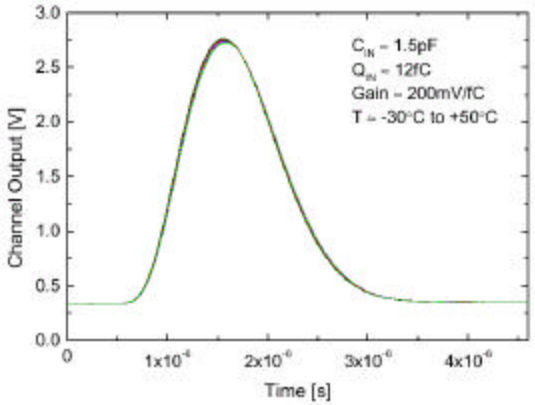
$(W/L)_{MC} = N \cdot (W/L)_{MF}$

Zero created by MC, CC cancels pole formed by MF, CF

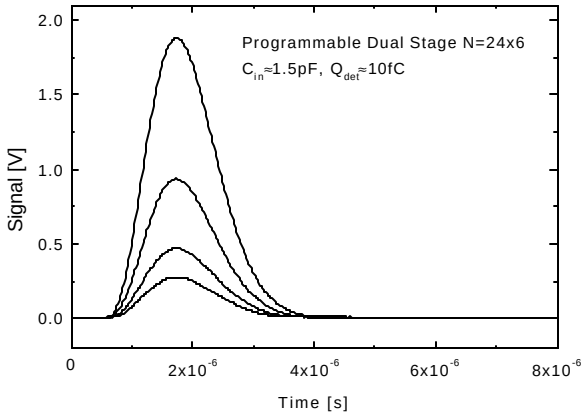
Rely on good matching characteristics of CMOS FETs and capacitors

Amplifier performance

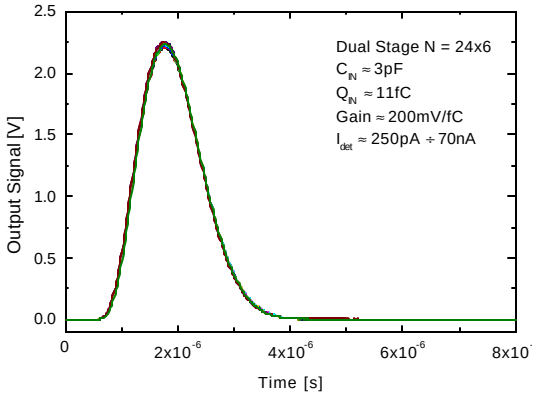
Pulse vs. Temperature



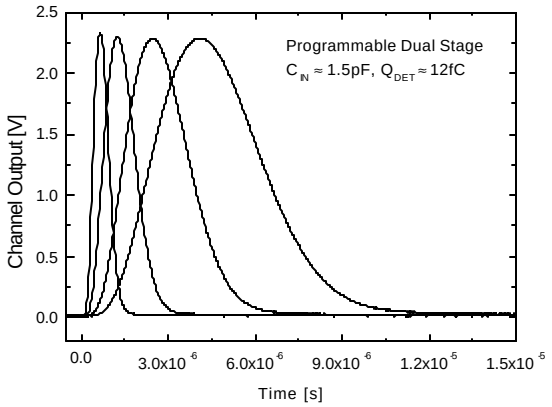
Gain variation



Pulse vs. I_{leak}



Peaking time variation



Measured amplifier performance

ENC	26 + 27 e-/pF
Linearity error	< 0.3% full scale
Cross Talk (packaged)	< 0.5% (<0.1% non-adjacent)
Baseline dispersion	2 mV rms
Power dissipation	18 mW/chan.

Stability improvements for practical use

	I_{leak}	Supply	Temperature	Rate (to 5/tp)	Cin	Zload
Gain	< 0.1%/nA	<.001%/V	-0.04%/°C	< 0.1%	<0.1%/pF	No slew-rate limit
Baseline	< 0.3mV/nA	<30 μV/V	75 μV/°C	< 8 mV	-	Zout ~ 150 Ω

^{241}Am Spectrum