
A Generation of Readout ASICs for CZT Detectors

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The BNL-eV Cooperation

CZT readout : discrete or ASIC ?

Cost

- multi-chip project \approx \$35/ch (compare \approx \$75/ch)
- large numbers \approx \$1/ch
- R&D : C.R.A.D.A.

Manufacture

- time savings
- board simplification
- reduced number of process steps

Reliability

- reduced external interconnects
- lower exposure

Size

- \approx 1 mm²/ch (compare \approx 700 mm²/ch)
- opening to new applications

Power

- \approx 10 mW/ch (compare \approx 300 mW/ch)
- reduced detector temperature
- opening to battery operation

Performance

- reduced parasitics
- high order shaping
- additional processing

The BNL-eV Cooperation
CZT readout : discrete or ASIC ?

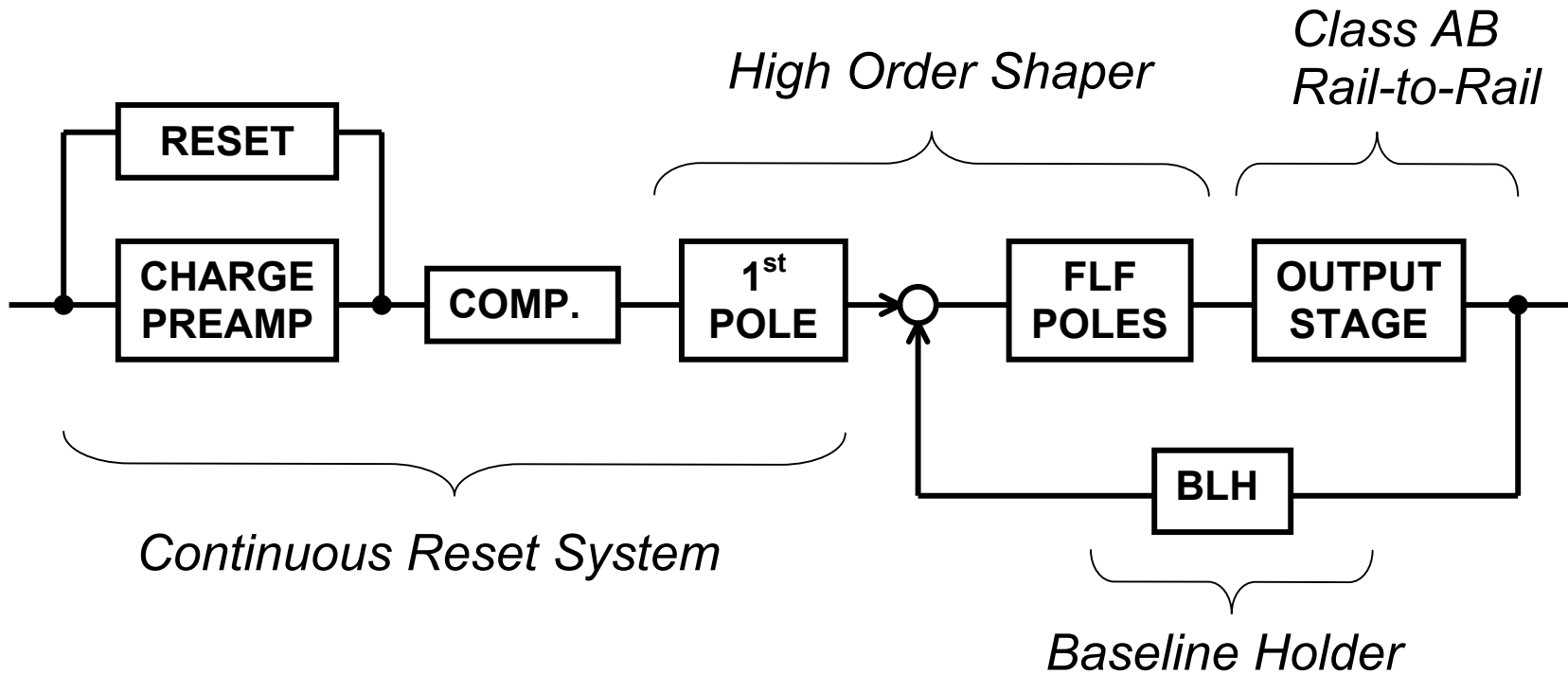
ASIC's key requirements

- low noise
 - high linearity
 - programmability
 - low power
-
- low noise dc coupling
 - high order shaping
 - high driving capability
 - high baseline stability

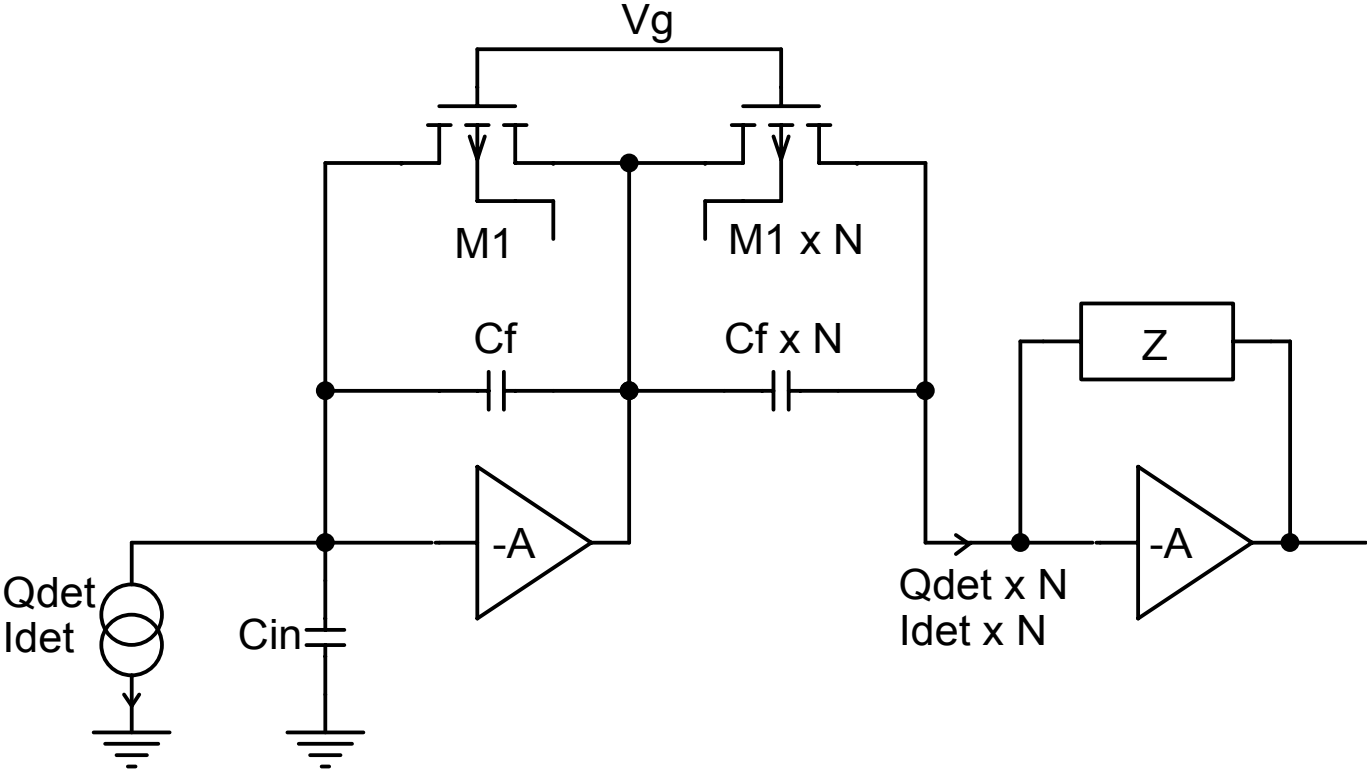


A generation of ASICs

Channel Simplified Schematic

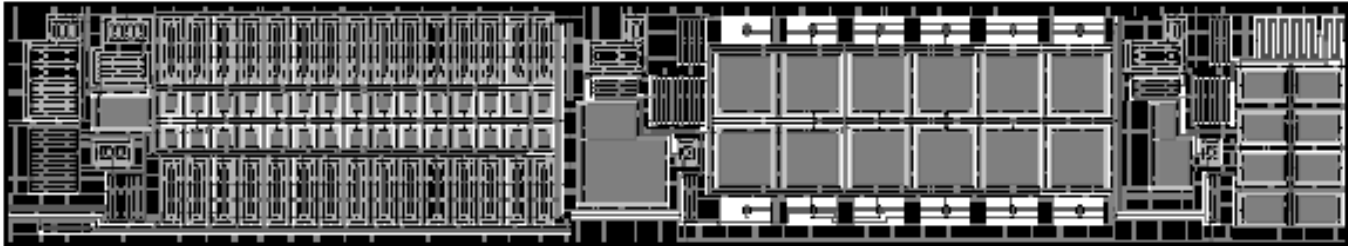


Reset System

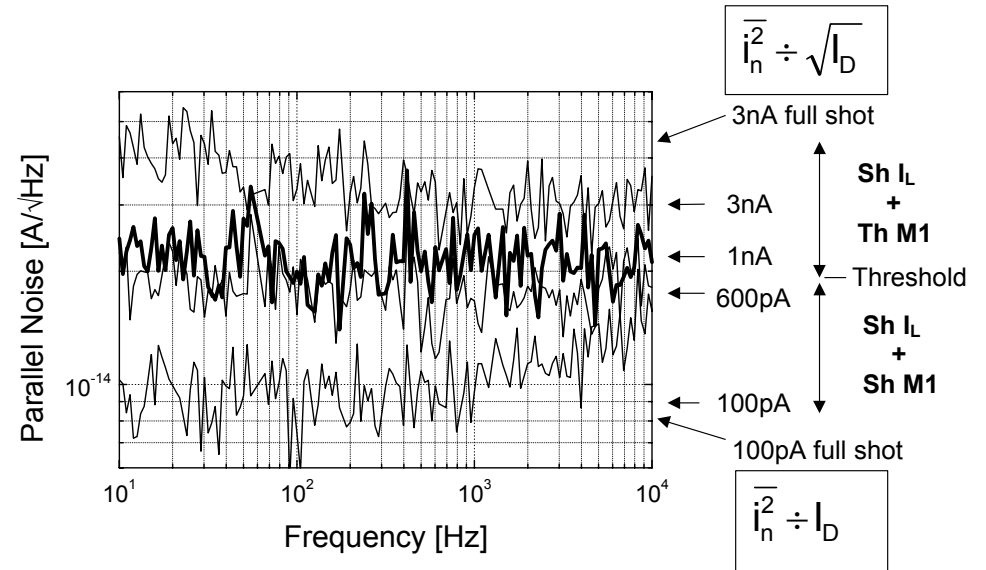
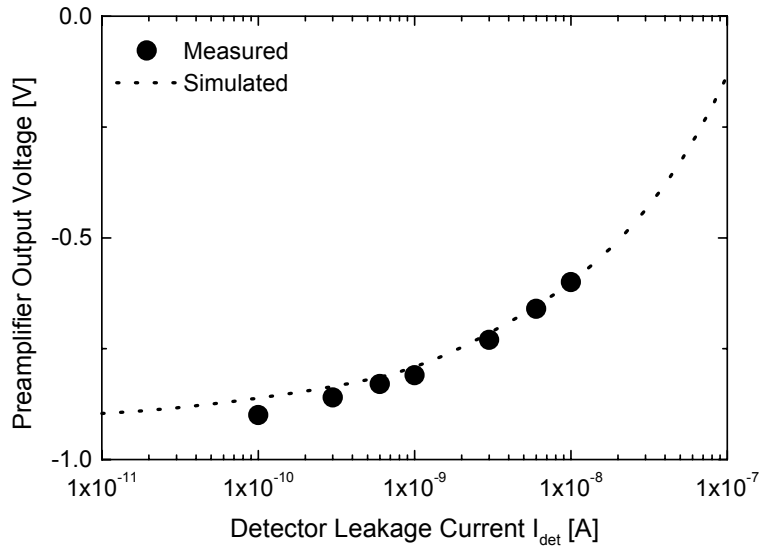
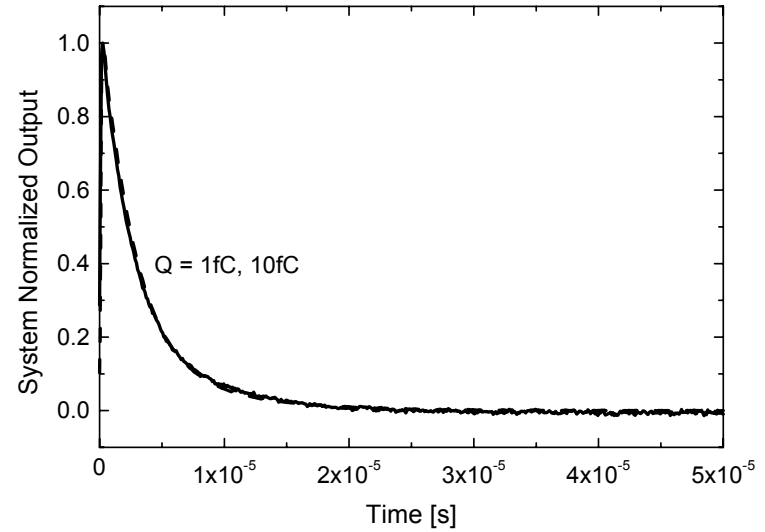
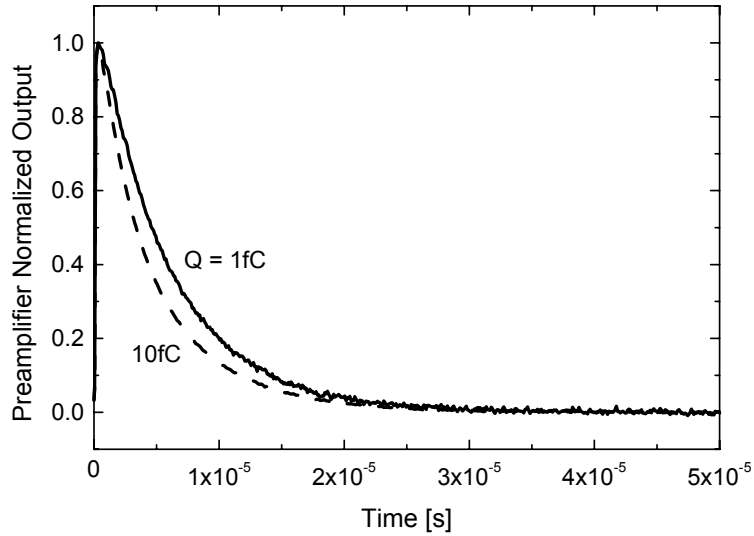


$$N_1 = 24$$

$$N_2 = 6$$

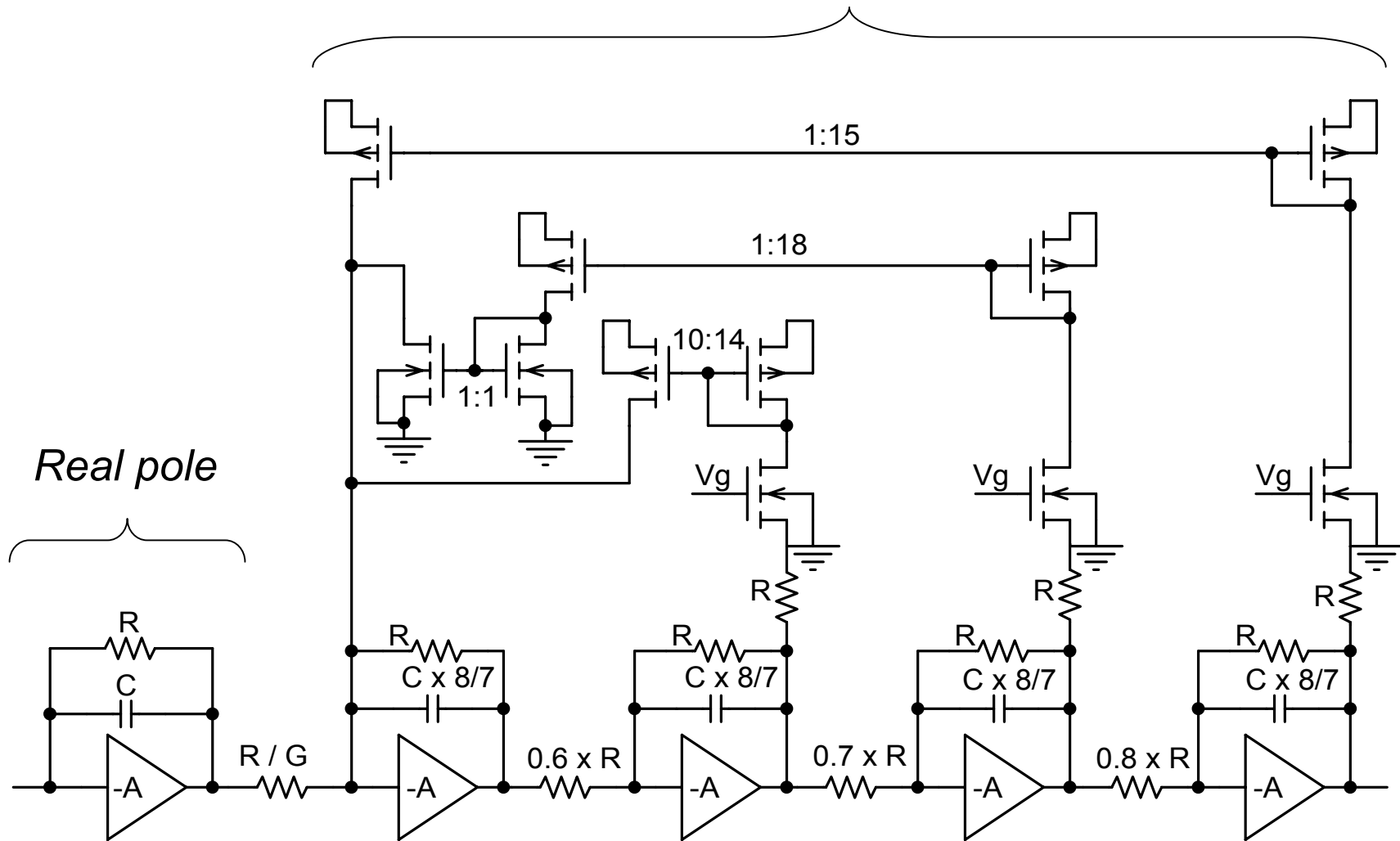


Reset System: Experimental Results

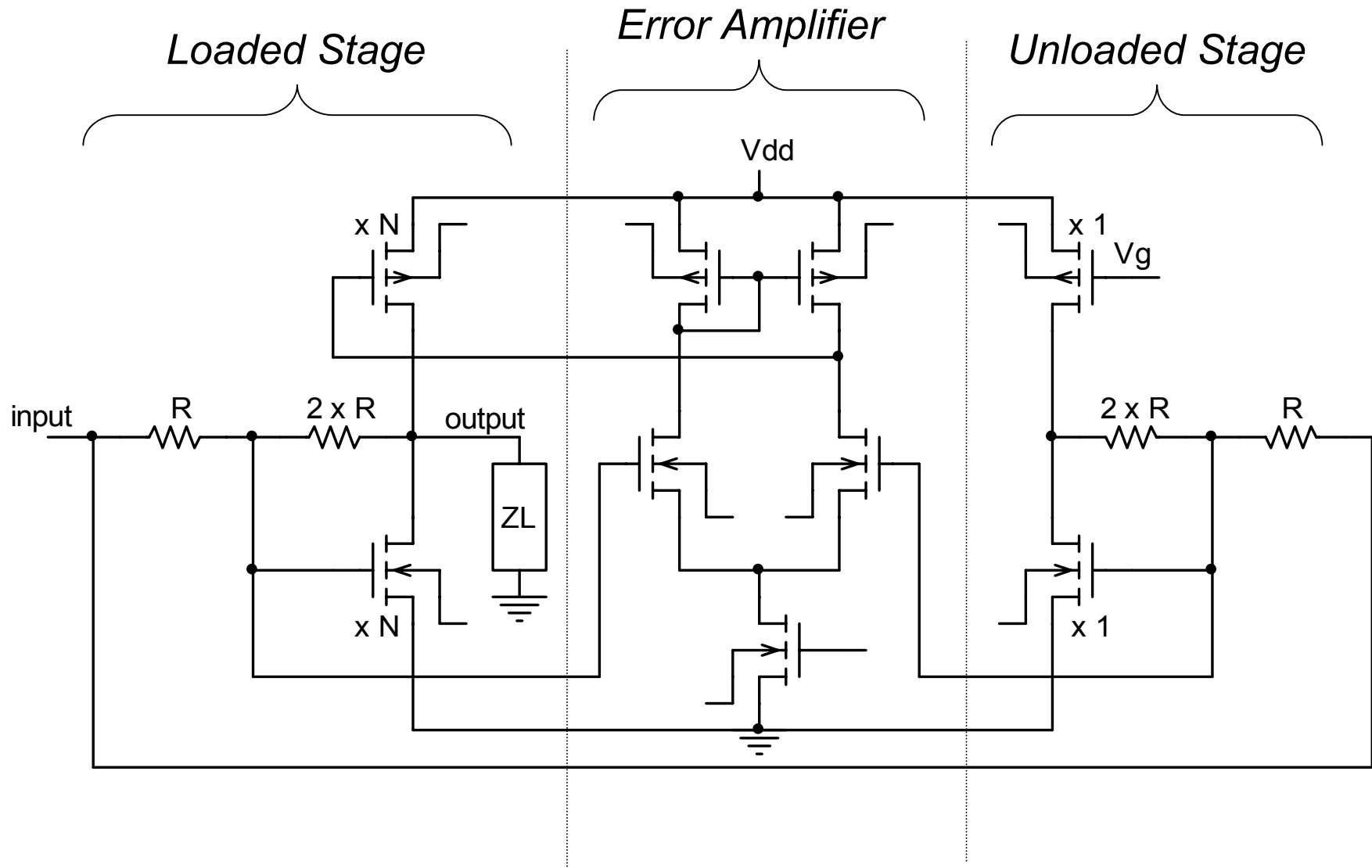


Shaper Amplifier: 5th order complex semigaussian

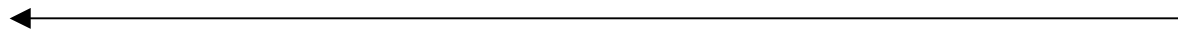
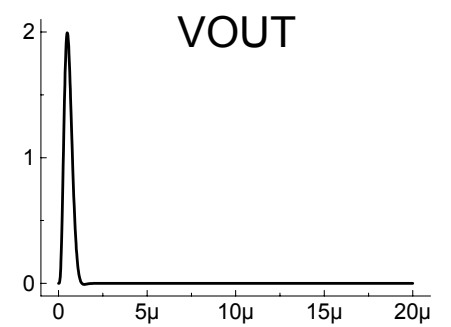
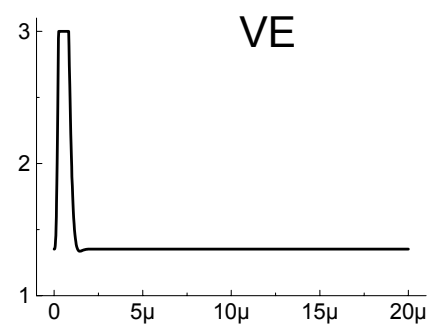
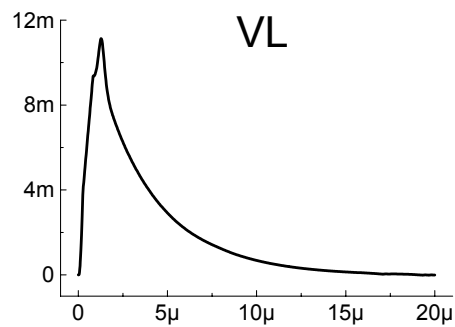
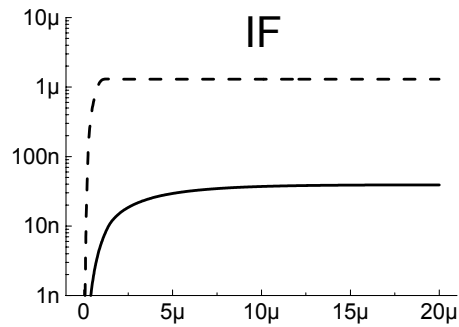
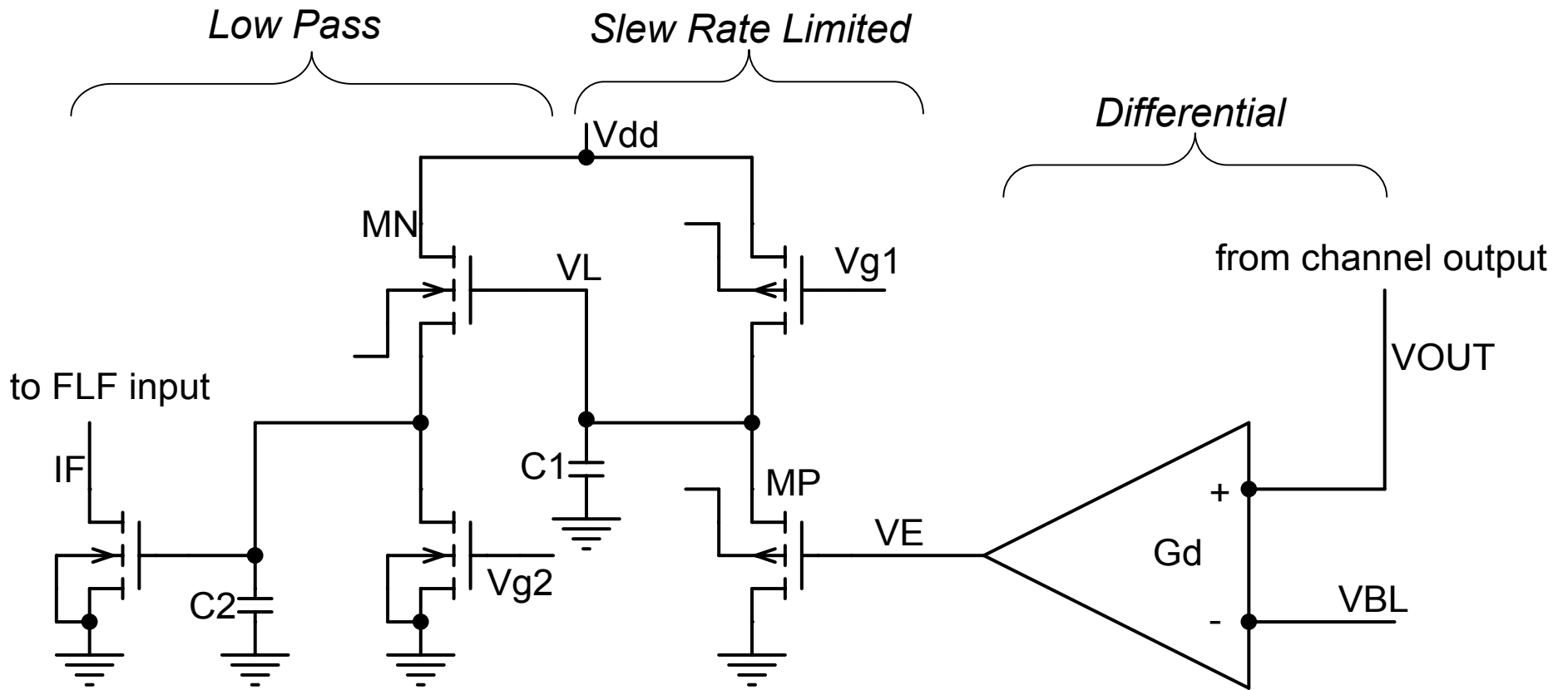
FLF 4 complex conjugate poles



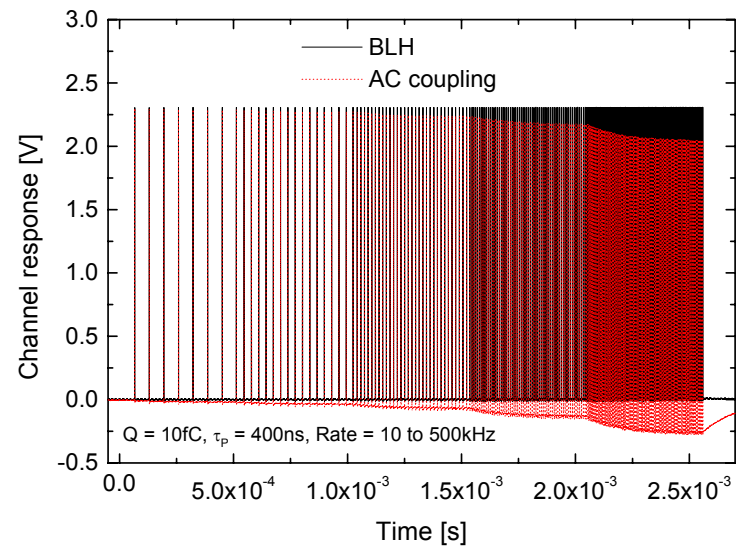
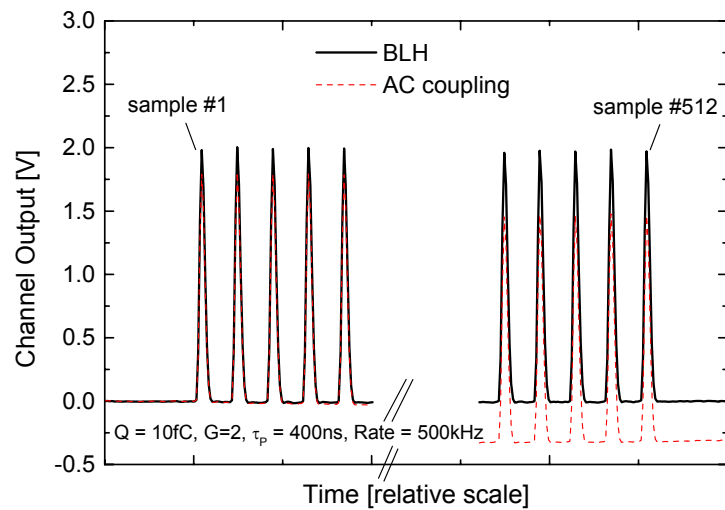
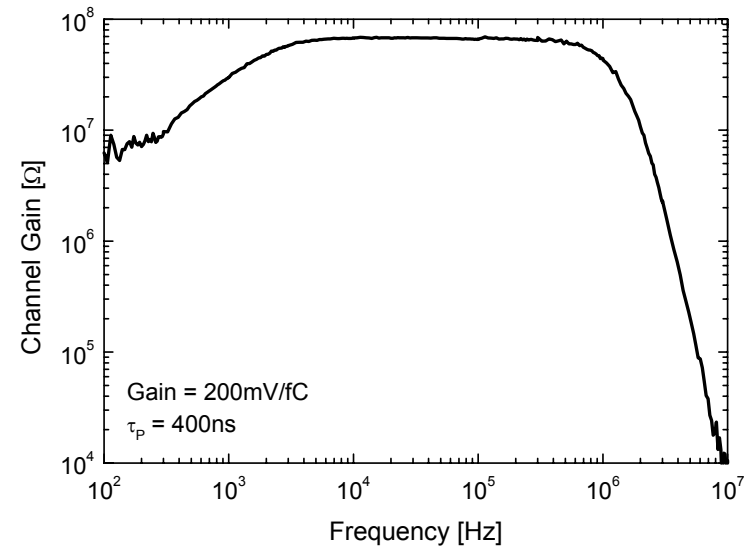
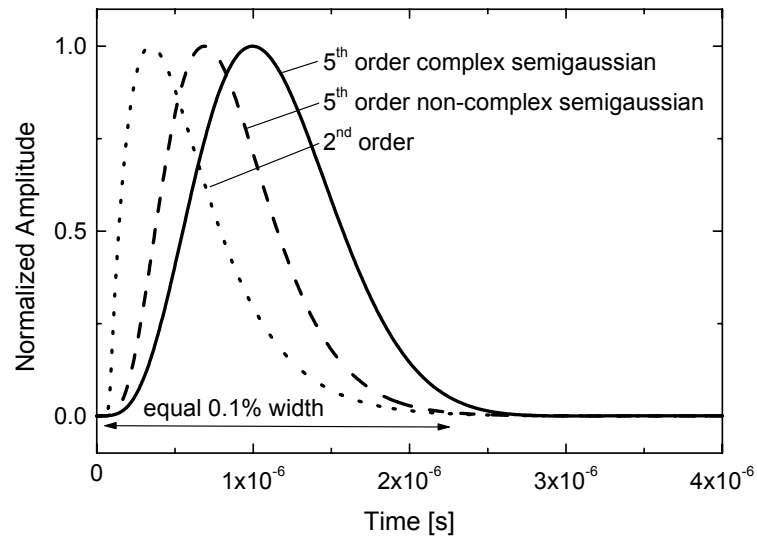
Output Stage



BLH (Baseline Holder)



SHAPER / BLH (Baseline Holder): Experimental Results



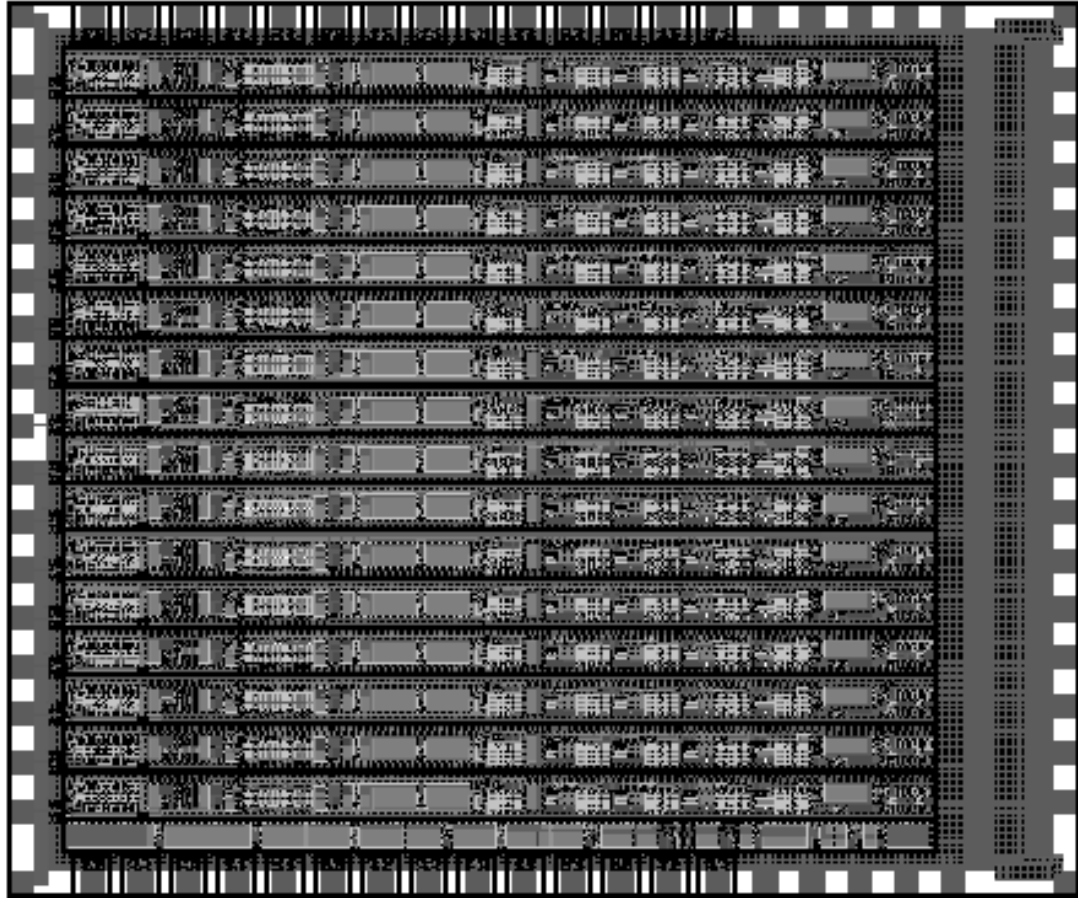
Prototypes

	<i>application</i>	<i>channels</i>	<i>shaping</i>	<i>gain [mV/fC]</i>	<i>pk time [μs]</i>
IC45	B,D,E	2	UNI	200	0.4
IC46	B,D,E	2	UNI	200	0.4
IC48	B	2	BIP	260	0.2
IC49	B,D,E	4	UNI	200	0.4
IC54	A	16	UNI	30-200	0.9 - 1.2
IC55	C	8	UNI	26-180	2.25 - 3.0
IC56	B	4	BIP	260	0.2
IC59	D,E	4	UNI	200	0.4
IC60	A	16	UNI	30-200	0.6 - 4.0

- A general purpose
- B bone densitometry
- C intra-operative probe
- D baggage scanning
- E down-hole logging

Typical

Size 5.1mm × 3.7mm
Ch.s 16



Gain	30mV/fC, 50mV/fC, 100mV/fC, 200mV/fC
Pk Time	0.6 μ s, 1.2 μ s, 2.4 μ s, 4.0 μ s
ENC² (@ 1.2 μ s, 200mV/fC)	$35^2 + 35^2/\text{pF}^2 + 55^2/\sqrt{\text{nA}} + 0.2\text{Q}/q$
Integral Linearity Error	< 0.3%
Cross Talk	< 0.4% (< 0.1% non adj.)
Power	$\approx 4\text{mW} + 18\text{mW}/\text{ch.}$
Baseline Adjustment	-100mV \div +400mV

Test With CdZnTe Detector

Conclusions and Future Work