Status of the CDF Silicon Detector [1]

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Abstract

The CDF Run II silicon micro-strip detector is an essential part of the heavy flavor tagging and forward tracking capabilities of the experiment. Since the commissioning period ended in 2002, about 85% of the 730 k readout channels have been consistently providing good data. A summary of the recent improvements in the DAQ system as well as experience of maintaining and operating such a large, complex detector are presented.

Key words: CDF, silicon micro-strip detector, high energy physics

1. Introduction

CDF is a collider experiment that is running at the Fermilab Tevatron. The core of the CDF II detector (1) is an 8 layer silicon micro-strip tracker. The design of the upgraded silicon system provides improved impact parameter resolution and increased acceptance in the forward regions. This translates into better tracking and heavy flavor tagging efficiencies. Of critical importance is also the system's ability to trigger on displaced tracks, enhancing the CDF II B-physics program.

The system is separated into three sub-detectors which share a common infrastructure; the five-layered SVX II for precision tracking and triggering, the innermost Layer 00 (L00) to improve impact parameter resolution, and two Intermediate Silicon Layers (ISL) located between SVX II and the main CDF II tracking chamber. All three detectors use the same custom made front end ASIC, the SVX3D chip (2), which features dead-timeless operation with separate acquisition and readout cycles. The digitization logic provides 8 bit resolution, dynamic pedestal subtraction and data sparsification which reduces the raw data size of each sub-detector into the DAQ system.

The SVX II is the heart of the silicon detector. Five layers of sensors are arranged at radii between 2.5 and 10.6 cm, covering 90 cm along the beam direction. The symmetric segmentation in ϕ permits the treatment of each of the 30° wedges independently. The Silicon Vertex Trigger (SVT), which identifies tracks with large impact parameter, is based on this symmetry, the tight alignment constraints, and the fast readout achieved by reading each wedge in parallel. SVX II uses double-sided sensors with axial strips at $\approx 60\mu$m pitch on one side (layer dependent), and either 90° strips

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(at $\approx 140\mu$m) or 1.2° small-angle stereo strips (at $\approx 60\mu$m) on the other, providing 3D information. The ISL consist of one central (at radius 20 cm) and two forward (at 18 and 29 cm) silicon layers between the SVX II and the tracking chambers, providing track linking between the two systems and extending the silicon tracking to high pseudo-rapidity ($\eta \leq 2$). The ISL use double sided small angle stereo (1.2°) strips, with a strip pitch of 112 μm on both sides. L00, the innermost silicon layer, is mounted directly on the beam-pipe at a radius of 1.4 cm. The sensors are radiation hard, single-sided and designed to withstand a high bias voltage ($\approx$ 500V) to allow extended running after type inversion. The strip pitch is 25μm but only alternate strips are read out, this improves spatial resolution without significant degradation in efficiency or two-hit separation. Fig. 1 shows a schematic view of the CDF II silicon system, the combined detectors have a total of 772,432 electronic channels and 6 m^2 of silicon, making it the largest silicon detector in operation.

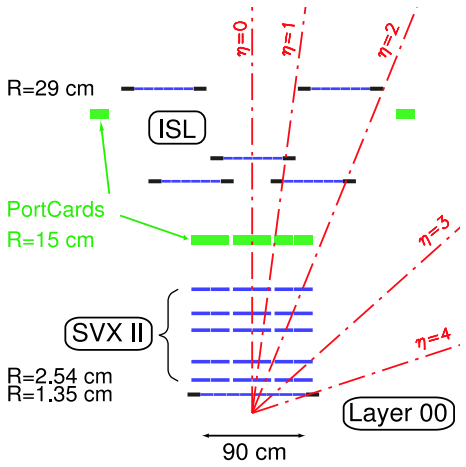

Fig. 1. Schematic view of the CDF II silicon detectors in the rz-projection, the z coordinate is highly compressed.

2. Commissioning

Two of the problems during the commissioning period are related to recent improvements in the silicon DAQ system: the pick up noise in the L00 readout and the breaking of wirebonds during anomalous trigger conditions. Soon after L00 became operational it was discovered that pick up noise was introduced due to the long leads connecting the sensors to the readout chips, which are located at larger radii to mitigate the effects of radiation (3). This prevented the use of the SVX3D dynamical pedestal subtraction as the pedestals were not uniform across a chip. In order to solve this problem all the channels are read out and software pedestal subtraction is performed offline.

Perhaps the most challenging of the commissioning problems were the wire-bond failures (4) which resulted in the permanent loss of the the z side of 12 SVX II ladders. The wirebonds, perpendicular to the 1.4 T magnetic field, carry power from the $r\phi$ to the z side SVX3D chips. The current consumption of the chips increases drastically when the readout cycle is initiated, hence, the Lorentz forces induced on the wires upon a synchronous trigger condition will cause the wires to oscillate and break due to mechanical fatigue. This failure mode was reproduced on the teststand on real (spare) ladders and using finite element analysis. Two measures were taken to avoid further wirebonds failures. The SVX3D chip settings were adjusted to reduce the current draw, and a new VME board which performs frequency analysis was introduced. The board computes the time interval between successive readout commands and halts data taking if a certain number of similarly spaced commands are detected. Since these measures have been implemented no further wire-bond failures have been found.

3. The Silicon Data Acquisition System

The DAQ system is shared between the three silicon sub-detectors: this simplifies operations and lower the costs. The DAQ is VME based, with 135 boards spread over 17 crates, half of which are in the collision hall. The command and data flow of the system is shown in Fig. 2.

The Silicon Readout Controller (SRC) is the brain of the DAQ system. The SRC receives the clock and trigger signals from the CDF Clock and

Trigger Supervisor (TS) and generates the commands to read out the silicon detector. Upon an event that satisfies the Level 1 trigger requirements, the TS issues a Level 1 accept signal (L1A) to the SRC. The SRC sends the readout commands to the SVX3D chips through the fiber interface boards (FIBs). The digitized data, after pedestal subtraction and sparsification, is sent back to the interface boards optically. From the FIBs the data is sent to the VME readout buffers (VRBs) and the SVT system. The readout chain is completed once all the data arrives to the VRBs.

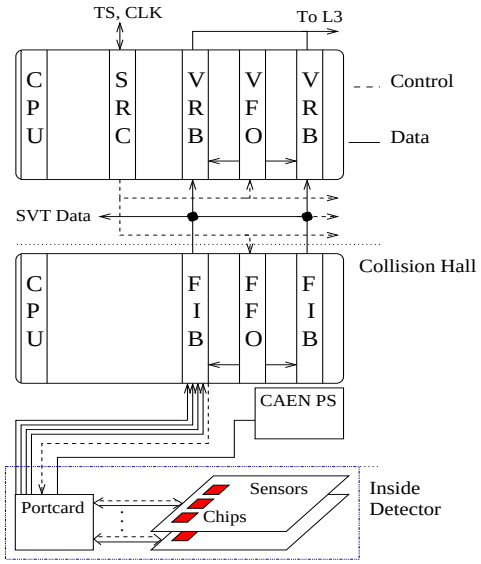

Fig. 2. Schematic view of the CDF II silicon DAQ system.

The fact that all the L00 channels had to be read out due to noise pickup caused two problems. In the first place the long readout introduced high deadtime for the silicon system, limiting the rate at which events could be considered for a silicon vertex trigger. Secondly, L00, having the longest (and fixed) readout time, caused synchronous triggers conditions at high trigger rates. In order to solve both these problems the original design which included only one SRC for the whole silicon detector was modified. ISL and L00 are now controlled by a separate SRC and are only readout after a Level 2 accept is issued (only the SVXII data is used by the SVT), this reduced the readout for the SVT decision by, on average, a factor of more than two and reduced the odds of having a wire-bond failure since the readout time of SVX II is not fixed but depends on detector occupancy.

Another source of concern has been the stability of the clock signals received by the SRC. During the data taking period of November 2003 to July 2004 occasional glitches in the input clock signals to the SRC sometimes brought the whole DAQ system to a halt because a large number of SVX3D chips would go into a high current consumption state. This was caused by an unforeseen idiosyncrasy in the readout chips which require continuous communication. Firmware improvements have made the SRC more robust to glitches, however some incidents continue to occur where the input clock signals are completely lost. Since the FPGAs in the SRC are full, a new board, the clock cloning card, which will generate all the clock signals needed by the SRC, is being commissioned. Initial tests of the board were successful, and installation is scheduled for the coming shutdown.

The silicon DAQ system was designed to run to 50 kHz L1A rates. However, the resonance protection board halted data taking too often at high trigger rates and high luminosities, making the data taking process difficult. It was expected that at high trigger rates stochastic synchronous trigger conditions would occur, specially at high luminosity (i.e. high occupancy). A simulation of the trigger system was used to tune the resonance board parameters. As a result data taking at rates as high as 40kHz proceeded with few interruptions and no wire-bond failures.

4. Operational Experience

Maintaining the detector at a high efficiency level requires a significant effort compared to other CDF sub-detector systems, specially in terms of human resources. At least two, of about ten, Silicon Operations Group members are on 24-hr call. The recurring problems which most often occupy the group at the time of this writing are beam related incidents, power supply failures, and command and data path failures. Most of the failure modes are understood and often require access

to the collision hall (on average three times per month).

The silicon detector is specially sensitive to beam incidents given its proximity to the beam line. These incidents are a major source of concern, since they can cause permanent damage to the detector. The front-end chips have been most affected during these types of incidents (5), presumably because the large instantaneous radiation dose induces large currents, which may cause the permanent loss of communication with the affected chip and all the chips down the daisy-chain. Though several ladders exhibited temporary problems immediately after beam incidents, only one ISL ladder was permanently damaged during 2005. The new collimators and the constant monitoring of the beam status by the shift crew helped improve the situation.

The CDF silicon detector uses custom powers supplies manufactured by CAEN which are located in the collision hall. Different failure modes have been observed (spontaneous loss of power, corrupted read-back, and loss of communication with the module) which are believed to be induced by radiation. CDF and CAEN are collaborating to investigate whether these failures can be prevented.

There are several failures modes, which are mostly understood, that affect the communication of commands to and data from the detector. Problems with the optical transmission of data include situations where the signal levels of the Dense Optical Interface Modules (DOIMs) (6) fall below the detection level of the optical receivers and malfunctioning receivers. The possibility of replacing the current DOIM receivers with a more sensitive version is under study (5). Failures of the ICs of the FIB and readout buffer boards are common. The FIB boards RAMs are affected by single-event-upsets, but most of the time these are detected and corrected by the on board firmware. The readout buffer boards also have IC failures, but the failure rate is much lower since these boards are not in the collision hall.

5. Summary

The CDF II silicon detector has been running stably for three years. The data collection efficiency is high, 93% of the ladders are powered and 84% are providing data with an error rate $< 1\%$. A significant effort is needed from the collaboration to keep the detector at this level of performance. Since the commissioning period ended, several DAQ issues have been addressed to keep up with the improving performance of the accelerator.

References

[1] R. Blair, et al., The CDF II detector technical design report, FERMILAB-Pub-96/390-E.

[2] M. Garcia-Sciveres, et al., The SVX3D integrated circuit for dead-timeless silicon strip readout, Nucl. Instr. Meth. A435 (1999) 58.

[3] C. S. Hill, Initial experience with the CDF Layer 00 silicon detector, Nucl. Instr. Meth. A511 (2003) 118.

[4] G. Bolla, et al., Wire-bond failures induced by resonant vibrations in the CDF silicon tracker, Nucl. Instr. Meth. A518 (2004) 277.

[5] A. Mitra, Operations experience of the CDF Run II Silicon, 7th International Conference on Position Sensitive Detectors, Liverpool, UK, 12 September, 2005.

[6] M. L. Chu, et al., Radiation hardness of the 1550-nm edge emitting laser for the optical links of the CDF silicon tracker, Nucl. Instr. Meth. A 541 (2005) 208.