A Custom 96-Channel VME TDC for the CDF Detector for Tevatron Collider Run II

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Abstract-- **A 96-channel TDC (Time to Digital Converter) VME board was designed for the CDF detector in Tevatron Collider Run II at Fermilab. The features include: a custom ASIC (Application Specific Integrated Circuit) component that provides time measurements of signals from the various detector elements; a DSP (Digital Signal Processor) that formats the digitized data sent to the data acquisition system; a built-in diagnostic system; a VME interface to read out the data and control the board configuration. This TDC board implements the CDF data acquisition and trigger protocols. The TDCs were designed initially to achieve 300 Hz readout rate. More than 400 of these TDCs provide 1 ns resolution timing for signal pulses from wire chambers, scintillator panels, and calorimeter towers. In addition, custom daughter boards connected to the TDCs provide data to the level-1 trigger system. We describe the functionality of the TDC boards and performance during Run II operation.**

I. Introduction

THE CDF detector [1]-[2] is one of two large experiments currently running at Fermilab's Tevatron, a proton-antiproton collider operating at a center-of-mass energy of 1.96 TeV. The 36 circulating bunches of protons and antiprotons intersect at the two detectors at a rate of 1.7 MHz. CDF uses timing information from over 40,000 channels of wire chamber, scintillator panel and calorimeter tower output signals for triggering on and reconstructing events from the proton-antiproton collisions. For example, electrically charged particles emanating from a proton-antiproton collision travel through the COT (Central Outer Tracker) wire chamber and ionize gas molecules within the chamber volume. The arrival time of signals caused by liberated electrons striking the chamber wires indicates how far the passing particle was from the wire. Using such measurements from multiple wire planes allows one to reconstruct the trajectory of the charged particle through the tracking volume. TDCs are used to measure the arrival time of a detector signal relative to a reference signal from the trigger system.

To simplify commissioning and operations, CDF sought a single TDC board design to readout all detector components that need signal timing. No commercial TDCs fulfilled all the requirements, so a custom TDC was designed to satisfy the specifications of the various detector subsystems and to follow the CDF trigger [3], [4] and DAQ (data-acquisition) system [5] protocols. The CDF TDC is a 96-channel VME board that employs a custom ASIC, the JMC96, to provide 1 ns resolution timing on the incoming detector signals. More than 400 of these TDC boards are used throughout the experiment.

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II. Specifications

The CDF TDC must satisfy the needs of several different detector systems. All detectors require the TDC to resolve the leading and trailing edges of multiple signals (hits) for a given event. The COT wire chamber and scintillator systems need 1 ns time resolution. The long drift times of the muon wire chambers require the TDC to be capable of detecting hits within a 2 μs long window after a beam crossing.

The TDC must also follow the CDF trigger and DAQ specifications. The level-1 trigger has a "deadtimeless" 5.5 μs deep pipeline operating synchronously. Data propagates down the pipeline while the level-1 decision is made by the trigger hardware. The level-1 trigger decision reaches the front-end boards, such as the TDCs, as the relevant data reaches the end of the pipeline. Level-1 accepts cause the data to be stored in one of four level-2 buffers while the level-2 trigger decisions are made asynchronously to the level-1 decisions. Upon a level-2 accept, data is read out from the front-end boards and sent to the event builder. The event builder assembles the data from all subsystems and sends them to the level-3 trigger computer farm.

The initial CDF Run II trigger and DAQ specifications called for a 45 kHz level-1 accept rate and a 300 Hz level-2 accept and readout rate. Planned upgrades specify a level-2 accept and readout rate of up to 1 kHz.

III. Board Overview

The TDC boards have a 9U×400 mm form factor and reside in VIPA-standard crates with a VME-based processor board (MVME 23XX or MVME 24XX). Also in the crate is another CDF-specific board, called the TRACER, to provide clock and trigger on user-defined pins of the J2 backplane. The TDC receives those signals and routes them to components on the board.

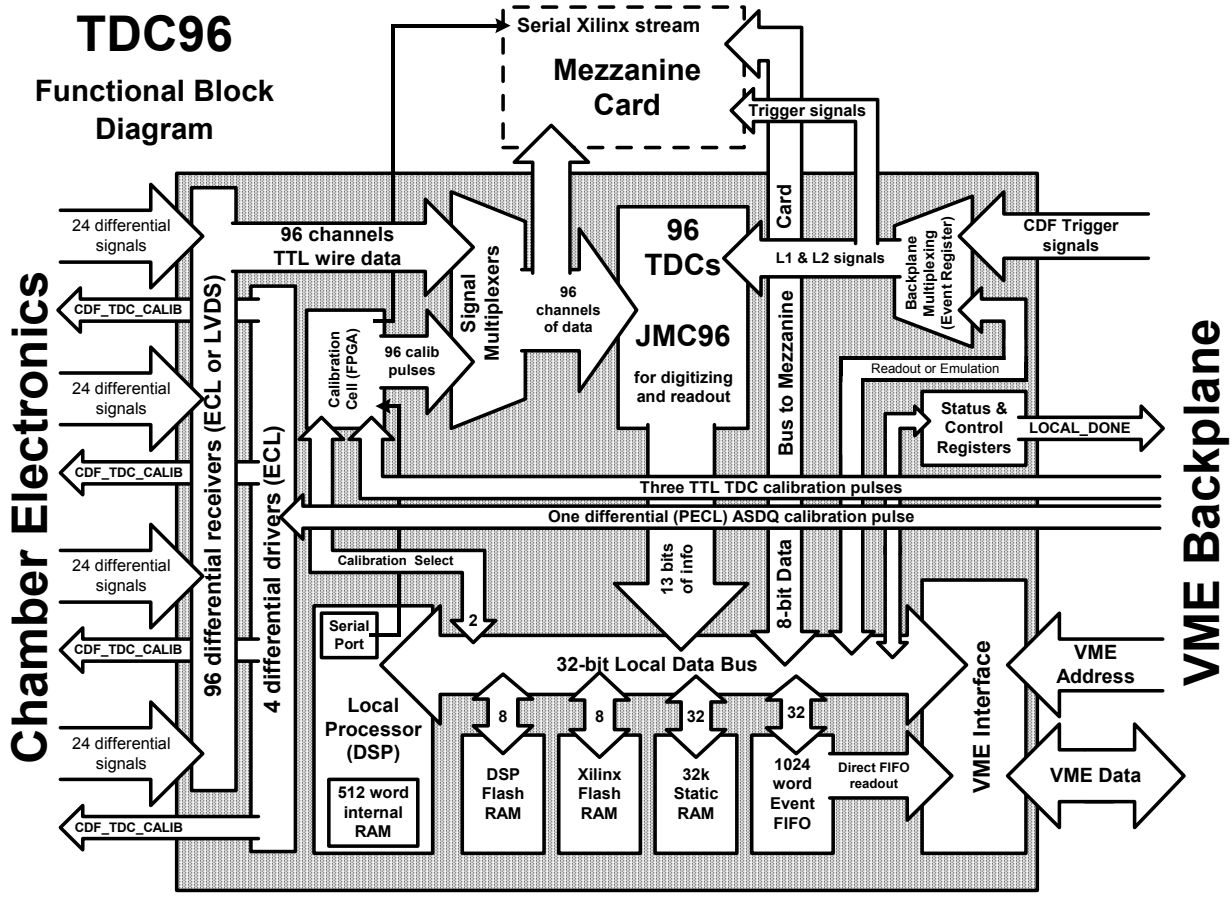

Fig. 1. Functional block diagram of the CDF TDC board. The main features of the board and connections between them are indicated.

The main features of CDF TDC board, designed at the University of Michigan, are depicted in Figure 1. Cables carrying the differential signals from the detector hardware connect to the TDC via four front-panel connectors. The signals are terminated at the inputs of the receiver components which also convert the differential inputs to TTL. The TDC board was laid out to accommodate either differential LVDS or differential ECL input signals. Space is available for receiver chips of both signal types, but only the components for one are installed. The LVDS and ECL boards also use different front-panel connectors.

The 96 TTL-level signals, as well as the 96 signals from the so-called Calibration Cell FPGA (Field Programmable Gate Array), are routed to the multiplexers that select which signals are sent to the JMC96 chips for digitization. The Calibration Cell is used as an in-situ diagnostic tool; it can select and fan out one of three user-controlled signals from the backplane to any of the TDC chips. Those signals can be used to verify operation of the 96 channels independent of the front-panel signals. Normally, the multiplexers send the signals from the front-panel inputs to the JMC96 chips.

The TDC uses an on-board DSP (Texas Instruments TMS 320C32-60) to process and format event data, to respond to DAQ requests, and to configure the Calibration Cell FPGA and the rest of the board at power-up. Although it is rated for 60 MHz operation, the DSP is under-clocked at 41.6667 MHz so that one clock is needed for the DSP and the JMC96 chips. The DSP's executable is stored in flashram. When the DSP boots, it assembles 8-bit code bytes from flashram into 32-bit instruction words and stores them in the on-board SRAM (static ram).

The TDC has various other resources on-board. Flashram is used to store DSP code, FPGA configuration bitstreams, board identifications (serial number, input signal type, subdetector) and calibration constants. The flashrams are programmed by VME, so it is convenient to update firmware or other information in-situ. The static ram is used to hold the DSP executable while the DSP is running. There are various other registers to control configuration and report status. There is a 32-bit wide, 1024-word deep, dual-ported FIFO (the event FIFO) that stores the data after the DSP has processed an event.

The TDC uses the Cypress CY7C960 and CY7C964 chipset as its VME interface. All communication is done using 32-bit data transfers. VME transactions can be used to configure the

board for operation, program the on-board flashram, and readout data from the event FIFO.

All board resources (memory, registers, JMC96 chips) can be accessed locally by the DSP and externally via VME. The DSP and VME can not access these resources simultaneously, so dedicated circuitry is used to halt the DSP while VME accesses a resource on the DSP's local bus. The event FIFO is an exception: VME can read this FIFO directly, so one event's data can be read from the FIFO while the DSP writes the next event's data to the FIFO. This feature allows higher DAQ bandwidth.

The TDC can also host custom daughter cards that are part of the level-1 trigger system. The cards mount onto three dedicated, 140-pin SMT connectors and receive the TTL-level signals input to the JMC96 chips. They also receive the CDF-specific clock and trigger signals from the TDC board. The DSP can configure any FPGAs on the daughter card using a bitstream stored in the TDC flashram. The daughter cards differ for each detector subsystem, but they share the ability to form "trigger primitives" based on hit coincidence or timing and pass that data via the TDC board and a dedicated crate backplane (J3) to the level-1 trigger system for additional processing.

IV. JMC96 Chip Overview

The JMC96 chip, designed at the University of Michigan, contains all of the functionality needed for signal digitization and implementing the CDF trigger system protocol. Figure 2 shows a block diagram of the JMC96. The TTL-level input signal enters a 48-stage delay line. The delay is controlled by an internal phase-locked loop that is driven by a crystal oscillator on the TDC board. The crystal oscillator stability, 1 part in 10,000, determines the overall accuracy of the time digitization. Every 48 ns, the delay line is copied to a 48-bit register, such that the register contains a 48 ns record of the input signal digitized in 1 ns bins. That data then enters a shift register whose length corresponds to the 5560 ns length of the level-1 trigger pipeline. The level-1 trigger decision for a given event reaches the TDC boards by the time that events data reaches the end of the pipeline. A level-1 accept causes the last 2 μs of data in the pipeline to be copied to one of four level-2 buffers specified in the level-1 accept; otherwise, the data drops off the end of the pipeline. The level-1 accept signals are propagated down a second 48-stage delay cell and stored in one of four level-1 registers for later use.

The data stored in a level-2 buffer remains there until overwritten by a future level-1 accept for the same buffer. Once the TDC chips receive a level-2 accept from the trigger system, the times of any hits are calculated. First, the time of the level-1 accept is determined from the appropriate level-1 register. Then, the data stored in the corresponding level-2 buffer are scanned to identify leading (0→1) and trailing (1→0) edges of input signal pulses. The time of each edge transition is calculated and then has the level-1 accept time subtracted from it. For each leading or trailing edge found, a 13-bit "edge word" is written to an on-chip FIFO. The edge word consists of 1 bit for the edge sense (leading or trailing) and 12 bits for the edge time relative to the level-1 accept. The DSP reads the edge words from the on-chip FIFO when it processes the hit data to be stored in the TDC event FIFO.

The JMC96 production-run chips were manufactured in 1996 by Hewlett-Packard on a 0.8 micron feature line. The die size was approximately 6 mm × 6 mm. The chips were packaged as a 44-pin PLCC component. Approximately 80% of the 60000 packaged chips passed the post-production testing procedure.

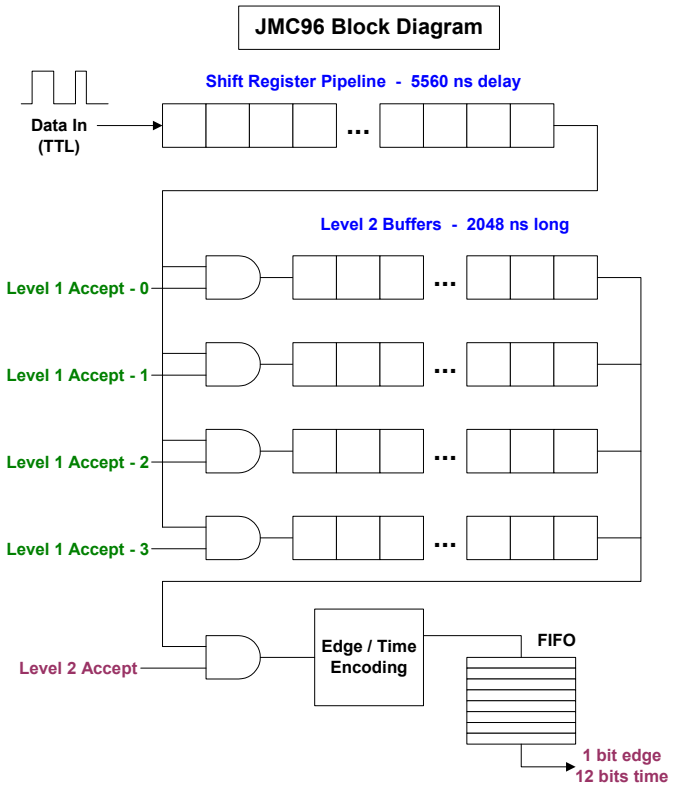

Fig. 2. Block diagram of the JMC96 TDC chip. The level-1 trigger pipeline, the four level-2 buffers, time encoding, and readout FIFO are shown.

V. Calibration

After passing initial checkout tests, every TDC board undergoes a calibration procedure. This calibration accounts for channel-to-channel differences in the input receiver circuitry and propagation delays of the input signals and the level-1 accept signals across the board. The linearity can not be corrected since it determined solely by the crystal oscillator.

In order to calibrate the offsets to 1 ns, a Tektronix HFS 9003 pulse generator (1 ps resolution, 250 ps rise time) was used to pulse the front-panel inputs and the level-1 accept line with a predetermined pattern. The TDC was read out, and the reported times were used to calculate the channel-to-channel offset constants. These constants are stored in a database and

in the TDC flashram. The DSP reads the offsets and applies the correction to the reported hit times when processing an event. Typical channel-to-channel variations are 3-8 ns.

VI. Event Processing and Readout

A primary function of the DSP is to read the edge words from the 96 TDC chips, process that data the desired format, and then write that reformatted data into the TDC board event data FIFO. After a level-2 accept, the DSP reads out any edge words from the 96 TDC chips. The DSP pairs up leading and trailing edges to calculate a start time and width for each input pulse. The DSP applies the calibration constant to the start time to correct the channel-to-channel offsets. The DSP can also apply a cut on the pulse start time so that hits outside a specified time window are discarded. Such a cut is useful for the COT TDCs, because the drift time causes the hits for each event to arrive within a 300 ns window of the TDC chips' 2 μs buffers. For each processed pulse, the DSP writes a 32-bit "hit word" to the event FIFO. A header word containing the number of hits, level-2 buffer number, and other identification data is formed by the DSP and written to the FIFO.

After the DSP has finished writing data to the event FIFO, the TDC board stops driving an open-collector line on the backplane called "TDC_DONE". The crate CPU can determine when all TDC boards have released TDC_DONE and are ready for readout. Then, the crate CPU begins reading data from the TDC event FIFOs using 32-bit VME block transfers to send the data into the event-building stream. When reading out a total of 7 kB of data from 16 TDCs in a single crate, we measured a 12 MB/s readout rate over VME. The trigger system does not issue the next level-2 accept until all crates, including TDC crates, are ready for readout. The crate CPU can readout a previous event's data while the DSP processes the next event with a level-2 accept.

VII. Performance

The TDC boards have met the original specifications for 1 ns time resolution and 300 Hz readout rate. To demonstrate the TDC timing measurement performance, we can use the in-situ diagnostic system. Each channel is pulsed repeatedly via the calibration cell FPGA to provide hits at several known times throughout the 2 μs internal buffers. The reported times are readout from the boards and compared to the expected times. For each channel, the RMS of the reported times is calculated separately for the hits at different pulsing times. The averages of those RMS times are shown in Figure 3 for all 96 channels of a single TDC board. Even without accounting for the jitter induced by the FPGA, the RMS of time reported by the TDC is less than 1 ns. To demonstrate TDC linearity of a channel, a line is fit to a plot of the average reported time versus the expected time for the different pulse times. Figure 4 shows the slope of the fitted line for each channel of a single TDC board. The linearity is better than 0.1%.

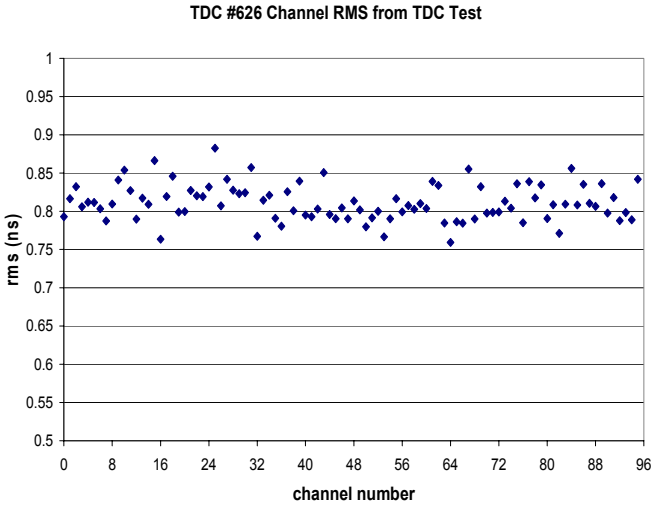

Fig. 3. RMS of reported time distribution for all channels of a single TDC board. Each channel was pulsed repeatedly using the in-situ diagnostic system The RMS is less than 1 ns.

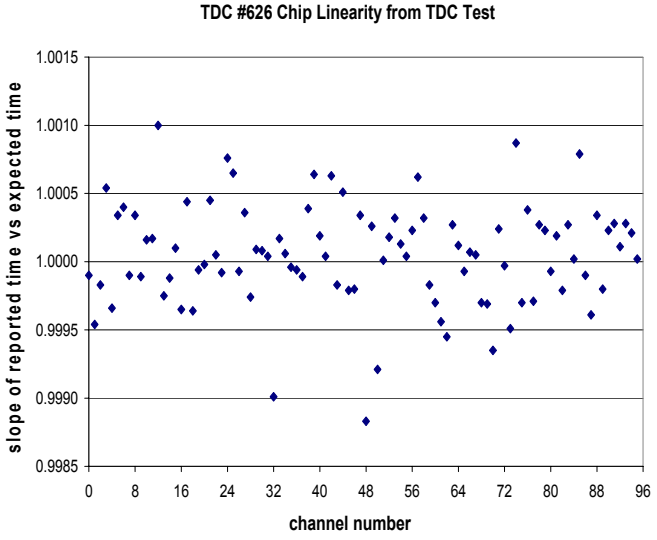

Fig. 4 Time linearity for all channels of single TDC board. Each channel was pulsed repeatedly using the in-situ diagnostic system. Each point is the slope of a line fitted to a plot of the average reported time versus the expected time for several pulse times. The linearity is typically better than 0.1% for each channel.

The TDCs have exceeded the initial 300 Hz level-2 accept and readout rate specification. At the highest Tevatron luminosities seen to date (~1 10^{32} $cm^{-2}s^{-1}$), the system, including the TDCs, has run at 25 kHz level-1 accept rates and 400 Hz level-2 accept rates. The present system is limited to approximately 420 Hz where the event builder system throughput starts causing significant deadtime.

The DSP processing time depends upon the occupancy of the associated detector hardware, i.e., the number of hits on each channel. Figure 5 illustrates the DSP processing time as a function of channel occupancy for two different DSP code

versions and for the two board revisions. Detector occupancies, especially for the COT, increase with Tevatron luminosity as the number of interactions per beam crossing rises. The COT TDCs typically have the greatest occupancies of all the detectors using TDCs. At Tevatron luminosities between 4 and 4.5 10^{32} $cm^{-2}s^{-1}$, COT TDCs with the highest occupancies are expected to have an average of 3 hits per channel [6].

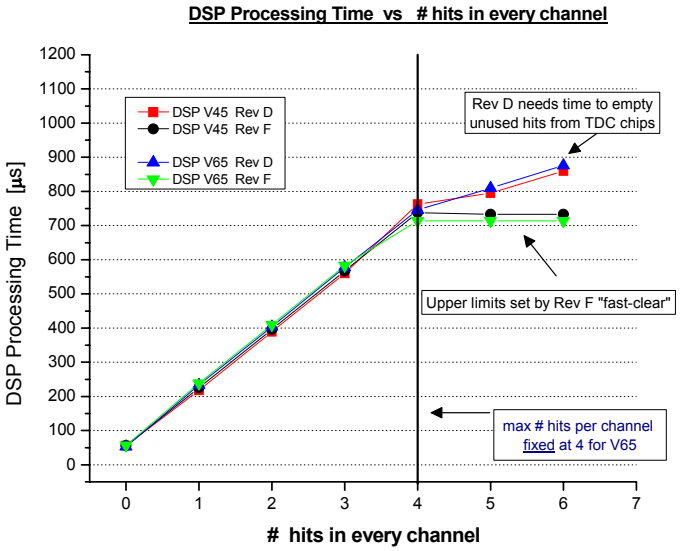

Fig. 5. DSP processing time as a function of the channel occupancy. DSP V45 is the current DSP code, whereas DSP V65 is a recently developed code that implements a more compact data format to reduce the data volume readout via VME. The curves for Revision D TDCs illustrate the time spent by the DSP emptying unused hits from the JMC96 chip FIFO. Revision F boards have a "fast-clear" feature that clears unused hits automatically.

As a result of the high occupancies, the COT TDCs require the most DSP processing time, and those TDC crates are typically the last ones to be ready for readout after a level-2 accept. Since the DSP event processing and data readout can occur simultaneously, the larger of DSP processing time and readout time sets the rate limit for the TDC crates. Using the current DSP V45 code at current luminosities, the readout of the TDC event FIFO takes longer than DSP processing. At the highest expected luminosities, the time to readout the expected data volumes from COT TDCs would not allow us to reach the new design goal of 1 kHz readout rate. However, the new DSP code V65 implements a compact data format that reduces the data volume by nearly a factor of two. With the smaller data volume, the DSP processing time becomes the limitation, and tests have shown that the 1 kHz readout goal can be reached with for the COT occupancies expected at the highest expected Tevatron luminosities.

VIII. Summary

For Tevatron Run II, the CDF experiment uses more than 400 custom VME TDCs to provide 1 ns timing for more than 40000 channels of detector hardware, including wire chambers, scintillator panels, and calorimeter towers. The 96-channel TDC designed by the University of Michigan employs a JMC96 custom ASIC to provide better than 1 ns RMS timing measurements and follow the CDF trigger and DAQ protocols. The TDCs already exceed the initial 300 Hz readout rate design, and the ultimate 1 kHz readout rate goal at the highest Tevatron luminosities is achievable.

IX. Acknowledgment

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X. References

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