

1	INPUT/OUTPUT DATA PROCESSING	49	...Masking
2	.Input/Output expansion	50	...Vectored
3	.Input/Output addressing	51	..Accessing via a multiplexer
4	..Address data transfer	52	.Input/Output data buffering
5	.Input/Output command process	53	..Alternately filling or emptying buffers
6	..Operation scheduling		
7	..Concurrently performing Input/Output operation and other operation unrelated to Input/Output	54	..Queue content modification
		55	..Contents validation
		56	..Buffer space allocation or deallocation
8	.Peripheral configuration	57	..Fullness indication
9	..Address assignment	58	.Input/Output process timing
10	..Configuration initialization	59	..Processing suspension
11	..Protocol selection	60	..Transfer rate regulation
12	..As input or output	61	..Synchronous data transfer
13	..By detachable memory	62	.Peripheral adapting
14	..Mode selection	63	..Universal
15	.Peripheral monitoring	64	..Via common units and peripheral-specific units
16	..Characteristic discrimination		
17	..Availability monitoring	65	..Input/Output data modification
18	..Activity monitoring	66	...Width conversion
19	..Status updating	67	...Keystroke interpretation
20	.Concurrent Input/Output processing and data transfer	68	...Data compression and expansion
		69	...Analog-to-digital or digital-to-analog
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22	.Direct Memory Accessing (DMA)	70	...Digital-to-digital
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24	..By command chaining	72	..Application-specific peripheral adapting
25	..Timing		
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27	..Via separate bus	74	...For data storage device
28	..With access regulating	100	INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
29	.Flow controlling		
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32	.Transfer termination	301	..Card insertion
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37	..Access dedication	105	.Protocol
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40	..Access prioritization	108	..Bus locking
41	...Dynamic	109	..Bus polling
42	...Group	110	..Bus master/slave controlling
43	...Physical position	111	..Rotational prioritizing (i.e., round robin)
44	...Prioritized polling		
45	...Time-slot accessing	112	..Bus request queuing
46	..Input/Output polling	113	..Centralized bus arbitration
47	...Polled interrupt	114	...Static bus prioritization
48	..Input/Output interrupting		

115 ...Physical position bus
 prioritization
 116 ...Dynamic bus prioritization
 117 ...Time-slotted bus accessing
 118 ...Delay reduction
 119 ..Decentralized bus arbitration
 120 ...Hierarchical or multilevel
 accessing
 121 ...Static bus prioritization
 122 ...Physical position bus
 prioritization
 123 ...Dynamic bus prioritization
 124 ...Time-slotted bus accessing
 125 ...Delay reduction
 305 ..Bus interface architecture
 306 ..Bus bridge
 307 ...Variable or multiple bus width
 308 ...Direct memory access (e.g.,
 DMA)
 309 ...Arbitration
 310 ...Buffer or que control
 311 ...Intelligent bridge
 312 ...Multiple bridges
 313 ...Peripheral bus coupling (e.g.,
 PCI, USB, ISA, and etc.)
 314 ...Common protocol (e.g., PCI to
 PCI)
 315 ...Different protocol (e.g., PCI
 to ISA)
 316 ..Path selecting switch
 317 ...Crossbar
 200 **ACCESS LOCKING**
 220 **ACCESS POLLING**
 240 **ACCESS ARBITRATING**
 241 ..Centralized arbitrating
 242 ..Decentralized arbitrating
 243 ..Hierarchical or multilevel
 arbitrating
 244 ..Access prioritizing
 260 **INTERRUPT PROCESSING**
 261 ..Multimode interrupt processing
 262 ..Interrupt inhibiting or masking
 263 ..Interrupt queuing
 264 ..Interrupt prioritizing
 265 ..Variable
 266 ..Programmable interrupt
 processing
 267 ..Processor status
 268 ..Source or destination identifier
 269 ..Handling vector

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