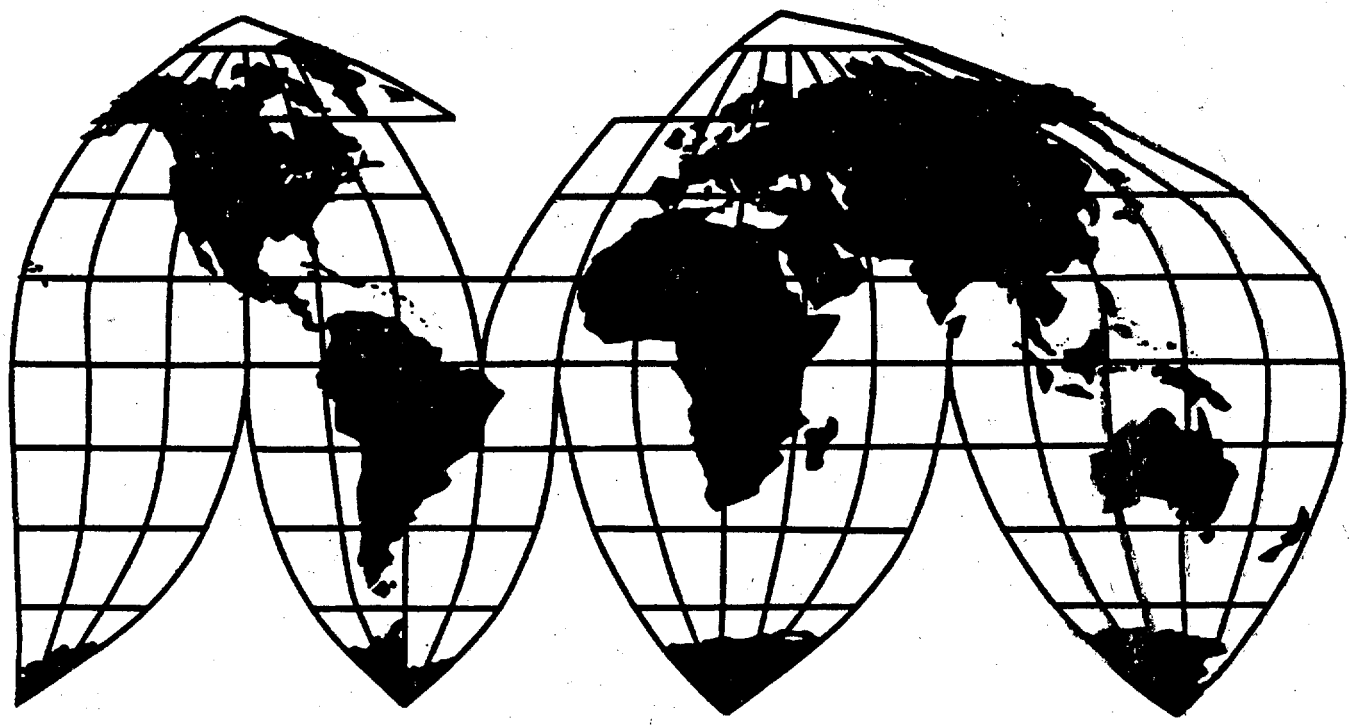
In the Matter of

Certain Hardware Logic Emulation Systems and Components Thereof

Investigation No. 337-TA-383

Publication 2991 **September 1996**

U.S. International Trade Commission



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U.S. International Trade Commission

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In the Matter of

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UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	
CERTAIN HARDWARE LOGIC EMULATION SYSTEMS AND COMPONENTS THEREOF	**Inv. No. 337-TA-383**

NOTICE OF COMMISSION DECISION NOT TO MODIFY OR VACATE AN INITIAL DETERMINATION GRANTING TEMPORARY RELIEF, AND ISSUANCE OF A TEMPORARY LIMITED EXCLUSION ORDER AND A TEMPORARY CEASE AND DESIST ORDER, SUBJECT TO POSTING OF BOND BY COMPLAINANT

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the Commission has determined not to modify or vacate the presiding administrative law judge's (ALJ) initial determination (ID) granting temporary relief in the above-referenced investigation, and has issued a temporary limited exclusion order and a temporary cease and desist order, subject to posting of a bond by complainant.

FOR FURTHER INFORMATION CONTACT: Jay H. Reiziss, Esq., Office of the General Counsel, U.S. International Trade Commission, telephone 202-205-3116.

SUPPLEMENTARY INFORMATION: This action is taken under the authority of section 337 of the Tariff Act of 1930, 19 U.S.C. § 1337, and Commission rule 210.66, 19 C.F.R. § 210.66.

On March 4, 1996, Quickturn Design Systems Incorporated ("Quickturn" or "complainant") filed a complaint under section 337 alleging unfair acts in the importation, the sale for importation, and the sale within the United States after importation of certain hardware logic emulation systems and components thereof by two proposed respondents: Mentor Graphics Corporation ("Mentor") of Wilsonville, Oregon and Meta Systems ("Meta") of Saclay, France (collectively "respondents"). Quickturn also simultaneously filed a motion for temporary relief.

In the motion for temporary relief, complainant alleged infringement of claims 1, 2, 3, and 15 of U.S. Letters Patent 5,448,496 and claim 8 of U.S. Letters Patent 5,036,473, both owned by Quickturn. On March 8, 1996, the Commission voted to institute an investigation of the complaint and to accept provisionally the motion for temporary relief, and published a notice of investigation in the Federal Register. 61 Fed. Reg. 9486 (March 8, 1996). The temporary

relief phase of this investigation was designated "more complicated" by the presiding ALJ on April 14, 1996 (Order No. 14). The ALJ held an evidentiary hearing on temporary relief from April 23, 1996, through May 4, 1996. Complainant, respondents, and the Commission investigative attorney (IA) participated in the hearing. Thereafter, oral argument was held before the ALJ on June 5, 1996. The Commission received submissions on the issues of remedy, the public interest, and bonding from all parties on June 23, 1996, in accordance with Commission rule 210.67(b).

On July 8, 1996, the ALJ issued his ID (Order No. 34) granting Quickturn's motion for temporary relief. On July 18, 1996, respondents and the IA filed written comments on the temporary relief ID, as provided for in rule 210.66(c). Complainant and the IA filed replies to respondents' comments, and respondents filed a reply to the IA's comments on July 22, 1996, as provided for in rule 210.66(e).

The Commission, having considered the ID, the comments and responses to comments of the parties, and the record in this investigation, determined that there were no clearly erroneous findings of fact, no errors of law, or policy reasons to vacate or modify the ID. Consequently, pursuant to Commission rule 210.66(f), the ID became the Commission's determination on the issue of whether there is reason to believe a violation of section 337 has occurred.

The Commission having determined that there is reason to believe that a violation of section 337 has occurred in the importation, sale for importation, or sale in the United States of the accused hardware logic emulators, subassemblies thereof, or component parts thereof, and having determined that temporary relief is warranted, considered the issues of the appropriate form of such relief, whether the public interest precludes issuance of such relief, complainant's bond, and respondents' bond during the period such relief is in effect.

The Commission determined that a temporary limited exclusion order and a temporary cease and desist order directed to respondent Mentor are the appropriate form of temporary relief. The Commission further determined that the statutory public interest factors do not preclude the issuance of such relief, and that respondents' bond under the temporary limited exclusion order and the temporary cease and desist orders shall be in the amount of forty-three (43) percent of the entered value of the imported articles.

Commission rule 210.68 requires that all bonds posted by a complainant must be approved by the Commission Secretary before the temporary relief which the bond will secure will be issued. Consequently, the issuance of temporary relief described in the preceding paragraph is subject to the posting and approval of complainant's bond in the amount of $200,000. Complainant is to file its bond with the Commission Secretary within seven (7) business days of publication of this notice in the Federal Register.

Copies of all nonconfidential documents filed in connection with this investigation are available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street SW., Washington, D.C. 20436,

telephone 202-205-2000. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on 202-205-1810.

By order of the Commission.

Donna R. Koehnke

Donna R. Koehnke
Secretary

Issued: August 5, 1996

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of **CERTAIN HARDWARE LOGIC EMULATION SYSTEMS AND COMPONENTS THEREOF**	**Inv. No. 337-TA-383**

ORDER

On March 4, 1996, Quickturn Design Systems Incorporated ("Quickturn" or "complainant") filed a complaint under section 337 of the Tariff Act of 1930 (19 U.S.C. § 1337) alleging unfair acts in the importation, the sale for importation, and the sale within the United States after importation of certain hardware logic emulation systems and components thereof by two proposed respondents: Mentor Graphics Corporation ("Mentor") of Wilsonville, Oregon and Meta Systems ("Meta") of Saclay, France (collectively "respondents"). Complainant also simultaneously filed a motion for temporary relief.

In the motion for temporary relief, complainant alleged infringement of claims 1, 2, 3, and 15 of U.S. Letters Patent 5,448,496 and claim 8 of U.S. Letters Patent 5,036,473, both owned by Quickturn. On March 8, 1996, the Commission voted to institute an investigation of the complaint and to accept provisionally the motion for temporary relief, and published a notice of investigation in the Federal Register. 61 Fed. Reg. 9486 (March 8, 1996). The temporary relief phase of this investigation was designated "more complicated" by the presiding administrative law judge (ALJ) on April 14, 1996 (Order No. 14). The ALJ held an evidentiary hearing on temporary relief from April 23, 1996, through May 4, 1996. Complainant, respondents, and the Commission investigative attorney (IA) participated in the hearing.

Thereafter, oral argument was held before the ALJ on June 5, 1996. The Commission received submissions on the issues of remedy, the public interest , and bonding from all parties on June 23, 1996, in accordance with Commission rule 210.67(b).

On July 8, 1996, the ALJ issued his ID (Order No. 34) granting Quickturn's motion for temporary relief. On July 18, 1996, respondents and the IA filed written comments on the temporary relief ID, as provided for in rule 210.66(c). Complainant and the IA filed replies to respondents' comments, and respondents filed a reply to the IA's comments, as provided for in rule 210.66(e).

The Commission, having determined to adopt the presiding ALJ's ID concluding that there is reason to believe that there is a violation of section 337 in the importation, sale for importation, or sale in the United States after importation of the accused hardware logic emulators, and having determined that temporary relief is warranted, considered the issues of the appropriate form of such relief, whether the public interest precludes issuance of such relief, complainant's bond, and respondents' bond during the period that temporary relief is in effect. The Commission has determined that a temporary limited exclusion order and a temporary cease and desist order (issued as a separate order) are the appropriate form of temporary relief. The Commission has further determined that the statutory public interest factors do not preclude the issuance of such relief, and that respondents' bond during the period of temporary relief shall be in the amount of forty-three (43) percent of the entered value of infringing imported hardware logic emulators and components thereof. Finally, the Commission has determined that complainant's bond shall be in the amount of $200,000.

Accordingly, it is hereby ORDERED THAT --

1. Hardware logic emulation systems, subassemblies thereof, and components thereof, including logic boards for use therein, manufactured by Meta Systems of Saclay, France, or any of its affiliated companies, parents, subsidiaries, licensees, contractors, or other related entities, or their successors or assigns, that infringe claim 8 of U.S. Letters Patent 5,036,473 or claims 1, 2, 3, or 15 of U.S. Letters Patent 5,448,496 are excluded from entry for consumption into the United States during the pendency of USITC Investigation No. 337-TA-383, except under license of the patent owner or as provided by law.

2. The temporary relief described in the preceding paragraph of this Order is issued subject to the posting by complainant and approval by the Commission of a complainant's bond in the amount of $200,000.

3. In accordance with subsection (l) of section 337, the provisions of this Order do not apply to hardware logic emulators, subassemblies thereof, and components thereof imported by or for the United States.

4. The provisions of this Order do not apply to articles certified by the importer to the Customs Service to be imported for use as a replacement for an identical or substantially equivalent subassembly or component on a hardware logic emulation system imported into the United States prior to the effective date of this Order.

5. The articles identified in paragraph (1) of this Order are entitled to entry into the United States under bond in the amount of forty-three (43) percent of entered value from the day after the Commission has approved complainant's posted bond until the day after the Commission issues its final determination in Investigation 337-TA-383, unless, pursuant to subsection (j) of section 337, the President notifies the Commission within 60 days after the date he receives this Order, that he disapproves this Order.

6. The Commission may amend this Order in accordance with the procedure described in section 210.76 of the Commission's Rules of Practice and Procedure, 19 C.F.R. § 210.76.

7. The Secretary shall serve copies of this Order upon each party of record in this investigation and upon the Department of Health and Human Services, the Department of Justice, the Federal Trade Commission, and the U.S. Customs Service.

8. Notice of this Order shall be published in the Federal Register.

By order of the Commission.

Donna R. Koehnke
Secretary

Issued: **August 5, 1996**

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of **CERTAIN HARDWARE LOGIC EMULATION SYSTEMS AND COMPONENTS THEREOF**	**Inv. No. 337-TA-383**

ORDER TO CEASE AND DESIST

IT IS HEREBY ORDERED THAT Mentor Graphics Corporation, 8005 S.W. Boeckman Road, Wilsonville, Oregon, 97070, cease and desist from importing, selling for importation, distributing, offering for sale, selling, advertising, soliciting U.S. agents or distributors for, or otherwise transferring in the United States hardware logic emulation systems, subassemblies thereof, and components thereof, covered by claims 1, 2, 3, or 15 of U.S. Letters Patent 5,448,496 or claim 8 of U.S. Letters Patent 5,036,473, during the pendency of USITC Investigation No. 337-TA-383.

I

(Definitions)

As used in this Order:

(A) "Commission" shall mean the United States International Trade Commission.

(B) "Complainant" shall mean Quickturn Design Systems, Inc., 440 Clyde Avenue, Mountain View, California, 94043.

(C) "Respondent" and "Mentor" shall mean Mentor Graphics Corporation, 8005 S.W. Boeckman Road, Wilsonville, Oregon, 97070.

(D) "Person" shall mean an individual, or any non-governmental partnership, firm, association, corporation, or other legal or business entity other than the above Respondent or its majority owned and/or controlled subsidiaries, their successors, or assigns.

(E) "United States" shall mean the fifty states, the District of Columbia, and Puerto Rico.

(F) "Covered product" shall mean hardware logic emulation systems, subassemblies thereof, and components thereof that the Commission has found likely to infringe claims 1, 2, 3, or 15 of U.S. Letters Patent 5,448,496 or claim 8 of U.S. Letters Patent 5,036,473.

(G) The terms "import" and "importation" refer to importation for entry for consumption under the Customs laws of the United States.

II

(Applicability)

The provisions of this Cease and Desist Order shall apply to Respondent and to its principals, stockholders, officers, directors, employees, agents, licensees, distributors, controlled (whether by stock ownership or otherwise) and/or majority owned business entities, successors and assigns, and to each of them, and to all other persons who receive actual notice of this Order by service in accordance with section VII hereof, insofar as they are engaging in conduct prohibited by Section III, *infra*, for, with, or otherwise on behalf of Respondent.

III

(Conduct Prohibited)

The following conduct of Respondent in the United States is prohibited by this Order. Respondent shall not:

(A) import or sell for importation into the United States covered product except under license of the patent owner;

(B) distribute, offer for sale, sell, or otherwise transfer (except for exportation) in the United States imported covered product except under license of the patent owner;

(C) advertise covered product; or

(D) solicit U.S. agents or distributors for imported covered product.

IV

(Conduct Permitted)

Notwithstanding any other provision of this Order, specific conduct otherwise prohibited by the terms of this Order shall be permitted if, in a written instrument, the owner of U.S. Letters Patent 5,448,496 and U.S. Letters Patent 5,036,473 licenses or authorizes such specific conduct, or such specific conduct is related to the importation or sale of covered product by or for the United States. Nothwithstanding any other provision of this order, Respondent may engage in conduct otherwise prohibited of this Order if such conduct is directly related to the sale of covered product imported on or after August 5, 1996, which covered product is subject to the entry bond as set forth in the temporary limited exclusion order issued by the Commission on August 5, 1996. Notwithstanding any other provision of this Order, Respondent may furnish

services to its customers, including installation of replacement parts authorized to be imported under paragraph 4 of the temporary limited exclusion order issued herewith, that are directly related to covered product imported and sold in the United States prior to the effective date of this Order.

V

(Reporting)

For purposes of this reporting requirement, the reporting periods shall commence on January 1 and July 1 of each year, and shall end on the subsequent June 30 and December 31, respectively. The first report required under this section shall cover the period August 5, 1996, to December 31, 1996. This reporting requirement shall continue in force until the day after the Commission issues its final determination in Investigation No. 337-TA-383, unless, pursuant to subsection (j) of section 337 of the Tariff Act of 1930, the President notifies the Commission within sixty (60) days after the date he receives this Order, that he disapproves this Order.

Within thirty (30) days of the last day of the reporting period, Respondent shall report to the Commission:

(A) The quantity in units and the value in dollars of covered product that Respondent has imported or sold in the United States during the reporting period and the quantity in units and value of covered product that remains in inventory at the end of the reporting period.

(B) All contracts, whether written or oral, entered into during the reporting period in question, to sell or otherwise transfer covered product during the reporting period.

In connection with the importation and sales or other transfers referred to in paragraphs (A) and (B) above, Respondent shall provide the Commission with two copies of all invoices,

delivery orders, bills of lading, and other documents concerning the importation or sale in question. Such copies shall be attached to the reports required by paragraphs (A) and (B) above.

Any failure to make the required report or the filing of any false or inaccurate report shall constitute a violation of this Order.

VI

(Recordkeeping and Inspection)

(A) For the purpose of securing compliance with this Order, Respondent shall retain any and all records relating to the sale, offer for sale, or distribution in the United States of covered product made and received in the usual and ordinary course of business, whether in detail or in summary form, for a period of two (2) years from the close of the fiscal year to which they pertain.

(B) For the purposes of determining or securing compliance with this Order and for no other purpose, and subject to any privilege recognized by the federal courts of the United States, duly authorized representatives of the Commission, upon reasonable written notice by the Commission or its staff, shall be permitted access and the right to inspect and copy in Respondent's offices during office hours, and in the presence of counsel or other representatives if Respondent so chooses, all books, ledgers, accounts, correspondence, memoranda, and other records and documents, both in detail and in summary form as are required to be retained by subparagraph VI(A) of this Order.

VII

(Service of Cease and Desist Order)

Respondent is ordered and directed to:

(A) Serve, within fifteen (15) days after the issuance of this Order, a copy of this Order upon each of its respective officers, directors, managing agents, agents, and employees who have any responsibility for the marketing, distribution, or sale of covered product in the United States;

(B) Serve, within fifteen (15) days after the succession of any persons referred to in subparagraph VII(A) of this Order, a copy of the Order upon each successor; and

(C) Maintain such records as will show the name, title, and address of each person upon whom the Order has been served, as described in subparagraphs VII(A) and VII(B) of this Order, together with the date on which service was made.

(D) The obligations set forth in paragraphs VII (B) and (C) above shall remain in effect until the day after the Commission issues its final determination in Investigation No. 337-TA-383, unless, pursuant to subsection (j) of section 337 of the Tariff Act of 1930, the President notifies the Commission within 60 days after the date he receives this Order, that he disapproves this Order.

VIII

(Confidentiality)

Any request for confidential treatment of information obtained by the Commission pursuant to Sections V and VI of the Order should be in accordance with Commission Rule 201.6, 19 C.F.R. § 201.6. For all reports for which confidential treatment is sought, Respondent must provide a public version of such report with confidential information redacted.

Information obtained by the means provided for in sections V and VI of this Order will be made available only to the Commission and its authorized representatives, will be entitled to

confidential treatment, and will not be divulged by any authorized representative of the Commission to any person other than duly authorized representatives of the Commission, except as may be required in the course of securing compliance with this Order, or as otherwise required by law. Disclosure hereunder will not be made by the Commission without ten (10) days prior notice in writing to Respondent.

IX

(Enforcement)

Violation of this Order may result in any of the actions specified in section 210.75 of the Commission's Rules of Practice and Procedure, 19 C.F.R. § 210.75, including an action for civil penalties in accordance with section 337(f) of the Tariff Act of 1930, 19 U.S.C. § 1337(f), and any other action as the Commission may deem appropriate. In determining whether Respondent is in violation of this Order, the Commission may infer facts adverse to Respondent if Respondent fails to provide adequate or timely information.

X

(Modification)

The Commission may amend this Order on its own motion or in accordance with the procedure described in section 210.76 of the Commission's Rules of Practice and Procedure, 19 C.F.R. § 210.76.

XI

(Bonding)

With respect to covered product imported prior to August 5, 1996, the conduct prohibited by paragraph III of this Order may be continued during the period the during which

this Order is in effect subject to Respondent posting a bond in the amount of forty-three (43) percent of the entered value of the covered product in question. This bond provision does not apply to conduct which is otherwise permitted by paragraph IV of this Order. Covered product imported on or after August 5, 1996, is subject to the entry bond as set forth in the limited temporary exclusion order issued by the Commission on August 5, 1996, and is not subject to this bond provision.

The bond is to be posted in accordance with the procedures established by the Commission for the posting of bonds by complainants in connection with the issuance of temporary exclusion orders.

The bond and any accompanying documentation is to be provided to and approved by the Commission prior to the commencement of conduct which is otherwise prohibited by paragraph III of this Order.

The bond is to be forfeited in the event that the President approves, or does not disapprove within the Presidential review period, the Commission's Orders of August 5, 1996, or any subsequent final order issued after the completion of Investigation No. 337-TA-383, unless the U.S. Court of Appeals for the Federal Circuit, in a final judgment, reverses any Commission final determination and order as to Respondent on appeal, or unless Respondent exports the products subject to this bond or destroys them and provides certification to that effect satisfactory to the Commission.

The bond is to be released in the event the President disapproves this Order and no subsequent order is issued by the Commission and approved, or not disapproved, by the President, upon service on Respondent of an Order issued by the Commission based upon

application therefor made by Respondent to the Commission.

By Order of the Commission

Donna R. Koehnke
Secretary

Issued: August 5, 1996

The following pages have been omitted from the public version of Order No 34: Initial Determination because they contain only confidential business information:

82, 86, 97, 124, 164--167, 170--174, 180, 184, 194--198, 201, 215--218, 228, 231--240, 243, 249--251, 265--267, 271, 276, 279, 293, 311--313, 355--380.

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	
CERTAIN HARDWARE LOGIC EMULATION SYSTEMS AND COMPONENTS THEREOF	Inv. No. 337-TA-383

COMMISSION OPINION ON REMEDY, THE PUBLIC INTEREST, AND BONDING

We have determined to adopt the presiding administrative law judge's (ALJ) initial determination (ID) concluding that there is reason to believe that there is a violation of section 337 in the importation, sale for importation, or sale in the United States after importation of the accused hardware logic emulation systems.[1] Specifically, we adopt the ALJ's finding that it is likely that the patents in issue are valid and infringed by respondents' imported hardware logic emulation systems. We also adopt the ALJ's finding that complainant, Quickturn Design Systems Incorporated, a relatively small, single product company competing in the rapidly evolving hardware logic emulation market, is threatened with irreparable harm in the event temporary relief is not granted.

Having determined that temporary relief is warranted, we also determine that a temporary limited exclusion order and a cease and desist order are the appropriate forms of temporary relief. We have further determined that the statutory public interest factors do not preclude the issuance of such relief, and that respondents' bond during the period of the limited temporary exclusion order shall be in the amount of forty-three (43) percent of the entered value of infringing imported hardware logic emulators and components thereof. Finally, we have determined that the complainant's bond shall be in the amount of $200,000. This opinion explains the basis for these determinations.

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[1] These systems consist of reconfigurable logic devices, linked by reconfigurable interconnect devices, that can be programmed to replicate the operation of an integrated circuit ("IC") design to determine its performance characteristics under conditions that closely approximate the actual intended use. In other words, an emulation system configured with a particular circuit design can be connected to an external system (or "target" system) for which the circuit is designed, permitting the circuit to be tested under actual operating conditions (a process known as going "in-circuit"). The emulator's ability to verify the operation of a circuit design before actual fabrication of a prototype device results in substantial savings of development time and costs.

I. PROCEDURAL BACKGROUND

On March 4, 1996, Quickturn Design Systems Incorporated ("Quickturn" or "complainant") filed a complaint under section 337 of the Tariff Act of 1930 (19 U.S.C. § 1337) alleging unfair acts in the importation, the sale for importation, and the sale within the United States after importation of certain hardware logic emulation systems and components thereof by two proposed respondents: Mentor Graphics Corporation ("Mentor") of Wilsonville, Oregon and Meta Systems ("Meta") of Saclay, France (collectively "respondents"). Complainant also simultaneously filed a motion for temporary relief.

In the motion for temporary relief, complainant alleged infringement of claims 1, 2, 3, and 15 of U.S. Letters Patent 5,448,496 (the "'496 patent") and claim 8 of U.S. Letters Patent 5,036,473 (the "'473 patent") both owned by Quickturn. On March 8, 1996, the Commission voted to institute an investigation of the complaint and to accept provisionally the motion for temporary relief, and published a notice of investigation in the Federal Register.[2] The temporary relief phase of this investigation was designated "more complicated" by the presiding ALJ on April 14, 1996 (Order No. 14). The ALJ held an evidentiary hearing on temporary relief from April 23, 1996, through May 4, 1996. Complainant, respondents, and the Commission investigative attorney (IA) participated in the hearing. Thereafter, oral argument was held before the ALJ on June 5, 1996. The Commission received submissions on the issues of remedy, the public interest , and bonding from all parties on June 23, 1996, in accordance with Commission rule 210.67(b).

On July 8, 1996, the ALJ issued his ID (Order No. 34) granting Quickturn's motion for temporary relief. On July 18, 1996, respondents and the IA filed written comments on the temporary relief ID, as provided for in rule 210.66(c). Complainant and the IA filed replies to respondents' comments, and respondents filed a reply to the IA's comments on July 22, 1996, as provided for in rule 210.66(e). On August 5, 1996 the Commission determined to adopt the presiding ALJ's ID.

II. REMEDY

If there is reason to believe that a violation of section 337 has occurred (and the public interest factors discussed below do not prohibit a remedy), the Commission has broad discretion in selecting the form, scope, and extent of the remedy.[3] Under subsections 337(e)

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[2] 61 Fed. Reg. 9486 (March 8, 1996).

[3] *Hyundai Electronics Industries Col, Ltd. v. United States International Trade Commission*, 899 F.2d 1204 (Fed. Cir. 1990) (affirming Commission remedy determination in *Certain Erasable Programmable Read-Only Memories, Components Thereof, Products Containing Such Memories, and Processes for Making Such Memories*, Inv. No. 337-TA-276, USITC Pub. 2196 (continued...)

and (f), the Commission may issue a temporary exclusion order, a cease and desist order, or both, depending on the circumstances of each investigation.[4] The Commission may issue either a temporary general exclusion order, which covers goods irrespective of source, or a temporary limited exclusion order, which covers goods from only certain foreign sources.[5]

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[3] (...continued)
(May 1989)); *Viscofan, S.A. v. United States International Trade Commission*, 787 F.2d 544, 548 (Fed. Cir. 1986) (affirming Commission remedy determination in *Certain Processes for the Manufacture of Skinless Sausage Casings and Resulting Products*, Inv. Nos. 337-TA-148 and 169, USITC Pub. 1624 (December 1984)). However, as the Commission stated in *Certain Devices for Connecting Computers Via Telephone Lines*, although the Commission's remedial authority is quite broad, it has applied this authority "in measured fashion and has issued only such relief as is adequate to redress the harm caused by the prohibited imports." Inv. No. 337-TA-360, Commission Opinion (Dec. 12, 1994) at 9.

[4] Section 337(e)(1), 19 U.S.C. § 1337(e)(1), provides in relevant part:

> If, during the course of an investigation under this section, the Commission determines that there is reason to believe that there is a violation of this section, it may direct that the articles concerned, imported by any person with respect to whom there is reason to believe that such person is violating this section, be excluded from entry into the United States. . . .

Section 337(f)(1) provides:

> In addition to, or in lieu of, taking action under subsection (d) . . . of this section, the Commission may issue and cause to be served on any person believed to be violating this section . . . an order directing such person to cease and desist from engaging in the unfair methods or acts involved [unless precluded by consideration of enumerated public interest factors.]

[5] 19 U.S.C. §1337(d)(2)(effective January 1, 1995); *see also* 19 C.F.R. §210.50(c) (incorporating the statutory standard into the Commission's Rules of Practice and Procedure). Under this provision, the Commission can issue a general exclusion order only where it is "necessary to prevent circumvention of an exclusion order limited to products of named persons; or there is a pattern of violation of this section and it is difficult to identify the source of infringing products." This limitation on the Commission's authority to issue general exclusion orders appears in the section of the statute pertaining to permanent exclusion orders, section 337(d), rather than in the section that grants the Commission authority to issue temporary relief, section 337(e). Nevertheless, notwithstanding the placement of this provision in the statute, we believe that it was intended to apply equally to permanent and temporary general exclusion orders. The legislative history of the Uruguay Round Agreements Act (URAA) amendments to section 337 indicates that the new statutory limitations "do not differ significantly" from the Commission's
(continued...)

The Commission traditionally has issued cease and desist orders when commercially significant inventories of infringing goods are present in the United States.[6]

Commission rule 210.67(a) authorizes, but does not require, the ALJ to address the appropriate remedy and the public interest.[7] In this investigation, the ALJ concurred with the IA's positions regarding the appropriate remedy, which are discussed below.

Complainant Quickturn argued that issuance of an exclusion order is appropriate to prevent infringing imports and is the customary remedy where temporary relief is granted. Quickturn seeks such an order only with respect to respondents in this matter (*i.e.*, a limited exclusion order), acknowledging that there is no basis for issuance of a general exclusion order at this stage of the investigation. With respect to a cease and desist order, complainant argued that it has provided ample evidence that respondents are engaged in significant sales and solicitation activities in the United States and that any further solicitation and marketing

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(...continued)
traditional framework for analyzing the appropriateness of a general exclusion order, which was applied in the same manner to both temporary and permanent relief. See S. Rep. No. 412, 103rd Cong., 2d Sess. 120 (1994); H.R. Rep. No. 826, 103rd Cong., 2d Sess., pt. 1, at 141 (1994).

[6] *See, e.g., Pressure Transmitters*, Inv. No. 337-TA-304, USITC Pub. 2392 (June 1991); *Certain Strip Lights*, Inv. No. 337-TA-287 (October 3, 1989) (Unpublished opinion); *Certain Nonwoven Gas Filter Elements*, Inv. No. 337-TA-275, USITC Pub. 2129 (September 1988); *Certain Compound Action Metal Cutting Snips*, Inv. No. 337-TA-197, USITC Pub. 1831 (March 1986); *Certain High Intensity Retroreflective Sheeting*, Inv. No. 337-TA-268, USITC Pub. 2121 (September 1988); *Certain Erasable Programmable Read Only Memories*, Inv. No. 337-TA-276, USITC Pub. 2196 (May 1989)(while the existence of significant inventories was not conclusively proven, it could be reasonably assumed from the record that such inventories were present); *Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293 (March 1990).

The Commission's purpose in issuing cease and desist orders in patent-based cases has been to afford complete relief to complainants where infringing goods are already present in the United States, and thus cannot be reached by issuance of an exclusion order. *See, e.g., Certain Compound Action Metal Cutting Snips*, Inv. No. 337-TA-197, Commission Opinion at 5-7. Unlike an exclusion order, which is enforced by the U.S. Customs Service, a cease and desist order is an *in personam* order typically directed to a party in the United States and is enforced by the Commission, not Customs. The Commission has *in personam* jurisdiction over respondent Mentor, a company doing business at 8005 S.W. Boeckman Road, Wilsonville, Oregon, 97070, based on proper service of the complaint and notice of investigation and Mentor's full participation in this investigation.

[7] Any findings made by the ALJ may be superseded by Commission findings. 19 C.F.R. § 210.67(a).

activities by Mentor would constitute continued infringement of the patents in issue. Complainant also submitted a copy of a publication in which respondents indicated that, in the event temporary relief issues, they may "establish[] U.S.-based assembly" for the accused device.

Respondents argued that, if a temporary exclusion order issues, the order should exempt replacement parts and "components required to upgrade existing systems", as well as service and maintenance of existing systems in the United States. In support of this position, they state that if their U.S. customers (such as Bull Information Systems) are unable to obtain replacement parts or components needed to upgrade their systems, [ ].[8] For the same reasons, they state that any exclusion order should ensure that respondents may continue to service and maintain existing systems in the U.S.

Respondents also argued that there is no basis for a temporary cease and desist order because [ ]. In particular, respondents submitted a statement from a Mentor employee stating that [ ]. In addition, respondents argued that, to the extent that they are permitted to import under bond during the temporary relief period, a cease and desist order preventing general sales and marketing activities would be outside the Commission's statutory jurisdiction.

In the IA's view, the appropriate relief is a limited exclusion order directed to respondents' emulation systems, and components thereof, that the Commission has reason to believe infringe the asserted claims of the patents at issue. The IA noted that there are [, that are dependent upon the operation of those emulators. On that basis, the IA recommended that the temporary exclusion order include an exception for importation of emulator components that respondents certify are required for repair of emulators already installed in the United States.

The IA also believes that a cease and desist order prohibiting sales (except under bond) of Meta emulators present in the United States as of the date of entry of the order is appropriate. According to the IA, as of the date of the temporary relief proceedings, [ ]. The IA further stated that [

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[8] Comments on remedy submitted to the Commission by intervenor Bull HN Information Systems [ ].

] and that therefore [ ] is likely to irreparably harm Quickturn. Accordingly, the IA recommended that a cease and desist order prohibiting the sale or other transfer (except under bond) of Meta emulators held by the respondents within the United States at the date of issuance is appropriate in this investigation. The IA submitted, however, that any such cease and desist order should be narrowly tailored to prohibit only sales and similar transfers except under bond, rather than the broad array of commercial activities Quickturn seeks to prohibit. Specifically, the IA recommended that any cease and desist order should not prohibit respondents' marketing, sales, and support activities that are directed to goods imported or sold under bond. Finally, for the reasons discussed above in connection with the irreparable harm analysis, the IA does not believe that the public interest would be harmed by issuance of the proposed exclusion and cease and desist orders.

We agree with the ALJ's and the IA's recommendation and accordingly have issued a temporary limited exclusion order covering the accused hardware logic emulators, in assembled or unassembled form, that we have found likely to infringe claim 8 of the '473 patent and/or claims 1, 2, 3, or 15 of the '496 patent. We also agree that the temporary limited exclusion order should not extend to components, such as logic boards, certified to be imported to replace and repair inoperative components on [ ] Meta units present in the United States [ ].[9] Such an exception would prevent disruption to the business operations of Mentor's customers during the pendency of this investigation, and grant them time to prepare for the possibility of a permanent exclusion order, which probably would not include such an exception.

We agree as well with the ALJ and the IA regarding the appropriateness of issuing a temporary cease and desist order. Thus, we have determined to issue a cease and desist order prohibiting domestic respondent Mentor from importing, selling, distributing, offering for sale, or otherwise transferring in the United States (except under bond) hardware logic emulators covered by the patent claims at issue.[10] We believe that the presence of even one of the Meta units (at an estimated value of [ ] in the United States would constitute "commercially significant inventory," which the Commission traditionally has found

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[9] The temporary limited exclusion order makes it clear that it extends to the importation of subassemblies, other than those required as a one-for-one replacement of their counterparts in existing systems.

[10] As noted below, however, under the cease and desist order Mentor is permitted to conduct activities directly related to the sale of accused devices imported under bond during the period in which temporary relief would be effective. Mentor also is permitted to furnish services to its customers that are directly related to the accused devices it imported and sold in the United States prior to the effective date of the cease and desist order, including the installation of replacement logic boards.

warrants the issuance of a cease and desist order.

While respondents have represented that [

]. In addition, they have actively opposed the issuance of a cease and desist order. In these circumstances, and because the Commission's purpose in issuing cease and desist orders has been to afford complete relief to complainants where infringing goods are already present in the United States, we believe it appropriate in this case to issue such an order.[11]

We also agree with the IA that such an order should not extend to respondents' marketing and promotional activities in the United States. Unlike a permanent exclusion order, a temporary "exclusion order" actually must permit importations under bond. Accordingly, because respondents are statutorily entitled to import under bond goods that are subject to a temporary exclusion order, the incidental right to market those devices should not be prohibited by the temporary cease and desist order. For the same reasons that we believe the temporary exclusion order should not extend to replacement components, such as logic board assemblies, we also believe that any cease and desist order issued should not cover respondents' activities in connection with servicing its customers' imported Meta emulators, including the installation of such replacement components.

III. THE PUBLIC INTEREST

Before granting relief, the Commission must consider the effect that such relief would have on "the public health and welfare, competitive conditions in the United States economy, the production of like or directly competitive articles in the United States, and United States consumers."[12] The legislative history of this provision indicates that the Commission should

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[11] Moreover, we note that if, as respondents have represented, [
] respondents will not be harmed by the issuance of a cease and desist order.

[12] 19 U.S.C. §§ 1337(d) and (f). *See also Rosemount v. United States Int'l Trade Comm'n*, 15 U.S.P.Q.2d at 1572, 910 F.2d 819 (Fed. Cir. 1990)*("Rosemount")*. In *Rosemount*, the Federal Circuit, in affirming the *Pressure Transmitters* decision, stated:

> We also agree with the Commission's rejection of the view that the public interest inevitably lies on the side of the patent owner because of the public interest in protecting patent rights . . . other public interest factors are delineated in the above-quoted section 1337(e)(1) and must

(continued...)

decline to issue relief when the adverse effect on the public interest would be greater than the interest in protecting the patent holder.[13]

The ALJ found that: (1) Quickturn is capable of supplying the hardware logic emulation requirements of domestic users; (2) there is no significant likelihood that temporary relief would substantially impact the industries that purchase hardware logic emulation systems (*i.e.*, the U.S. semiconductor industry); (3) it is in the public interest to issue temporary relief to protect a domestic industry's valid and exclusive rights in its intellectual property; and (4) the statute provides, that in the event of the grant of temporary relief, respondents will be permitted to import the devices under bond and therefore the domestic industry, if it wants to, will have access to the Meta emulators. Based on these findings, the ALJ concluded that the public interest favors the granting of temporary relief.

Complainant and the IA both submit that entry of temporary relief in the form of a limited exclusion order directed to infringing hardware logic emulators and a cease and desist order directed to Mentor would not raise any public interest concerns under 19 U.S.C. §§ 1337(e) or (f). They note that there is no evidence that the U.S. demand for such products could not be supplied by complainant. They also argued that the U.S. semiconductor industry would not be harmed by the issuance of such temporary relief, principally because only a small portion of that industry uses hardware logic emulation.

Respondents argue that the public's interest would be furthered by ensuring that the technically superior Meta device will continue to be available to the U.S. semiconductor industry during the period of temporary relief. In particular, they argue that the Meta emulator's shorter "compile times" allow much greater flexibility and functionality in the design process and provide a significant technological advantage over Quickturn's emulators. Therefore, according to respondents, even if Quickturn could satisfy the current U.S. demand for traditional emulation products, granting temporary relief would "force the U.S. chip industry to use Quickturn's outdated off-the-shelf chip technology, while Meta's innovative custom-chip technology is freely available to our foreign competitors in Europe and Asia."

Based on the evidence of record, we agree that the issuance of a limited exclusion order and a cease and desist order to Mentor would not have an adverse effect on the public interest. First, as the ALJ noted, the public interest favors the protection of U.S. intellectual property

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[12] (...continued)
be taken into account.

Rosemount, 910 F.2d at 822, 15 U.S.P.Q.2d at 1572.

[13] *See* S. Rep. 1298, 93rd Cong., 2d Sess. 197 (1974).

rights.[14] Second, only a relatively small percentage of the 60 billion dollar U.S. semiconductor industry uses hardware emulation, due to the high cost of emulators. The evidence indicates that complainant can supply this demand for hardware logic emulators in the U.S. market. Even more to the point, respondents have indicated that they expect to supply [ ] units to the U.S. market in 1996.[15] We do not believe that the U.S. semiconductor industry would be significantly adversely affected if either Quickturn supplied [ ] emulators or these purchases were delayed pending the outcome of the permanent relief phase of this investigation. Indeed, these purchases need not be delayed to the extent that respondents' products could enter the United States upon the posting of a bond even under a grant of temporary relief.

Finally, hardware logic emulators are not the type of product that has in the past raised public interest concerns (such as, for example, drugs or medical devices) and we are not aware of any other public interest concern that would militate against entry of the remedial orders we have determined to issue. Accordingly, we conclude that the statutory public interest factors do not preclude issuance of relief in this investigation.

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[14] *See Rosemount*, 15 U.S.P.Q.2d at 1572 (Fed. Cir. 1990)(patent protection is a dominant factor in determining the public's interest in granting relief). In this regard, we also note that the Commission has declined to grant relief on public interest grounds in only three cases in 20 years. In *Certain Automatic Crankpin Grinders*, Inv. No. 337-TA-60, U.S.P.Q. 71 (ITC 1979), the Commission denied relief because of an overriding national policy interest in maintaining and increasing the supply of fuel efficient automobiles, coupled with the domestic industry's inability to supply domestic demand. In *Certain Inclined Field Acceleration Tubes*, Inv. No. 337-TA-67, USITC Pub. 1119 (1980), the Commission denied relief because there was an overriding public interest in continuing basic atomic research using the imported acceleration tubes, which were of a higher quality than the domestic product. Finally, in *Certain Fluidized Supporting Apparatus*, Inv. No. 337-TA-182/188, USITC Pub. No. 1667 (1984), the Commission denied relief because the domestic producer could not supply demand for hospital beds for burn patients within a commercially reasonable time, and no therapeutically comparable substitute for care of burn patients was available.

[15] Thus, while [ ] units could have a substantial effect on Quickturn, they are far less significant to the approximately $60 billion U.S. semiconductor industry.

IV. COMPLAINANT'S BOND[16] [17]

Section 337(e)(2) gives the Commission the authority to require a complainant to post a bond as a prerequisite to the granting of temporary relief.[18] Commission rule 210.52(c) provides as follows:

> In determining whether to require a bond as a prerequisite to the issuance of temporary relief, the Commission will be guided by Rule 65 of the Federal Rules of Civil Procedure.[19]

The ALJ found, based on the record developed in the temporary relief phase of the investigation, that complainant has made a showing of a strong likelihood of success on all of the issues affecting the merits of the case. In particular, complainant's strong showing with respect to validity and infringement of the claims in issue, the fact that Mentor and Meta had a reasonable opportunity to consider the claims in issue prior to importing the accused goods into the United States, and Mentor's resolve to enter the U.S. hardware logic emulator market, persuaded the ALJ that no bond should be required of Quickturn, and he so recommended.

Complainant argued that its strong likelihood of success on the merits and its financial condition justify waiver of a bond. Alternatively, complainant argued that if the Commission should determine that a bond is required, it should be no greater than $250,000 because (a) the potential harm, if any, to respondents is minimal, (b) the speculative nature of respondents' potential damages, if any, weighs against a large bond, and (c) any temporary relief will be required for only a relatively limited time period, viz., until March 13, 1997.

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[16] Commissioner Newquist does not join the following discussion regarding complainant's bond. He would not require complainant to post a bond.

[17] Commissioner Crawford does not join the Commission's opinion respecting complainant's bond. Instead, she would have accepted the ALJ's recommendation on this issue.

[18] Section 337(e)(2) provides that, when a complainant has been granted temporary relief, "[t]he Commission may require the complainant to post a bond as a prerequisite to issuance of a [temporary relief] order under this subsection."

[19] 19 C.F.R. § 210.52(c). Rule 65(c) of the Federal Rules of Civil Procedure states in pertinent part that:

> No restraining order or preliminary injunction shall issue except upon the giving of security by the applicant, in such sum as the court deems proper, for the payment of such costs and damages as may be incurred or suffered by any party who is found to have been wrongfully enjoined or restrained.

Respondents reiterated their position that complainant has not made a strong showing of likelihood of success. They also argued that Quickturn, with over $80 million in sales and $40 million in cash reserves, is not indigent and that Mentor and Meta will be significantly harmed if temporary relief issues. Hence, they argued that a "substantial" complainant's bond is appropriate.

The IA argued that the purpose of requiring a complainant to post a temporary relief bond is to deter frivolous motions on temporary relief and the use of such motions to harass respondents. In this case, however, he notes that the evidence of validity and infringement is strong. Accordingly, the IA argued for a relatively small complainant's bond in an amount equal to [

], which he estimated to be roughly $200,000.

We note that, in adopting the ALJ's ID on temporary relief, we have found that complainant has made a strong showing of likelihood of success on the merits of this investigation. We also adopted the ALJ's finding that complainant has demonstrated that it is threatened with irreparable harm in the event temporary relief does not issue. Nevertheless, there exists the possibility that our construction of the claims of the patents in issue and/or our infringement determination in this investigation may ultimately change.[20] Since the purpose of the bond requirement is to protect the enjoined party from costs and damages resulting from a wrongful injunction while fixing the movant's liability for such an order,[21] we believe a relatively small bond should be required of complainant. In this regard, we agree with the IA and have set complainant's bond at $200,000, [

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V. RESPONDENTS' BOND[22]

As noted above, pursuant to section 337(e)(1), articles subject to a temporary exclusion order are entitled to entry into the United States under a bond paid by respondents in an amount determined by the Commission.[23] Specifically, section 337(e)(1) also provides that during the pendency of the investigation, the excluded articles "shall be entitled to entry under

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[20] *New England Braiding Co. Inc. v. A.W. Chesterton Co.*, 23 U.S.P.Q.2d 1622, 1626 (Fed. Cir. 1992). *See* ID at 75, note 40.

[21] *See Continuum Co. Inc. v. Incepts, Inc.*, 873 F.2d 801, 803 (5th Cir. 1989).

[22] Commissioner Crawford does not join the Commission's opinion respecting respondents' bond. Instead, she would have accepted the ALJ's recommendation on this issue.

[23] 19 U.S.C. §1337(e)(1).

bond prescribed by the Secretary [of the Treasury] in an amount determined by the Commission to be sufficient to protect the complainant from any injury."[24]

The ALJ found that there is an indication that respondents will be active in the U.S. emulation market during the period for which temporary relief would be in effect. He also found that when there was no competing product, Quickturn would [ ] of approximately [ ], but that the [ ] to [ ] when Quickturn competed with the Meta device. He therefore concluded that, based on the difference between these two [ ] levels, respondents should be subject to a bond of 25 percent of the entered value of each Meta emulator imported during the temporary relief period.

Complainant argued that respondents bond should be set at a minimum of 100 percent of the sales price of any emulation products imported or sold, or services provided, by respondents during the pendency of the temporary relief. According to complainant, the Commission should use complainant's gross profit as the appropriate measure to offset any injury during the temporary relief period. Gross profit is appropriate, they argue, because it takes account of the fact that, if Quickturn does not make a sale, it does not incur the variable costs of production, but does incur fixed costs like overhead, sales and administrative expenses. In addition, to account for this lost sales revenue, Quickturn argues that some amount should be added to the bond to account for price erosion and the other aspects of the irreparable harm to Quickturn that would result from respondents' sales of infringing devices.

The IA argued that complainant has not provided sufficient justification for the proposed 100 percent bond. Instead, the IA noted that, although the evidence does not lend itself to a ready quantification of the amount of bond that would compensate complainant for the harm to it, there is at least evidence as to an amount that would tend to counteract any price erosion caused by respondents. Accordingly, the IA proposed that the bond should be set in an amount equal to the difference between the [ ] in the absence of emulation competition [ ] and the [ ] Quickturn offers when faced with competition from Mentor and Meta [ ]. Thus, the IA argued that respondents should be subjected to a bond of 30 percent of the entered value of each Meta emulator imported during the temporary relief period.

We disagree with the ALJ's recommendation that 25 percent is an appropriate bond rate for respondents. The ALJ based this recommendation essentially on the extent of price erosion

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[24] *Id.* This bonding standard for temporary relief investigations is new and became part of section 337 through the URAA amendments to the statute. Previously, the Commission set a respondent's bond by taking into account, among other things, the amount that would offset any competitive advantage to the respondent resulting from the respondent's alleged unfair method of competition or unfair acts in the importation or sale of the articles in question. *See* 19 C.F.R. §210.50(a)(3).

that respondents caused Quickturn to endure in the U.S. market.[25] The method used by the ALJ (and supported by the IA) -- setting the bond amount based on evidence of price suppression -- is the approach traditionally taken by the Commission in setting bond for the Presidential review period in permanent section 337 investigations. We do not believe, however, that, in the context of the temporary relief phase of this investigation, this approach satisfies the new statutory requirement that the amount of the bond be "sufficient to protect the complainant from any injury."[26] As the ALJ found, Quickturn's potential harm from the sale of respondents' accused devices goes well beyond this price erosion. We believe that this new statutory requirement directs that respondents' bond should more closely approximate this potential harm to Quickturn.

Although such an analysis is, by its very nature, difficult to quantify, it is reasonable to conclude that the potential harm to Quickturn is greater than the extent of the price erosion alone. As complainant points out, it loses all the revenues it would have garnered from each sale, not just the amount represented by the price erosion. The principal harm to Quickturn from that lost revenue is the long-term impact on Quickturn's research and development efforts. As noted above, Quickturn is a relatively small, single product company competing in the rapidly evolving hardware logic emulation market. As such, even a single lost sale to an accused device could have a significant and long-term negative impact on Quickturn's ability to compete.

In these circumstances, while any bond amount cannot capture precisely the full extent of any such long-term impact on Quickturn from sales of the accused devices, there is evidence that Quickturn allocates approximately 18 percent of gross revenues to research and development. Accordingly, we have set respondents' bond at 43 percent of the entered value of the Meta devices, reflecting 25 percent for the price erosion that the sale of an infringing Meta device causes and an additional 18 percent to compensate Quickturn for the impact of such sales on its research and development budget.

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[25] This figure is supported by evidence presented at trial. In the one case of head-to-head competition in the U.S. between Quickturn and Mentor, Mentor's final quote was $[ ], compared to Quickturn's final quote of $[ ]. Quickturn's initial quote on this sale was its list price of $[ ]. Consequently, for this sale Quickturn [ ] list price.

[26] *See, e.g., Certain Nonwoven Gas Filter Elements*, 11 ITRD 1391, 1399 (1988).

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	)	
	)	
CERTAIN HARDWARE LOGIC EMULATION SYSTEMS AND COMPONENTS THEREOF	)	Investigation No. 337-TA-383
	)	
	)	

Order No. 34: Initial Determination[1]

Paul J. Luckern, Administrative Law Judge

Pursuant to the Notice of Investigation (61 Fed. Reg. 9486) (March 8, 1996), this is the administrative law judge's initial determination, under Commission rule 210.58, on complainant's Motion No. 383-1 for temporary relief. The administrative law judge determines, after a review of the record developed, that complainant is entitled to temporary relief. Accordingly, Motion No. 383-1 is granted.[2]

[1] The Commission's rules require that Order No. 34 be called an initial determination so that it can be reviewed by the Commission even if no petition for review is filed. This is not the final decision of the administrative law judge in this investigation.

[2] Also issued on July 8, 1996 are (1) Order No. 32 granting complainant's Motion No. 383-38 re errata, denying respondents' Motion No. 383-39 to terminate and denying respondents' Motion No. 383-44 for sanctions, (2) Order No. 33 denying respondents' Motion No. 383-46 to strike and (3) Order No. 35 ordering parties to submit proposed procedural schedules for the permanent relief phase of the investigation.

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ABBREVIATIONS

CBr	Complainant's Post Hearing Brief
CDX	Complainant's Demonstrative Exhibit
CFF	Complainant's Proposed Finding of Fact
CRBr	Complainant's Reply Brief
CRFF	Complainant's Rebuttal Finding of Fact
CX	Complainant's Exhibit
FF	Finding of Fact
RBr	Respondents' Post Hearing Brief
RFF	Respondents' Proposed Finding of Fact
RO	Respondents' Objections to Complainant's Finding of Fact
RRBr	Respondents Reply Brief
RRFF	Respondents' Rebuttal Finding of Fact
RX	Respondents' Exhibit
Tr	Transcript of hearing
SBr	Staff's Post Hearing Brief
SFF	Staff's Proposed Finding of Fact
SRBr	Staff's Reply Brief
SRFF	Staff's Rebuttal Finding of Fact

I. Procedural History

On March 4, 1996, a complaint and Motion No. 383-1 for temporary relief were filed under section 337 on behalf of complainant Quickturn Design Systems of California (Quickturn). Respondents, identified in the Commission's notice of investigation, are Mentor Graphics Corp. of Oregon (Mentor) and Meta Systems of France (Meta).

Complainant's Motion No. 383-1 for temporary relief requested that the Commission issue a temporary exclusion and temporary cease and desist orders prohibiting the importation into, and the sale within, the United States after importation of certain hardware logic emulation systems and components that infringe claim 8 of U.S. Letters Patent 5,036,473 (the '473 patent) or claims 1, 2, 3, or 15 of U.S. Letters Patent 5,448,496 (the '496 patent) during the course of the Commission's investigation. Complainant's Motion No. 383-1 was provisionally accepted by the Commission pursuant to Commission rule 210.58.

Order No. 14, which issued on April 4, 1996, made the temporary relief phase of the investigation more complicated, pursuant to Commission rule 210.60, and set the prehearing conference and hearing for commencement on April 22. The hearing continued on April 24, 25, 26, 27, 28, 29, 30, May 1, 2, 3 and concluded on May 4 at which time the evidentiary record for the temporary relief phase was closed. Post hearing submissions have been filed. Also, closing arguments were held on June 5.

Respondents[3], at the hearing, were provided the opportunity to file subsequent to the hearing a motion to strike certain evidence, which Motion No. 383-46 was filed. In addition

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[3] The word "respondents," as used in this initial determination, refers to Mentor and Meta only.

on April 24,1996 complainant filed "Errata Re Correction Of Typographical Error In Complainant Quickturn's Motion For Temporary Relief Under 19 U.S.C. Section 1337(e) And (f) And Memorandum In Support Thereof; And In Complainant Quickturn's Prehearing Statement" and on April 25 complainant filed an "Errata Re Correction Of Typographical Error In The Complaint Of Quickturn Design Systems, Inc. Pursuant to 19 U.S.C. §1337," to the effect that paragraph 63 of the complaint should be changed. At the hearing the administrative law judge stated that he was treating the filing of the two errata as Motion No. 383-38. Respondents also have filed Motion No. 383-39 to terminate the temporary relief phase of this investigation with respect to claim 8 of the '473 patent and Motion No. 383-40 for sanctions for abuse of process.[4]

Order No. 29, which issued on April 26, 1996, denied the motion of Bull HN Information Systems, Inc. (Bull) of Billerica, Mass. to intervene, without prejudice to Bull moving to intervene in the permanent phase of this investigation. Order No. 30, which issued on May 14, 1996 was an initial determination granting Bull's motion to intervene in the permanent phase of the investigation. The Commission, on June 12, 1996, issued a notice of its determination not to review Order No. 30.

The matter is now ready for a decision.

This initial determination on complainant's Motion No. 383-1 is based on the record compiled at the hearing and the exhibits admitted into evidence. The administrative law judge has also taken into account his observation of the witnesses who appeared before him

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[4] Order No. 33, which issued on July 8,1996 denied respondents' Motion No. 383-46 to strike. Order No. 32, which issued also on July 8, granted complainant's Motion No. 383-38 re errata, denied respondents' Motion No. 383- 39 to terminate and denied respondents' Motion No. 383-44 for sanctions.

during the hearing. Proposed findings submitted by the parties not herein adopted, in the form submitted or in substance, are rejected as either not supported by the evidence or as involving immaterial matter and/or as irrelevant. The findings of fact which form a portion of this initial determination include references to supporting evidence in the record. Such references are intended to serve as guides to the testimony and exhibits supporting the findings of fact. They do not necessarily represent complete summaries of the evidence supporting said findings.

II. Parties

See FF 1 to 8 for identification of the private parties.

III. Importation

See FF 9 to 11 for importation by the private parties.

IV. Jurisdiction

The complaint does state a cause of action under section 337 of the Tariff Act of 1930, as amended. Thus, the Commission has jurisdiction over the subject matter of this investigation. Each of Mentor and Meta responded to the complaint and participated in the investigation thereby submitting to the personal jurisdiction of the Commission. The Commission has in rem jurisdiction over the products at issue by virtue of the respondents' admissions that Meta's accused products have been imported into the United States. See Certain Circuit Board Testers, Inv. No. 337-TA-342, USITC Pub. 2622, Opinion of the Commission, at 2, n. 2 (1993) (Circuit Board).

V. Products in Issue

The products at issue are hardware logic emulation systems which consist of reconfigurable logic devices and interconnect resources that are programmed primarily via software to emulate an integrated circuit design, resulting in substantial savings of time and money during the design of integrated circuits. Hardware logic emulators are particularly useful in verifying designs for application-specific integrated circuits (ASICs), custom chips and multi-chip systems (FF 12, 13).

VI. Requirements For The Issuance of Temporary Relief

The Commission can temporarily exclude articles under investigation if, during the course of the investigation, the Commission determines that "there is reason to believe that there is a violation" of the statue, unless after considering certain enumerated public interest factors, it finds that the articles should not be excluded. 19 U.S.C. § 1337(e)(1). Temporary relief is only granted when there is a threat of irreparable harm to the domestic industry. Certain Electrical Connectors and Products Containing Same, Order No. 25, Unreviewed Initial Determination on Temporary Relief at 89 (September 8, 1995) (Electrical Connectors). The "irreparable harm" is harm likely to occur before the Commission is able to issue permanent relief, which in this investigation is the harm likely to occur from August 5, 1996 to March 10, 1997.

The temporary relief can be in the form of a temporary cease and desist order in addition to, or in lieu of, a temporary exclusion order, provided that the issuance of the cease and desist order is consistent with the public interest factors. See Section 337(f)(1), as amended by the Omnibus Trade and Competitiveness Act of 1988, Pub.L. 100-418 (1988 Trade Act), 19 U.S.C. § 1337(f)(1).

Any temporary relief is granted by the Commission "to the same extent as preliminary injunctions . . . may be granted under the Federal Rules of Civil Procedure." 19 U.S.C. § 1337(e)(3), and Commission rule 210.52. Under 35 U.S.C. § 283, a district court may grant a preliminary injunction whenever, according to the principles of equity, such injunction is necessary to prevent the violation of any right secured by a patent. We Care, Inc. v. Ultra-Mark International Corp., 930 F.2d 1567, 1570 (Fed. Cir. 1991) (We Care). Consistent with We Care, to be entitled to temporary relief in a section 337 investigation complainant must establish a right thereto in light of the following four factors:

1. A reasonable likelihood of success on the merits;[5]
2. Irreparable harm to the domestic industry in issue in the absence of temporary relief;
3. The balance of harm tipping in complainant's favor; and
4. A tolerable effect on the public interest.

See Sofamor Danek Group Inc. v. Depuy Motech Inc., 74 F.3d 1216, 37 USPQ2d 1529, 1531 (Fed. Cir. 1996) (Sofamor). No one factor taken individually is necessarily dispositive. Chrysler Motors Corp. v. Auto Body Panels, Inc., 908 F.2d 951, 953 (Fed. Cir. 1990). Each factor must be weighed and measured against the other factors and against the form and magnitude of the relief requested. Hybritech Inc. v. Abbott Laboratories, 849 F.2d 1446, 1451, 7 USPQ2d 1191, 1195 (Fed. Cir. 1988) (Hybritech Inc.). Temporary relief is "not to

[5] See Roper Corp. v. Litton Systems, Inc., 757 F.2d 1266, 1271, 225 USPQ 345, 348 (Fed. Cir. 1985) and T.J. Smith and Nephew Limited v. Consolidated Medical Equipment, 821 F.2d 646, 647, 3 USPQ2d 1316, 1317 (Fed. Cir. 1987), which shows that the movant's probability of success must rise to the level of a reasonable likelihood of success.

be routinely granted" Intel Corp. v. ULSI Systems Technology, Inc. 955 F.2d 1566, 1568, 27 USPQ2d 1136, 1138 (Fed. Cir. 1993), cert. denied 1145 Ct. 923 (1994).

As this administrative law judge stated in Certain Recombinantly Produced Human Growth Hormones, Inv. No. 337-TA-358, USITC Pub. 2764, Unreviewed Initial Determination on Temporary Relief at 81 to 93 (January 26, 1994) (Growth Hormones) and Electrical Connectors at 95, irreparable harm is consistently measured by the aggregate effect of the alleged unfair acts. Such measurement is consistent with the determination of whether there is a "[t]hreat of irreparable harm [irrespective of the source] to the domestic industry in the absence of the requested relief," Circuit Board, Commission Opinion at 4. Accordingly, the administrative law judge, in determining the appropriateness of temporary relief, is measuring any irreparable harm by the aggregate effect of respondents' alleged unfair acts, in the absence of the requested relief, as well as considering the balance of harms between the parties and the effect, if any, the requested relief would have on the public interest.

An administrative law judge's decision to issue temporary relief is discretionary. New England Braiding Co. v. A.W. Chesterton Co., 970 F.2d 878, 882, 23 USPQ2d 1622, 1625, 1626 (Fed. Cir. 1991) (Braiding). Entitlement to temporary relief is determined in the context of the presumption and burdens that would adhere at the hearing on the merits. Braiding 970 F.2d at 880, 881, 23 USPQ2d at 1625, 1626. Where a patent is involved, the statutory presumption of validity, viz. 35 U.S.C. § 281, "is not evidence which can be 'weighed' in determining likelihood of success." Thus the statutory presumption of validity does not relieve a patentee, who moves for temporary relief, from carrying the normal burden of demonstrating that it will reasonably likely to succeed, even when the issue

concerns the patent's validity. Id. Although it is not the patentee's burden to prove validity, on a motion for temporary relief the patentee must show that the alleged infringer's defense lacks substantial merit. A patentee can fail to make a sufficient showing of likelihood of success required to support a temporary exclusion order when the evidence presented in support of invalidity of the patent in issue raises a substantial question, even though that defense may not be entirely fleshed out. Id. A prior adjudication is not an absolute requirement for the grant of temporary relief. See Atlas Powder Co. v. Ireco Chemicals, 773 F.2d 1230, 227 USPQ 289 (Fed. Cir. 1985) (Atlas Powder).

When there is a "clear showing" of likelihood of success on patent infringement and validity there is a presumption of irreparable harm. Sofamor 74 F.3d 1219, 39 USPQ2d at 1533. An entitlement to a presumption of irreparable harm is not, in itself, necessarily dispositive of the irreparable harm question because a presumption of irreparable harm to a patentee, like all presumptions is rebuttable. Illinois Tool Works, Inc. v. Grip-Pak, Inc., 906 F.2d 679, 681-82, 15 USPQ2d 1307-09 (Fed. Cir. 1990).

In a temporary relief proceeding, on appellate review, the Federal Circuit Court of Appeals (CAFC) must determine whether in granting or denying temporary relief, the Commission abused its discretion Rosemount, Inv. v. International Trade Commission, 910 F.2d 819, 821 (Fed. Cir. 1990). Under this standard the CAFC "may set aside the decision under review if it rests on the foundation of an erroneous understanding of the law or on clearly erroneous findings of fact." If no material, legal or factual error is discerned, the CAFC may set aside a decision committed to the discretion of the review tribunal only if it

committed a clear error of judgment, that is, its decision, based on the facts, is patently unreasonable, arbitrary, or fanciful," Id.

VII. Opinion

A. Complainant's Reasonable Likelihood of Success on the Merits

The first factor for entitlement of temporary relief is "a reasonable likelihood of success on the merits." Complainant has alleged that respondents infringe dependent claim 8 of the '473 patent and independent claim 1, dependent claim 2, dependent claim 3, and independent claim 15 of the '496 patent. Claim 8 of the '473 patent is dependent on claim 7 which is dependent on claim 6 which is dependent on claim 1. Each of claims 2 and 3 of the '496 patent is dependent on claim 1.

1. Assignor Estoppel and Privity

Complainant argued that respondents are estopped from contesting the validity or enforceability of the '473 and '496 patents by operation of assignor estoppel and the related doctrine of privity. It is argued that the equities strongly favor application of the doctrine of assignor estoppel to Mentor, and that Meta is in privity with Mentor for purposes of assignor estoppel. (CBr at 3-20). The staff argued that the doctrine of assignor estoppel will probably be found to preclude Mentor and Meta from asserting that the '496 and '473 patents are invalid (SBr at 35-38).

Respondents argued that assignor estoppel does not apply to respondents; that Bull's intervention obviates the assignor estoppel issue; that complainant purchased the '473 patent "AS IS" in light of Mentor's disclaimer of warranties regarding validity and enforceability; that Meta is not in privity with Mentor; that the equities favor allowing Mentor to challenge

the '473 and '496 patents because complainant and not respondents had knowledge of the '353 patent; and that Mentor should not be estopped because the '496 patent claims technology distinct from the technology Mentor assigned to complainant and that Quickturn's knowledge of the '353 patent, which Mentor did not have, at the time Mentor sold its patent holdings to complainant gave complainant superior knowledge of the "infirmities" of the patent holdings. (RBr 46-54).

Assignor estoppel is an equitable doctrine that prevents one who has assigned the rights to a patent (or patent application) from later contending that what was assigned is a nullity. Diamond Scientific Co. v. Ambico, Inc., 848 F.2d 1220, 6 USPQ2d 2028, 2030 (Fed. Cir. 1988), cert. dismissed, 487 U.S. 1265 (1988) (Diamond Scientific). The four most frequently mentioned justifications for applying assignor estoppel, enunciated by the Federal Circuit in Diamond Scientific 6 USPQ2d at 2030, 2031, are the following factors: (1) to prevent unfairness and injustice; (2) to prevent a party from benefiting from its own wrong; (3) by analogy to estoppel by deed in real estate; and (4) by analogy to a landlord-tenant relationship. Moreover the Federal Circuit has held that:

> it is the implicit representation by the assignor that the patent rights that he is assigning (presumably for value) are not worthless that sets the assignor apart from the rest of the world and can deprive him of the ability to challenge later the validity of the patent. Thus to allow the assignor to make that representation at the time of the assignment (to his advantage) and later repudiate it (again to his advantage) could work an injustice against the assignee.

Id. 6 USPQ2d at 2031.

The record in this investigation establishes that, through the execution of an Asset Purchase Agreement dated February 28, 1992, a sale was consummated by which Mentor transferred its entire hardware logic emulation business to complainant in exchange for

$200,000 and stock of complainant (FF 28). This transfer of rights included rights to the '473 patent and an assignment of several patent applications, including application Serial No. 07/698,734, which ultimately gave rise to the '496 patent (FF 29).[6] The assignment had the following representations:

> NOW, THEREFORE, be it known for good and valuable consideration, said Mentor . . . does hereby sell, assign, transfer and set over unto said Quickturn . . ., the entire right, title and interest in and to said inventions and said Patents, . . . , the same to be held and enjoyed by the said Quickturn . . . for its own use and benefit, . . . to the end of the term for which said Patents are or may be granted . . . as fully and entirely as the same would have been held and enjoyed by said Mentor . . . , if this assignment and sale had not been made; . . . [Emphasis added]

(FF 29). [7] At the time of assignment, each of respondents and complainant were aware of an application by Sample et. al., which resulted in the issuance of the '353 patent (FF 30).

In Diamond Scientific, the Federal Circuit held that, despite the public policy encouraging people to challenge potentially invalid patents, there are still circumstances in which the equities of the contractual relationships between the parties should deprive one party of the right to bring that challenge. Thus, the analysis of assignor must be concerned mainly with the balance of equities between the parties. Id. 6 USPQ2d at 2031.

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[6] The '496 patent issued from application Serial No. 270,234, filed on July 1, 1994, which was a continuation of application Serial No. 175,981, filed on December 30, 1993, which, in turn, was a continuation of application Serial No. 07/698,734 (FF 412).

[7] In O. G. Products, Inc. v. Shorty, Inc., 992 F.2d 1211 (Fed, Cir.) , cert. denied 114 S.Ct. 192 (1993), the Court held that the district court properly estopped one Shorty from contesting the validity of a '438 patent in issue. The Court stated that if the '438 patent claims an invention within the assignment agreement, the assignor estoppel doctrine operates to prevent Shorty from contesting the validity of the patent. It then concluded that there was not a material difference between what Shorty assigned and the '438 patent. The Court also found that the prosecution history showed that the '438 patent merely elaborated on the invention Shorty "reassigned" and concluded that the scope of Shorty's assignment was "at least as broad as the invention claimed in the '438 patent" Id., 992 F.2d at 1214, 1215.

In addition to acting as a bar to the original assignor, the doctrine of assignor estoppel operates to bar other parties in privity with the assignor. Diamond Scientific, 6 USPQ2d at 2030, 2031. What constitutes "privity" varies, depending on the purpose for which privity is asserted. Privity, like the doctrine of assignor estoppel itself, is determined upon a balance of equities. The closer the relationship is between the entities alleged to be in privity, the more the equities will favor applying the doctrine of collateral estoppel to both entities. Shamrock Technologies v. Medical Sterilization, 903 F.2d 789, 793 (Fed. Cir. 1990).[8]

Respondent Meta has been designing, manufacturing, and selling the accused hardware logic emulations systems (FF 54, 55). Mentor has engaged in promotional activities in the United States aimed at selling Meta emulation systems to its U.S. customers (FF 58). One emulation system manufactured by Meta has been imported into the United States by Bull in Phoenix, Arizona (FF 77 to 79).[9] Respondent Mentor has also imported a Meta hardware

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[8] In Intel Corp. v. U.S. Intern. Trade Comm'n, 946 F. 2d 821 (Fed, Cir. 1988), the Federal Circuit held that the Commission had correctly concluded that both statutory and case law required that assignor estoppel be considered and applied in section 337 cases. However on Intel's appeal that the Commission's decision that one GI/M was not estopped because it was not in privity with one George Perlegos, the Court held that the Commission erred in failing to apply the doctrine of assignor estoppel to GI/M and that in determining whether GI/M was in privity with Perlegos, all contacts between them, direct and indirect, must be considered. Id. 946 F.2d at 837, 838.

[9] On April 22, 1996, pursuant to Commission rule 210.19, Bull HN Information Systems, Inc. of Billerica, Mass. filed Motion No. 383-36 for leave to intervene in this investigation. In support of Motion No. 383-36 it was argued that complainant had indicated in its complaint that movant, one of the customers of respondents Meta and Mentor, was infringing complainants' patents. Hence, movant argued that it had an interest relating to the subject matter of this investigation because any grant of relief to complainant, which would exclude respondents' products and components thereof from importation into the United States, could severely prejudice the movant's interests and disrupt its business. See Order No. 29 which denied Motion No. 383-36 without prejudice to any motion by movant to intervene in the permanent phase of this investigation. On May 1, 1996 Bull HN Information Systems, Inc. filed Motion No. 383-40 for leave to intervene in the permanent phase of this investigation. Order No. 30, which issued on May 14, 1996, was an initial determination which granted Motion No. 383-40. On June 12, 1996 the Commission determined not to review Order No. 30.

logic emulation system into the United States and installed it at Mentor facilities in Oregon. The Meta emulation system is used to train Mentor personnel (FF 60). Significantly, Mentor has now acquired Meta (FF 71).

The administrative law judge rejects respondents' argument that the '496 patent claims technology distinct from the technology Mentor assigned to complainant. It is a matter of public record that the Patent Office leveled a double patenting rejection at the claims of the '496 patent which was removed by the filing of a terminal disclaimer (FF 32). Moreover, it has been found that the claims in issue of both the '473 and '496 patents are directed to the method and apparatus, respectively, involving the use of the partial crossbar construction in a hardware emulation system. See infra. Hence the administrative judge finds no basis for respondents' argument that the claimed technology in the '473 and '496 patents is distinct. The fact that, at the time of the assignment, the Patent Office had not yet granted the '496 patent in issue is irrelevant. Thus, what Mentor assigned were the rights to "inventions" in the '734 application (FF 28, 29), and the fact that Quickturn later amended the claims in the '734 application does not detract from the application of assignor estoppel. see Diamond Scientific, 6 USPQ2d at 2031.[10]

The administrative law judge rejects respondents' argument that Bull's intervention obviates the assignor estoppel issue. Pursuant to Order Nos. 29 and 30, Bull was permitted to intervene only for purposes of permanent relief proceedings. Allowing the fact that Bull

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[10] To the extent Quickturn may have broadened the claims in the assigned '734 patent application (after it was assigned) beyond what could be validly claimed in light of the prior art, respondents may be allowed to introduce evidence of prior art to narrow the scope of the claims of the patents. Id. 6 USPQ2d at 2032. As discussed in "Claim Construction ('496 patent)" section 2 b. infra, the administrative law judge has found that the prior art of record did not narrow the scope of any claim in the '496 patent.

will participate in the permanent phase of the investigation to determine an issue in the temporary relief phase would nullify Order No. 29 denying Bull's intervention in the temporary relief phase. Moreover, there has not been an opportunity to take discovery on Bull's ability or inability to raise assignor estoppel in the permanent relief phase of this investigation.[11]

The administrative law judge further finds that the warranty disclaimer provision of the February 1992 Asset Transfer Agreement (FF 28) has no relevance to the assignor estoppel issue. The language of the warranty disclaimer shows that the disclaimer protected Mentor against a claim by complainant if the patents complainant purchased from Mentor later turned out to be invalid if contested by a third party. This disclaimer does not say that Mentor would be permitted to turn around and contend that the patents it sold to complainant were worthless.

The administrative law judge also rejects respondents' argument assignor estoppel does not apply to the '353 patent due to Quickturn's superior knowledge of the '353 patent at the time the '473 patent was assigned. Almost two years before Mentor sold its patent holdings to complainant, Mentor's outside patent lawyer, by a letter dated July 31, 1990, advised Mentor's inside counsel of the publication of complainant's European patent application corresponding to the application which matured into the '353 patent (FF 30). Hence, Mentor was put in a position to pursue an inquiry regarding the '353 patent if it had elected to do so,

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[11] Based on the evidence of record, it would appear that Bull is in privity with Mentor. Bull was a Meta customer prior to the hearing (FF 77). Mentor admits that [ ](FF 81). Bull has [ ](FF 82, 83). In addition, [ ] (FF 78).

in later negotiations leading to the assignment of the '473 patent and the '734 application to complainant in March of 1992.

In view of the foregoing, the administrative law judge finds that complainant is likely to succeed in preventing each of respondents Mentor and Meta from contesting the validity or enforceability of the '473 and '496 patents by operation of assignor estoppel and the related doctrine of privity.

2. Claim Construction

Claims are construed in the same manner when determining both validity and infringement. W.L. Gore & Associates, Inc. v. Garlock, Inc., 842 F.2d 1275, 1279, 6 USPQ2d 1277, 1280 (Fed. Cir. 1988). The construction of the meaning of language in a claim should be made independent of what is being alleged to infringe the claim. See Donald S. Chisum, Patents § 18.03 (1994) (Chisum).

When analyzing the likelihood of success on the merits regarding patent infringement, the administrative law judge must first, construe disputed claim language as a matter of law, see Markman v. Westview Instruments, Inc., 52 F.3d 967, 978, 34 USPQ2d 1321, 1328 (Fed. Cir. 1995) (en banc) affirmed 116 S.Ct. 1384, ___ U.S. ___, (1996) (Markman)[12]. However, "Markman does not obligate the [administrative law judge] to conclusively interpret claims at an early stage in a case." Sofamor, 74 F.3d at 1219, 37 USPQ2d at 1532. The administrative law judge then makes a determination of whether the accused

[12] The CAFC also held that the interpretation of language of a claim to be the exclusive province of a court and the Seventh Amendment to be consistent with that conclusion. Writ by the Supreme Court was granted on that issue. Justice Souter, delivering the opinion for a unanimous Court, held that the construction of a patent, including terms of art within its claim 5, is exclusively within the province of a court. 116 S.Ct. at 1387-1396.

device is likely to fall within the scope of the asserted claims. H.H. Robertson, 820 F.2d at 389, 2 USPQ2d at 1929; see also Sofamor, 74 F.3d at 1218, 37 USPQ2d at 1531.

To ascertain the meaning of claims, the claims, as well as the specification and the prosecution history are considered. Claims must be read in view of the specification of which they are a part. The specification contains a written description of the invention that must enable one of ordinary skill in the art to make and use the invention. For claim construction purposes, the written description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. A patentee is free to be his own lexicographer, although any special definition given to a word must be clearly defined in the specification. Markman, 52 F.3d at 978, 979, 34 USPQ2d at 1328, 1329. To determine likelihood of success, in this investigation the administrative law judge may construe disputed language as a matter of law.

The administrative law judge may, in his discretion, receive extrinsic evidence to aid him in coming to a correct conclusion as to the true meaning of language employed in a patent. Extrinsic evidence consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries and learned treatises. This evidence may be helpful to explain scientific principles, the meaning of technical terms, and terms of art that appear in the patent and prosecution history. It may also demonstrate the state of the prior art at the time of the invention. Extrinsic evidence may be necessary to inform the administrative law judge about the language in which the patent is written. Extrinsic evidence, however, is not for the purpose of clarifying ambiguity in claim terminology. It is not ambiguity in the document that creates the need for extrinsic evidence

issued may reflect either unartful claim drafting, a conscious attempt to create ambiguity, or a desire to claim a wide variety of inventions that are not described or enabled in the specification. See Genentech Inc. v. The Wellcome Foundation Ltd., 29 F.3d 1555, 1564, 31 USPQ2d 1161, 1167 (Fed. Cir. 1994).

a. The '473 Patent

The '473 patent, entitled "Method Of Using Electronically Reconfigurable Logic Circuits," issued on July 30, 1991. It is based on Application Serial No. 417,196, filed October 4, 1989. This application was a continuation-in-part of Application Serial No. 254,463 filed on October 5, 1988, now abandoned. The named inventors are Michael R. Butts of Portland, Oregon and Jon A. Batcheller of Newburg, Oregon (FF 382).

Claim 8 of the '473 patent, the only claim of the '473 patent in issue in Motion No. 383-1, reads:

> 8. The method of claim 7 which further includes:
>
> connecting each of said reconfigurable interconnect ERCLC(s) to at least one but not all of the pins of each of said N ERCLCs.

(FF 386).

Dependent claim 7, which is incorporated by reference in dependent claim 8, reads:

> 7. The method of claim 6 in which the ERCLCs each include a plurality of pins, and in which the interconnecting steps include:
>
> providing at least one reconfigurable interconnect; and
>
> connecting each of said reconfigurable interconnects to at least one but not all of the pins of a plurality of said N ERCLCs.

(FF 389). Dependent claim 6, which is incorporated by reference in dependent claim 7, reads:

6. The method of claim 1 which further includes:

(a) providing N ERCLCs;

(b) partitioning the first input data into N portions;

(c) providing each portion of the partitioned data to the ERCLC to which it corresponds, so the portion of the digital logic network represented thereby takes actual operating form on said ERCLC;

(d) interconnecting the N ERCLCs so that each of the ERCLCs is connected to at least one other of the ERCLCs and so that each of the nets specified in the input data is implemented; and

(e) repeating steps (b) through (d) for the second input data.

(FF 388). Independent claim 1, which is incorporated by reference in dependent claim 6, reads:

1. A method comprising the steps:

providing first and second electrically reconfigurable logic circuits (ERCLCs);

providing first input data representative of a first digital logic network, said input data including primitives comprised of boolean logic gates, and nets interconnecting said primitives;

automatically partitioning said first input data into first and second portions;

providing the first portion of the partitioned first data to the first ERCLC so a first portion of the first digital logic network represented thereby takes actual operating form on the first ERCLC;

providing the second portion of the partitioned first data to the second ERCLC so a second portion of the first digital logic network represented thereby takes actual operating form on the second ERCLC;

interconnecting the first and second ERCLCs so that at least one net specified in the first input data extends between the first and second ERCLCs;

providing second input data representative of a second digital logic network entirely unrelated to the first digital logic network except that both include

primitives comprised of boolean logic gates, and nets interconnecting said primitives, and both are to take actual operating form on the same ERCLCs;

automatically partitioning said second input data into first and second portions;

providing the first portion of the partitioned second data to the first ERCLC so a first portion of the second digital logic network represented thereby takes actual operating form on the first ERCLC;

providing the second portion of the partitioned second data to the second ERCLC so a second portion of the second digital logic network represented thereby takes actual operating form on the second ERCLC;

interconnecting the first and second ERCLCs so that at least one net specified in the second input data extends between the first and second ERCLCs.

(FF 387).

As seen supra, not only is claim 7 but also dependent claim 6 and independent claim 1 are incorporated by reference in dependent claim 8. In issue for claim interpretation are phrases in claim 8 and those incorporated by reference through claims 7, 6 and 1 into claim 8. Those phrases are treated infra as i, ii, iii, iv, v, vi and vii. Also treated infra, as viii, is the interpretation of claim 8 with respect to the term "partial crossbar."

i. "electrically reconfigurable logic circuits (ERCLCs)"

The phrase "electrically reconfigurable logic circuits (ERCLCs)" in independent claim 1, which is incorporated by reference in dependent method claim 8 through dependent claims 7 and 6, is not defined in the specification of the '473 patent. The term "electrically reconfigurable logic circuits (ERCLCs)" first appeared in an amendment dated December 20, 1990, filed during the prosecution of the '473 patent (FF 392). Independent claim 1 was amended by deleting "gate arrays (ERCGAs)" and inserting "logic circuits (ERCLCs)," which resulted in the claimed phrase "electrically reconfigurable logic circuits (ERCLCs)" in

patent claim 1. Each of dependent claims 6, 7, and 8 were amended by deleting each appearance of "ERCGAs" and replacing it with "ERCLCs." Dependent claim 7 also was amended by deleting the phrase "additional ERCGA to serve as a" (FF 392).

Respondents argued that the claim term "electrically reconfigurable logic circuits (ERCLCs)" of independent claim 1 should be interpreted as an "electrically reconfigurable gate array (ERCGA)."[13] Complainant argued, with respect to the term "electrically reconfigurable logic circuits (ERCLCs)," that the "difference between ERCGA and ERCLC is very clearly set out [in the '473 patent's file history]." (Tr. at 4670). The staff agreed with complainant's arguments. (Tr. at 4769).

An "ERCGA" is defined in the specification of the '473 patent as:

> an electronically reconfigurable gate array, that is a collection of combinational logic, and input/output connections (and optionally storage) whose functions and interconnections can be configured and reconfigured many times over, purely by applying electronic signals

(FF 393). The applicants stated in a December 20, 1990 amendment that the term "ERCGA" was replaced with the term "ERCLC":

> to make clear that the invention may be practiced with reconfigurable logic circuits that are not technically "gate arrays."

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[13] During closing arguments, respondents' counsel argued:

> JUDGE LUCKERN: . . . . What is your position as to how I should interpret ERCLCs of claim 1 of the '473 patent, line 3?
>
> MR. ANTHONY: I don't think anyone knows what that means beyond what's in the patent claim because it's not in the file wrapper other than the amendment. It's not defined in the file wrapper, it's not defined in the patent. For the purpose of this case, I think everybody has been choosing to define it as an ERCGA, which is defined in the patent.

(Tr. at 4668-4669).

(FF 394). Thus, based on the specification, and applicants' arguments made during prosecution, the administrative law judge finds that the term "ERCLCs" in the claim 1 phrase "electrically reconfigurable logic circuits (ERCLCs)" includes logic circuits that meet the definition of "ERCGA" in the specification of the '473 patent and also includes reconfigurable logic circuits that are "not technically" gate arrays.

ii. "N ERCLCs"

With respect to "N" of the term "N ERCLCs" in each of dependent claims 7 and 8 respondents argued that "N" is any integer which must be at least two, in light of independent claim 1. (RBr at 16). Complainant argued that the claim term "N" refers to an integer equal to three or more, because if N were equal to two, claim 1 would be identical to claim 6, and claim 7 would be identical to claim 8 (CFF 77).

The language of claim 6 of the '473 patent reads in part: "[t]he method of claim 1 which further includes: (a) providing N ERCLCs." (emphasis added). Independent claim 1 calls for "providing first and second electrically reconfigurable logic circuits (ERCLCs)." (FF 387). Each of complainant's Butts and respondents' technical expert Wolfe (FF 379) testified that "N" is an integer value which typically refers to a positive integer value (i.e. one or more) (FF 397). If the term "N" were given its typical interpretation as a positive integer (at least one), and given that claim 1 requires two ERCLCs (first and second ERCLC), claim 6 would "further include" providing at least one additional ERCLC, for a total of at least three ERCLCs.

At the hearing, respondents' technical expert Wolfe testified that, if the claim phrase "N ERCLCs" of claim 6 were read as "two ERCLCs", there would be no distinction

between dependent claim 6 and independent claim 1 (FF 398). Moreover, a dependent claim is, by definition, narrower than the claim from which it depends. see e.g. U.S. Patent & Trademark Office, Manual of Patent Examining Procedure § 1.75(c) (5th ed. rev. 16, 1994) ("One or more claims may be presented in dependent form, referring back to and further limiting another claim in the same application.") (emphasis added); Wahpeton Canvas Company, Inc. v. Frontier, Inc., 870 F.2d 1546, 10 USPQ2d 1201 (Fed. Cir. 1989). Accordingly, dependent claim 6 must add an additional limitation to independent claim 1.

In view of the foregoing, the administrative law judge finds that each of dependent claims 6, 7 and 8 are directed to a method employing three or more ERCLCs.

iii. "first input data representative of a first digital logic network"

It is argued by respondents, with respect to the phrase "first input data representative of a first digital logic network" in independent claim 1, which is incorporated by reference in dependent claim 8, that the phrase is modified by the phrase "automatically partitioning said first input data," which latter phrase is also in independent claim 1, such that the phrase in issue requires that "in the first breaking up of the input data, the user circuit . . . that there has to be a correlation, a physical one-for-one correlation between those chunks, and the input data." (Tr. at 4680-4681). In support, respondents argued that the "exemplary [partitioning] algorithms would take a circuit and divide it into pieces, and each of those pieces would have a one-to-one relationship with the original divided circuit." (Tr. at 4672). Thus, respondents argued that the "input data" called for in claim 8 in its reference to independent claim 1 thru dependent claims 6 and 7 must include some one to one correspondence with the "primitives comprised of boolean logic gates, and nets" of a user's

input design, and must preserve the actual operating form of the user's circuit, including the nets interconnecting the logic devices (RBr at 37, Tr. 4674-4675). Complainant and the staff have argued that no such one-to-one correspondence is required (Tr. at 4677, 4684).

Claim 1 requires "first input data representative of a first digital logic network" (emphasis added). The claim does not require, for example, first input data "identical" to or "having one to one correspondence with" a user design. Moreover, the specification of the '473 patent makes clear that the input data partitioned in the claimed method is not the user's actual design (FF 400, 401). For example, the '473 patent teaches that a user design is converted into "logic chip-specific primitives," and that in some instances only the functionality of the user's design is maintained, not the nets of the input design (FF 400, 401). In addition, as complainant's technical expert McCluskey (FF 378) testified, the input data:

> just represents the design. I don't think that that requires that it enumerate the design in this language or in terms of these primitives, and the discussion in the patent specifically points out that the input data doesn't have to be in terms of elementary gates, and it discusses the transformation into elementary gates.

(FF 399).

Even accepting respondents' argument that the partitioning algorithms of the preferred embodiment, detailed in the specification and known at that time, involved the use of input data having a one-to-one relationship to a user's design, the administrative law judge finds that that fact could not alter the clear language of independent claim 1 requiring "input data representative of a first digital logic network" (emphasis added) in the claimed method. It is error to read a feature of the preferred embodiment as a claim limitation. Laitram Corp., 863 F.2d at 865, 9 USPQ2d at 1296. Thus, it is found that the limitation "first input data

representative of a first digital logic network," as incorporated by reference in claim 8, reads on input data that is representative of a user's design and is not restricted to a one-to-one correspondence with the physical elements or nets of the user's circuit design.

iv. "interconnecting" with respect to the ERCLCs

Respondents argued that the term "interconnecting" with respect to "interconnecting" the ERCLCs of claim 1[14] and the phrase "interconnecting the N ERCLCs" in claim 6, incorporated by reference in claim 8, require each of the ERCLCs to be directly connected to at least one other ERCLC. (RBr at 38-39; Tr. at 4696).[15] Complainant and the staff argued

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[14] Independent claim 1 has the language:

> interconnecting the first and second ERCLCs so that at least one net specified in the first input data extends between the first and second ERCLCs
>
> * * *
>
> interconnecting the first and second ERCLCs so that at least one net specified in the second input data extends between the first and second ERCLCs (FF 387).

[15] Respondents, in support of their position, argued that each of complainant and the staff have read the term "connecting" in the claim 8 phrase "connecting each of said reconfigurable interconnect ERCLC(s) to at least one but not all of the pins of each of said N ERCLCs" to require a direct, hard wire connection between an interconnect ERCLC and the pins of said N ERCLCs. Therefore, respondents argued that the term "interconnecting the N ERCLCs" must be interpreted "consistently" with the term "connecting" to also require a direct connection (Tr. at 4708-4709, 4714-4715). At the hearing, complainant's Butts testified:

> the word "connecting" in claim 8. Given that that is discussing the actual ERCLCs involved and the interconnect devices, an engineer would certainly read that as a permanent hard wire connection that is direct.

(Butts, Tr. at 433). However, at closing arguments, complainant's counsel argued:

> Butts plainly was talking about . . . the connection between a logic and an interconnect chip and not a logic to logic chip, and so everything that [respondents' counsel] has said has absolutely no applicability to the claim language at hand.

(Tr. at 4703). The staff argued that the language of claim 8 "connecting each of said reconfigurable interconnect ERCLC(s) to at least one but not all of the pins of each of said N ERCLCs" did require

that claim 1 and claim 6 are directed to either a direct or indirect interconnection between ERCLCs, and that claim 7 and 8 only require an indirect connection between the N ERCLCs through the use of a reconfigurable interconnect (Tr. at 4699).

Neither independent claim 1 or dependent claim 6 are expressly limited to "direct" interconnects. The specification of the '473 patent teaches several types of interconnect architectures, including "direct interconnect," "channel routing" and "partial crossbar" interconnects (FF 404).[16] The '473 patent teaches that, with respect to direct interconnects

> In the direct interconnect, all logic chips are directly connected to each other . . . without the use of interconnect chips. The interconnect consists only of electrical connections among logic chips. Many different patterns of interconnecting logic chips are possible.

(FF 405). Figure 2 of the '473 patent is an example of the "direct interconnects" wherein "logic chips . . . [are] connected to neighboring logic chips." The specification of the '473 patent also teaches that, in the described "partial crossbar interconnect," "logic chips [are] . . . interconnected by . . . crossbar chips" (FF 405). Fig. 7 of the '473 patent shows "interconnecting the same four logic chips as in FIGS 1 and 2. Four crossbar chips . . . are used. Each crossbar chip connects to the same two pins of each logic chip" (FF 405). Thus, the administrative law judge finds that the specification uses the term

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a "wire or trace which goes from the interconnect device to the logic device, from pin to pin." (Tr. at 4710). Complainant adopted the staff's position on this point (Tr. at 4713). The administrative law judge finds no inconsistency in each of complainant's and the staff's proposed interpretation of the terms "connecting" in claim 8 and "interconnecting" in claims 1 and 6.

[16] The preferred embodiment uses the "partial crossbar interconnect" (FF 405).

"interconnecting" to refer to both direct, hard wire connections between logic chips and indirect connections through interconnect chips.[17]

While each of independent claim 1 and dependent claim 6 use the term "interconnecting" without modification, claim 13 of the '473 patent, (FF 391) which depends from independent claim 1, adds the limitation of "directly interconnecting neighboring ERCLCs." (emphasis added). It is well settled that "the presence of an express limitation in one claim negatives an intent similarly to limit by implication a claim in which the limitation is not expressed." 4 Chisum, Patents, § 18.03[2] (1995), citing Texas Co. v. Globe Oil & Ref. Co. 112 F.Supp. 455, 467, 98 USPQ 312 (N.D. Ill. 1953) aff'd 225 F.2d 725, 106 USPQ 392 (7th Cir. 1955); see also Marsh McBirney, Inc. v. Montedoro-Whitney Corp., 882 F.2d 498, 504, 11 USPQ2d 1794, 1798 (Fed. Cir. 1989). Thus, the administrative law judge finds that the claim term "interconnecting" in independent claim 1 and the phrase "interconnecting the N ERCLCs" of claim 6 refer to either a direct interconnection or an indirect interconnection.

Claim 7, which incorporates by reference claims 1 and 6, provides "the interconnecting steps include: providing at least one reconfigurable interconnect." The specification teaches, with respect to the "channel routing interconnects" that:

> the chips are divided into some which are not used for logic, dedicated only to accomplishing interconnections, thus becoming interconnect chips, and others are used exclusively for logic, remaining logic chips. In particular, logic chips are not directly interconnected to each other, but instead connected only to interconnect chips.

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[17] As admitted by respondents' expert Wolfe, there is no disclosure in the '473 patent specification which shows logic chips connected to other logic chips through both indirectly (using interconnect chips) and directly (using a hard wire or trace) (FF 406).

(FF 405) (emphasis added). The specification further teaches that:

> An interconnect is a reconfigurable means for passing logic signals between a large number of chip I/O pins as if the pins were interconnected with wires.

(FF 405) (emphasis added). Thus, when the interconnecting step includes "at least one reconfigurable interconnect" the administrative law judge finds that the specification teaches an indirect connection between logic chips.

In light of the claim language, as well as the specification, the administrative law judge finds that, the phrase "interconnecting the N ERCLCs so that each of the ERCLCs is connected to at least one other of the ERCLCs. . . ." limitation of claim 6 would be satisfied by either a direct or indirect connection between logic chips. He further finds that dependent claim 7, incorporated by reference into dependent method claim 8, limits the "interconnecting" step of dependent claim 6 to an indirect connection using at least one reconfigurable interconnect ERCLC (FF 389). Thus, claim 8 does not require any direct connection between logic ERCLCs.

v. "said reconfigurable interconnect ERCLC(s)"

Dependent method claim 8 has the phrase "said reconfigurable interconnect ERCLC(s)." Dependent method claim 7, which is incorporated by reference in dependent claim 8, has the phrase "providing at least one reconfigurable interconnect." Complainant has argued that the administrative law judge should rewrite the claim 8 phrase "interconnect ERCLC(s)" as simply "interconnect." (Tr. at 4636). Each of respondents and the staff

argued that claim 8 should be directed to a "reconfigurable interconnect ERCLC(s)." (Tr. 4651; Tr. 4666).[18]

The specification of the '473 patent teaches that "ERCGA devices . . ., namely the LCA, the ERA and the EEPLD, . . . may be used as interconnect chips. . . . The LCA is used for crossbar chips in the preferred implementation. . . ." (FF 408). The administrative law judge has construed the claim term "ERCLC" to encompass an "ERCGA," see section i. supra. Thus, the specification teaches than an ERCLC may be used as an interconnect chip.

On its face, claim 8 can be understood as requiring reconfigurable interconnect ERCLC(s) because claim 8 refers to the "reconfigurable interconnect" as "ERCLC(s)." Nothing in either the specification of the '473 patent or the prosecution history indicates that the phrase "reconfigurable interconnect ERCLC" should be rewritten as "reconfigurable interconnect."

vi. "providing at least one reconfigurable interconnect"

Claim 7, incorporated by reference in dependent claim 8, includes the phrase "providing at least one reconfigurable interconnect." As discussed supra in section v., the administrative law judge has interpreted claim 8 as requiring the step of "providing at least

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[18] Respondents argued that the administrative law judge should rewrite dependent claim 7 to require a "reconfigurable interconnect ERCLC(s)." (Tr. at 4651). However, such argument is inconsistent with the prosecution history. Thus, a December 20, 1990 amendment to the '473 patent modified dependent method claim 7 (application claim 8) by substituting the term "ERCLC" for the term "ERCGA," as well as deleting the phrase "additional ERCGA to serve as a" and changing the phrase "reconfigurable interconnect ERCGA" to "reconfigurable interconnects." (FF 392). In the same amendment, identical modifications were made to dependent method claim 5 (application claim 6) (FF 392, 410). Applicants argued in the prosecution of the '473 patent with respect to claim 5 (application claim 6):

> Dependent claim 6 [patent claim 5] has been amended to specify that the reconfigurable interconnects need not be ERCLCs [FF 394].

one reconfigurable interconnect ERCLC." Respondents argued that "in claim 8, the interconnect must contain logic" (RBr at 16) (emphasis in original). Complainant argued that "an interconnect ERCLC must have the ability to establish many logic interconnections between arbitrarily chosen groups of I/O pins at once, in an electrically reconfigurable fashion" (CFF 84).

The specification of the '473 patent describes "interconnect chip devices" as follows:

> Interconnect chips include crossbar chips, used in full and partial crossbar interconnects, and routing chips, used in direct and channel-routed interconnects. For a device to be useful as a Realizer interconnect chip:
>
> 1) It should have the ability to establish many logical interconnections between arbitrarily chosen groups of I/O pins at once, each interconnection receiving logic signals from its input I/O pin and driving those signals to its output I/O pin(s).
>
> 2) It should be electronically reconfigurable, in that its interconnect is defined electronically, and may be redefined to suit many different designs.
>
> 3) If a crossbar summing technique is used to interconnect tri-state nets in the partial crossbar interconnect, it should be able to implement summing gates. (If not, other tri-state techniques are used, as discussed in the tri-state section.)

(FF 407). The preferred embodiment disclosed in the '473 patent uses the Xilinx LCA as an "interconnect ERCLC." (FF 408). The specification also teaches that "interconnect chips" are distinct from "logic chips." The specification explicitly teaches that:

> "the ERCGA devices . . . satisfy these requirements, so they may be used as interconnect chips. Even though little or no logic is used in the interconnect chip, the ability to be configured into nearly any digital network includes the ability to pass data directly from input to output pins"

(FF 408) (emphasis added). With respect to the "channel-routing interconnects" the specification teaches:

> "the chips are divided into some which are not used for logic, dedicated only to accomplishing interconnections, thus becoming interconnect chips, the others are used exclusively for logic, remaining logic chips."

(FF 405) (emphasis added). The specification of the '473 patent further teaches:

> In the crossbar summing configuration, the summing OR gate is placed on the crossbar chip, making use of the fact that the crossbar chips in some embodiments are implemented with ERCGAs, such as LCAs, which have logic available.
>
> * * *
>
> Crossbar summing deviates from the practice of putting all logic in the logic chips and none in the crossbar chips, but an important distinction is that the logic placed in the crossbar chip is not part of the realized design's logic. It is only logic which serves to accomplish the interconnection functionality of a tri-state net.

(FF 409) (emphasis added).

In view of specification of the '473 patent, the administrative law judge finds that, while "interconnect ERCLC" must have logic capability, such as is found in an ERCGA, the "interconnect ERCLC" has to be "dedicated only to accomplishing interconnections," and any logic has to only serve to accomplish interconnection functionality.

vii. "connecting each of said reconfigurable interconnect ERCLC(s) to at least one but not all of the pins of each of said N ERCLCs"

Dependent method claim 8, requires "connecting each of said reconfigurable interconnect ERCLC(s) to at least one but not all of the pins of each of said N ERCLCs" (FF 386). Respondents argued that claim 8 requires "the interconnect [ERCLC] to be connected to at least one but not all of the pins of each of said N ERCLCs [and that] [t]his means that each chip, or ERCLC, on the board must be considered, not merely a subset of

the chips." (RBr at 16). Complainant and the staff argued that this claim limitation may be met by a subset of chips on a logic board. (CBr at 44-45, SBr at 25-29).

There is no express limitation in any of independent claim 1, dependent claim 6, dependent claim 7 or dependent claim 8 in issue that would limit those claims to an entire logic board (FF 386-389). Dependent claim 8, thru dependent claim 7, requires "providing at least one reconfigurable interconnect ERCLC(s)" see section v. supra. While the plain language of claim 8 refers to "each of said reconfigurable interconnect ERCLC(s)," respondents would read that limitation as "each of every reconfigurable interconnect ERCLC(s) on a logic board." The specification teaches, with respect to "system level interconnects" that:

> To distinguish among crossbar chips in a Realizer system, the partial crossbar interconnect which interconnects logic chips is called the X-level interconnect, and its crossbar chips are called Xchips. The interconnect which interconnects logic boards is called the Y-level interconnect, and its crossbar chips are called Ychips. In the X-level interconnect, the I/O pins of each logic board are divided into proper subsets, using the same division on each logic board. The pins of each Ychip are connected to the same subset of pins from each of every logic board. As many Ychips are used as there are subsets, and each Ychip has as many pins as the number of pins in the subset times the number of logic boards.
>
> * * *
>
> A specific example is the preferred embodiment:
>
> The partial crossbar interconnect is used hierarchically at three levels across the entire hardware system.
>
> A logic board consists of up to 14 logic chips, with 128 interconnected I/O pins each, and an X-level partial crossbar composed of 32 Xchips. Each Xchip has four paths to each of the 14 Lchips (56 total), and eight paths to each of two Ychips, totaling 512 logic board I/O pins per board.
>
> A box contains one to eight boards, with 512 interconnected I/O pins each, and a Y-level partial crossbar composed of 64 Ychips. Each Ychip has eight paths to

> an Xchip on each board via logic board I/O pins, and eight paths to one Zchip, totaling 512 box I/O pins per box.
>
> A rack contains one to eight boxes, with 512 interconnected I/O pins.each, and a Z-level partial crossbar composed of 64 Zchips. Each Zchip has eight paths to a Ychip in each box via box I/O pins.

(FF 411). This configuration is disclosed in Fig. 18 of the '473 patent. Thus, the preferred embodiment of the '473 patent teaches that "Xchips," which are "reconfigurable interconnect ERCLCs" are connected to "Ychips," which are "reconfigurable interconnect ERCLCs." The "Ychips" are in turn connected to "Zchips," which are "reconfigurable interconnect ERCLCs." None of the "Ychips" or "Zchips" are connected to any logic ERCLCs. (FF 411). While the preferred embodiment does show a logic board wherein each interconnect chip on that logic board is connected to every logic chip, it is improper to read a feature of the preferred embodiment as a claim limitation. see e.g. Intel Corp. v. U.S. Int'l Trade Comm'n, 946 F.2d 821, 836, 20 USPQ2d 1161, 1174 (Fed. Cir. 1991) (Intel Corp.). Moreover, every logic ERCLC in the preferred embodiment is not connected to every interconnect ERCLC. Rather, thirty two "Xchips" are connected to logic ERCLCs, while sixty four "Ychips" are connected only to "Xchips" and "Zchips," both of which are "interconnect ERCLCs," and sixty four "Zchips" are only connected to said sixty four "Ychips." Also, certain interconnect ERCLCs crossbar chips are connected to logic chips, and other crossbar chips are not connected to logic chips (FF 411).

The preamble of independent claim 1, incorporated by reference in dependent claim 8, directs that claim to "[a] method comprising the steps." It is well settled that "[i]n the lexicon of patent law, 'comprising' means that the 'recited elements are only a part of the device.' In other words, if the invention is claimed as 'comprising elements X and Y, it may

also 'read on' and cover a device with elements X, Y, and Z." 2 Chisum, Patents, § 8.06[1][b] (1995) (citations omitted); compare Moleculon, 793 F.2d at 1271, 229 USPQ at 812. The scope of a particular structure recited in a claim is not affected by the mere use of the term "comprising." As the Federal Circuit stated in Stiftung v. Renishaw PLC, 945 F.2d 1173 (Fed. Cir. 1991) (Stiftung), the issue is:

> whether the claim and specification in effect preclude any additional . . . means or otherwise require that the claims be limited to devices containing only the structures of the embodiments specifically described in the specification. Indeed, claim 2, which uses the term 'comprising,' is an 'open' claim which will read on devices which add additional element.

Id. at 1178, citing A.B. Dick Co. v. Burroughs Corp., 713 F.2d 700, 703, 218 USPQ 965, 967-68 (Fed. Cir. 1983), cert. denied, 464 U.S. 1042 (1984) (A.B. Dick). The administrative law judge finds nothing in the claims, specification, or prosecution history of the '473 patent that would preclude the addition of additional interconnect ERCLC(s) beyond the "at least one interconnect ERCLC(s)" required by claim 8. Thus, the administrative law judge finds that the claimed steps of providing at least one reconfigurable interconnect ERCLC, and connecting each of said interconnect ERCLC(s) to at least one but not all of the pins of each of said N ERCLCs, simply requires at least one interconnect ERCLC that is connected in the claimed manner and does not require that every interconnect ERCLC on a logic board must be connected to at least one pin of every logic ERCLC on a logic board.

viii. "partial crossbar"

Claim 8 rewritten in independent form[19] to include all of the limitations of the antecedent claims 7, 6 and 1 in the chain of dependency, reads as follows:

A method comprising the steps of:

(a)[20] providing N electrically reconfigurable logic circuits (ERCLCs), the ERCLCs each includ[ing] a plurality of pins;[21]

providing first input data representative of a first digital logic network, said input data including primitives comprised of boolean logic gates, and nets interconnecting said primitives;[22]

(b) automatically partitioning said first input data into N portions;[23]

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[19] Respondents objected to rewriting dependent claim 8 in issue in independent form on the grounds that the rewritten claim "misleadingly combines separate elements from separate claims in such a way as to suggest an inaccurate relationship between the elements." (RO73; Tr. at 4873 - 4876).

The administrative law judge finds the combination of the method steps in issue is appropriate and helpful in his consideration of dependent claim 8, the only claim of the '473 patent in issue. While a dependent claim of a patent is to be considered individually on its merits, and a dependent claim and independent claim of a patent need not necessarily even fall within the same statutory class of subject matter a claim "in dependent form" incorporates by reference any previous claim it refers to. See 2 Chisum, Patents, § 8.06[5] (1995).

[20] Dependent claim 6 provides the labels (a), (b), (c), (d) and (e) for the method steps in claim 6.

[21] Independent claim 1 requires the step of "providing first and second electrically reconfigurable logic circuits (ERCLCs)." Dependent Claim 6, which incorporates by reference the limitations of independent claim 1, requires "providing N ERCLCs." Dependent claim 7, which incorporates by reference claim 1 and claim 6, requires "the ERCLCs each include a plurality of pins." Dependent method claim 8 incorporates by reference the limitations of each of claims 1, 6 and 7 (FF 386-389).

[22] This language of independent claim 1 is incorporated by reference in dependent method claim 8 (FF 386-389).

[23] Independent claim 1 requires the step of "automatically partitioning said first input data into first and second portions." Dependent claim 6 requires "partitioning the first input data into N portions." Dependent claim 8 incorporates by reference the limitations of each of claims 1 and 6 (FF 386-389).

(c) providing each portion of the partitioned data to the ERCLC to which it corresponds, so the portion of the digital logic network represented thereby takes actual operating form on said ERCLC;[24]

(d) interconnecting the N ERCLCs so that each of the ERCLCs is connected to at least one other of the ERCLCs and so that each of the nets specified in the input data is implemented,[25] the interconnecting steps include:

providing at least one reconfigurable interconnect ERCLC[26]; and

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[24] Independent claim 1 requires the steps of:

providing the first portion of the partitioned first data to the first ERCLC so a first portion of the first digital logic network represented thereby takes actual operating form on the first ERCLC

providing the second portion of the partitioned first data to the second ERCLC so a second portion of the first digital logic network represented thereby takes actual operating form on the second ERCLC

Dependent claim 6, which incorporates by reference the limitations of independent claim 1, requires "providing each portion of the partitioned data to the ERCLC to which it corresponds, so the portion of the digital logic network represented thereby takes actual operating form on said ERCLC." Thus, the dependent claim 6 method step of providing each portion of partitioned data to the ERCLC to which it corresponds is the equivalent of the method steps of claim 1 relating to providing a first portion of partitioned data to a first ERCLC and a second portion of partitioned data to a second ERCLC, with the exception that claim 1 relates to 2 ERCLCs while dependent claim 6 relates to an arbitrary number (three or more) of ERCLCs. Dependent method claim 8 incorporates by reference the limitations of each of independent claim 1, dependent claim 6 and dependent claim 7 (FF 386-389).

[25] Independent claim 1 requires the step of "interconnecting the first and second ERCLCs so that at least one net specified in the first input data extends between the first and second ERCLCs." Dependent claim 6 requires "interconnecting the N ERCLCs so that each of the ERCLCs is connected to at least one other of the ERCLCs and so that each of the nets specified in the input data is implemented." Dependent method claim 8 incorporates by reference the limitations of each of claims 1 and 6 (FF 386-389).

[26] Dependent claim 7 adds the requirement that the "interconnecting steps" in the method of dependent claim 6 further includes "providing at least one reconfigurable interconnect." Dependent claim 8 requires an "interconnect ERCLC." See section v., supra

connecting each of said reconfigurable interconnect ERCLC(s) to at least one but not all of the pins of each of said N ERCLCs;[27] and

(e) repeating steps (b) through (d) for second input data representative of a second digital logic network entirely unrelated to the first digital logic network except that both include primitives comprised of boolean logic gates, and nets interconnecting said primitives, and both are to take actual operating form on the same ERCLCs;[28]

(FF 390).

Claim 8 does not have the language "partial crossbar." The following attributes of the "partial crossbar" interconnect however are detailed in the specification:

> In the partial crossbar interconnect, the I/O pins of each logic chip are divided into proper subsets, using the same division on each logic chip. The pins of each

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[27] Dependent method claim 7 includes the language "connecting each of said reconfigurable interconnects to at least one but not all of the pins of a plurality of said N ERCLCs." Dependent method claim 8 further includes "connecting each of said reconfigurable interconnect ERCLC(s) to at least one but not all of the pins of each of said N ERCLCs."

[28] Independent claim 1 includes the method steps of :

providing second input data representative of a second digital logic network entirely unrelated to the first digital logic network except that both include primitives comprised of boolean logic gates, and nets interconnecting said primitives, and both are to take actual operating form on the same ERCLCs;

automatically partitioning said second input data into first and second portions;

providing the first portion of the partitioned second data to the first ERCLC so a first portion of the second digital logic network represented thereby takes actual operating form on the first ERCLC;

providing the second portion of the partitioned second data to the second ERCLC so a second portion of the second digital logic network represented thereby takes actual operating form on the second ERCLC;

interconnecting the first and second ERCLCs so that at least one net specified in the second input data extends between the first and second ERCLCs.

Dependent claim 6, incorporating by reference independent claim 1, summarizes this group of steps as "repeating steps (b) through (d) for the second input data." Dependent claim 8 incorporates by reference each of independent claim 1 and dependent claim 6.

crossbar chip are connected to the same subset of pins from each of every logic chip.

(FF 405). In the language of claim 8, the "crossbar chip" corresponds to "said reconfigurable interconnect ERCLC(s)," (see section v., supra) the "logic chip" corresponds to "N ERCLCs," (see section i., supra) and the connections, viz. "the pins of each crossbar chip are connected to the same subset of pins from each of every logic chip," correspond to the claim 8 method step of "connecting each of said reconfigurable interconnect ERCLC(s) to at least one but not all of the pins of each of said N ERCLCs." Thus, the administrative law judge finds that claim 8 incorporates at least those features of the "partial crossbar interconnect" described in the specification of the '473 patent. Three illustrative examples of the "partial crossbar interconnect" are shown in the following Fig. 6, Fig. 7 and Fig. 18 of the '473 patent:

b. The '496 Patent

The '496 patent, entitled "Partial Crossbar Interconnect Architecture For Reconfigurably Connecting Multiple Reprogrammable Logic Devices In A Logic Emulation

System," issued on September 5, 1995, based on Application Serial No. 270,234. This application was a continuation of abandoned Application Serial No. 175,981, filed on December 30, 1993, which was a continuation of abandoned Application Serial No. 698,734, filed on May 10, 1991, which was a continuation-in-part of Application Serial No. 417,196, filed on October 4, 1989 and which issued as U.S. Patent No. 5,036,473, which was a continuation-in-part of abandoned Application Serial No. 254,463, filed on October 5, 1988. The named inventors are Michael R. Butts and Jon A. Batcheller (FF 412). The portion of the term of this patent subsequent to July 30, 2008 has been disclaimed (FF 412). Claims 1, 2, 3 and 15 are in issue in Motion No. 383-1.

Claim 1 reads:

> An electrically reconfigurable logic assembly for use in an electrically reconfigurable hardware emulation system which can be configured with a circuit design in response to the input of circuit information, said electrically reconfigurable logic assembly comprising:
>
> a plurality of reprogrammable logic devices, each of said reprogrammable logic devices having internal circuitry which can be reprogrammably configured to provide functional elements selected from the group of at least combinatorial logic elements and storage elements, each of said reprogrammable logic devices also having programmable I/O terminals which can be reprogrammably connected to selected ones of said functional elements configured into said reprogrammable logic devices;
>
> a plurality of reprogrammable interconnect devices, each of said reprogrammable interconnect devices having I/O terminals and internal circuitry which can be reprogrammably configured to provide interconnections between selected ones of said I/O terminals; and
>
> a set of fixed electrical conductors connecting said programmable I/O terminals on said reprogrammable logic devices to said I/O terminals on said reprogrammable interconnect devices such that each of said reprogrammable interconnect devices is connected to at least one but not all of said programmable I/O terminals on each of said reprogrammable logic devices.

(FF 415). Dependent claim 2 reads:

> An electrically reconfigurable logic assembly as recited in claim 1, wherein said reprogrammable logic devices comprise programmable gate arrays.

(FF 416). Dependent claim 3 reads:

> An electrically reconfigurable logic assembly as recited in claim 1, wherein said reprogrammable logic devices comprise FPGAs.

(FF 417). Independent claim 15 reads:

> An electrically reconfigurable logic assembly for use in an electrically reconfigurable hardware emulation system which can be configured with a circuit design in response to the input of circuit information, said electrically reconfigurable logic assembly comprising:
>
> a plurality of reprogrammable logic devices, each of said reprogrammable logic devices having internal circuitry which can be reprogrammably configured to provide functional elements selected from the group of at least combinatorial logic elements and storage elements, each of said reprogrammable logic devices also having programmable I/O terminals which can be reprogrammably connected to selected ones of said functional elements configured into said reprogrammable logic devices;
>
> a plurality of reprogrammable interconnect devices, each of said reprogrammable interconnect devices having I/O terminals and internal circuitry which can be reprogrammably configured to provide interconnections between selected ones of said I/O terminals;
>
> a set of fixed electrical conductors connecting said programmable I/O terminals on said reprogrammable logic devices to said I/O terminals on said reprogrammable interconnect devices such that each of said reprogrammable interconnect devices is connected to at least one but not all of said programmable I/O terminals on each of said reprogrammable logic devices; and
>
> an interface structure arranged to provide signal paths for signals carrying information to or from designated ones of said functional elements in said reprogrammable logic devices.

(FF 418). In issue for claim interpretation are the phrases treated infra as i, ii, iii, iv, v, vi, vii, viii and ix.

i. "partial crossbar interconnect"

None of independent claims 1 and 15 or dependent claims 2 and 3 of the '496 patent has the language "partial crossbar." The staff argued that "[e]ach of the claims at issue in the '496 patent [require the] . . . . type of interconnection . . . referred to in the specification as the 'partial crossbar' interconnection." (SBr at 19). Complainant argued that each of independent claims 1 and 15, and dependent claims 2 and 3 are directed to a "partial crossbar" interconnect. (CFF 87, 107). Respondents argued that "the partial crossbar architecture is found in the entire Claim 1." (RRFF 53).

The title of the '496 patent is "Partial Crossbar Interconnect Architecture for Reconfigurably Connecting Multiple Reprogrammable Logic Devices In A Logic Emulation System." (FF 412 (emphasis added). The specification contains a detailed description of the "partial crossbar" interconnect. see e.g. '496 patent (CX-6, col. 16, ln 5 - col. 18, ln. 28; col. 22, ln. 45 - col. 24, ln. 16). Moreover, in a June 29, 1993 amendment submitted during prosecution of the '496 patent, which introduced patent claims 1, 2, 3 and 15 in issue, applicants argued that:

> The so-called 'partial crossbar' connectivity scheme for connecting FPGAs in Applicants' logic emulation system is set forth in each of the new claims.

(FF 421). In a September 14, 1994 "amended information disclosure statement," submitted during prosecution of the '496 patent, applicants argued:

> Applicants have invented a new and highly useful connectivity scheme for a hardware logic emulation system, wherein reprogrammable logic devices capable of implementing the functional logic components of a digital logic circuit design undergoing emulation are interconnected to one another via a novel 'partial crossbar' architecture. Applicants' partial crossbar architecture employs a combination of reprogrammable interconnect device and fixed electrical conductors arranged such that each interconnect device is connected to at least

> one but not all of the I/O terminals of the logic devices. The connection paths established through the logic device I/Os, fixed electrical conductors and reprogrammable interconnect devices for a given digital logic circuit design undergoing emulation are circuit-switched paths as opposed to message-switched paths. Hence, the connection paths are dedicated to one source I/O and its destination I/O(s) in static fashion, meaning the same paths are used between the source and destination I/Os for the entire connection lifetime.
>
> * * *
>
> An electrically reconfigurable logic assembly incorporating Applicants' unique partial crossbar architecture is defined most broadly in independent claim 19 [patent claim 1]. The elements of claim 19 include reprogrammable logic devices with functional logic elements, reprogrammable interconnect devices and fixed electrical conductor arranged in a partial crossbar configuration for electrically connecting the reprogrammable logic devices to one another through the reprogrammable interconnect devices. Applicants' independent claim 33 [patent claim 15] adds an interface structure to the reconfigurable logic assembly of claim 19. . . .

(FF 445) (emphasis added). Also, the examiner in his February 16, 1995 "Examiner's Statement of Reasons for Allowance" in the '496 prosecution history, states:

> During the 10 August 1994 interview, applicants' representative repeatively [sic] stated that the claimed invention is directed to an electrically reconfigurable logic assembly incorporating the unique **partial crossbar architecture** in a hardware [sic] logic **emulation system**. The examiner agrees that the prior arts of record fail to specifically disclose such a unique claimed **partial crossbar architecture** for use in a hardware [sic] logic emulation system.

(FF 446) (emphasis in original). Thus, the administrative law judge finds that each of the claims of the '496 patent are directed to the "partial crossbar" interconnect.

ii. "logic assembly"

The preamble of claim 1 directs the claim to a "logic assembly" (FF 415). Respondents argued that "the 'assembly' claimed is a logic board [which would include all the chips on the board] and that part of a logic board [with not all the chips] would not be an 'assembly'" (RBr at 14) and that this reading is based on the "ordinary" meaning of

assembly as a "complete set of some type of parts" (RFF 260-263). It is also argued that this reading is necessary to distinguish the '496 patent claims from U.S. Patent No. 5,109,353 (the '353 patent) [29] (RBr at 26-30). Complainant and the staff argued that the term is not so limited. Rather, they would read the claim term "assembly" on less than all of the chips on a board. (CBr at 44-45, SBr at 25-29).

While the preamble of claim 1 does direct that claim to a "logic assembly" (FF 413), generally the preamble "does not limit the claims . . . [unless it is] necessary to give meaning to the claim and properly define the invention." Robert L. Harmon, "Patents and the Federal Circuit," § 5.6, pg 182 (3rd ed. 1994), see also 2 Chisum, Patents, § 8.06[1](d). The meaning of the claim term "assembly" is defined in mechanical terms as "[a] unit containing the component parts of a mechanism, machine, or similar device." *McGraw-Hill Dictionary of Scientific and Technical Terms* 133 (4th ed. 1989). (See SBr at 14-15). The term "assembly" is further defined as:

> (2) (electric and electronics parts and equipments). A number of basic parts or subassemblies, or any combination thereof, joined together to perform a specific function. The application, size, and construction of an item may be factors in determining whether an item is regarded as a unit, an assembly, a subassembly, or a basic part. A small electric motor might be considered as a part if it is not normally subject to disassembly. The distinction between an assembly and a subassembly is not always exact: an assembly in one instance may be a subassembly in another where it forms a portion of an assembly.

IEEE Standard Dictionary of Electrical and Electronics Terms, 57 (3rd ed. 1984). See RRFF42; CFF93 and 94; SFF83. Those dictionary definitions, relied on by all the parties,

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[29] The '353 patent was considered by the examiner in the prosecution of the '496 patent (FF 412). The '353 patent entitled "Apparatus for Emulation of Electronic Hardware System" issued on April 28, 1992 from Application Number 279,447 filed on December 2, 1988. The named inventors are Stephen P. Sample, Michael R. D'Amour, and Thomas S. Payne (FF 466).

establish that the term "logic assembly" does not define any specific structure, such as a logic board. As structure is defined by the remainder of claim 1 of the '496 patent, the administrative law judge does not find the term "assembly" "necessary to give meaning to the claim and properly define the invention." see e.g. Marston v. J.C. Penney Co., 353 F.2d 976, 148 USPQ 25 (4th Cir. 1965), cert. denied, 385 U.S. 974 (1966); DeGeorge v. Bernier, 226 USPQ 758, 761 (Fed. Cir. 1985). Hence, the administrative law judge finds that the phrase "logic assembly" does not act as a claim limitation.

Moreover, in light of the specification, prosecution history and other claims of the '473 patent, the term "logic assembly" cannot be limited to a "logic board." Thus, while the claim term "logic assembly" is not defined in the specification of the '496 patent (FF 422), the specification teaches single circuit board "assemblies" which contain each of the elements of claim 1 in issue, as well as multi-board "system-level" interconnections where "the partial crossbar interconnect [is reapplied] hierarchically, treating each board as if it were a logic chip. . ." (FF 432). The administrative law judge finds no language in the specification or the prosecution history to indicate that claim 1 and claim 15 in issue are limited to only those "assemblies."

Independent claim 18 of the '496 patent, not in issue, is limited to a logic board, as seen from the following portion of the claim:

> An electrically reconfigurable logic board for use in an electrically reconfigurable hardware emulation system . . . said electrically reconfigurable logic assembly comprising:
>
> a logic board structure
>
> * * *

(FF 419). Claim 20 of the '496 patent reads in part (col. 9, lines 22 to 26):

> An electrically reconfigurable hardware emulation system for emulating a digital logic network design, which digital logic network design can be represented by design data, said electrically reconfigurable hardware emulation system comprising:

(FF 420). As claim 18 is expressly limited to a "logic board" and claim 20 is expressly limited to an entire "system," the administrative law judge further finds it improper to read either of those limitations into the claim 1 term "logic assembly." See 4 Chisum, Patents at § 18.03[2].

Referring to the prosecution of the '496 patent, in a June 29, 1993 amendment which added patent claim 1, applicants argued that:

> Claim 19 [patent claim 1] . . . defines the electrically reconfigurable logic assembly which forms the basic hardware component in the preferred embodiment of the novel reconfigurable hardware emulation system which is the subject of the '734 application. The claim elements include 'reprogrammable logic devices' with functional elements, 'reprogrammable interconnect devices' and a 'partial crossbar' connectivity scheme with 'fixed electrical conductors' or electrically connecting the reprogrammable logic devices to one another via the reprogrammable interconnect devices.

(FF 445). There was no suggestion that patent claim 1 (application claim 19) is limited to an entire logic board, as argued by respondents. Applicants, in the '496 patent prosecution further argued with respect to patent claims 17 and 18 of the '496 patent (application claims 35 and 36):

> Claim [17] is a more detailed version of Claim [1]. The reprogrammable logic devices of Claim [1] are specifically defined as 'logic FPGAs' and the reprogrammable interconnect devices of Claim [1] are specifically defined as 'interconnect FPGAs'.
>
> * * *

> Claim [18] defines an electrically reconfigurable logic board which includes all of the detailed elements recited in Claim [17] mounted on a 'logic board structure.'

(FF 426). Hence, each of patent claims 17 and 18 were argued to be "more detailed versions" of claim 1, wherein claim 18 requires a "logic board structure" as part of "said electrically reconfigurable logic assembly" (FF 419), which further shows that a "logic assembly" of claim 1 may include a "logic board structure," but is not limited to a logic board structure.

Respondents' argument that the term "assembly" requires the claim to read on every chip on a logic board is also found not to be supported by the testimony of respondents' technical expert Wolfe. Specifically, he testified that:

> There are often going to be programmable gate array chips on this board that do not participate in the emulation and perform other functions on the board, and I don't think that has any effect on whether or not this is a reconfigurable logic assembly.

(FF 427). Accordingly, in view of both the prosecution history and specification of the '496 patent, other claims of the '496 patent and testimony of respondents' own technical expert, the administrative law judge finds that the "assembly" of claim 1 is not limited to at least a "logic board."[30]

iii. "a plurality of reprogrammable logic devices"

[30] Respondents argued that one could select a subset of chips from the logic board taught by the '353 patent, and that claim 1 of the '496 patent would read on that subset of chips (RBr at 30). The administrative law judge finds the '353 patent distinct from claim 1 of the '496 patent for reasons other than the term "assembly." See section 3 a. i. and 3 b. iii., infra.

Each of independent claims 1 and 15 contains the phrase "a plurality[31] of reprogrammable logic devices." The phrase "reprogrammable logic devices" is not expressly defined in the specification of the '496 patent (FF 428). Respondents argued that the term "reprogrammable logic devices" "can only correspond to the logic chips and the ERCGA's of the specification." (RFF 210, Tr. at 4727). In support, respondents argued that the "specification talks about logic chip devices and interconnect chip devices and in no way describes a logic device or an interconnect device as being . . . an entire board, which contains multiple logic chip devices and interconnect chip devices." (RBr at 36). Complainant argued that the phrase "reprogrammable logic devices" can include "collections of discrete chips." (CFF 98, Tr. at 4725).

The '496 patent specification defines a "logic chip" as "an ERCGA used to realize the combinational logic, storage and interconnections of an input design in the Realizer system" (FF 429). The specification further teaches, with respect to "Logic Chip Devices:"

> For a device to be useful as a Realizer logic chip, it should be an electronically reconfigurable gate array (ERCGA):
>
> 1) It should have the ability to be configured according to any digital logic network consisting of combinational logic (and optionally storage), subject to the capacity limitations.
>
> 2) It should be electronically reconfigurable, in that its function and internal interconnect may be configured electronically any number of times to seek many different logic networks.
>
> 3) It should have the ability to freely connect I/O pins with the digital network, regardless of the particular network or which I/O pins are specified, to allow the Realizer System partial crossbar or direct interconnect to successfully interconnect logic chips.

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[31] In the context of the claims in issue, it is undisputed that the "plurality" element merely requires the presence of two or more reprogrammable logic devices.

(FF 430). The specification further contains a description of "Partial Crossbar System-Level Interconnects." Under the "system-level" description, the specification teaches:

> One means of interconnecting logic boards is to reapply the partial crossbar interconnect hierarchically, treating each board as if it were a logic chip, and interconnecting board I/O pins using an additional set of crossbar chips.

(FF 432). The preferred embodiment of the '496 patent employs such a "system-level" interconnect:

> The partial crossbar interconnect is used hierarchically at three levels across the entire hardware system.
>
> A logic board consists of up to 14 logic chips, with 128 interconnected I/O pins each, and an X-level partial crossbar composed of 32 Xchips. Each Xchip has four paths to each of the 14 Lchips (56 total), and eight paths to each of two Ychips, totaling 512 logic board I/O pins per board.
>
> A box contains one to eight boards, with 512 interconnected I/O pins each, and a Y-level partial crossbar composed of 64 Ychips. Each Ychip has eight paths to an Xchip on each board via logic board I/O pins, and eight paths to one Zchip, totaling 512 box I/O pins per box.
>
> A rack contains one to eight boxes, with 512 interconnected I/O pins each, and a Z-level partial crossbar composed of 64 Zchips. Each Zchip has eight paths to a Ychip in each box via box I/O pins.

(FF 432). Thus, the specification does disclosed multiple chip logic boards treated "as if it were a logic chip."

In addition, the dictionary meaning of a "device" is:

> (comut. sci.) A general-purpose term used, often indiscriminately, to refer to a computer component or the computer itself.

McGraw-Hill Dictionary of Scientific and Technical Terms 133 (4th ed. 1989). The administrative law judge finds nothing in either the specification, the prosecution history, or the express claim language of claims 1 and 15 that would limit a "reprogrammable logic

device" to a "reprogrammable logic chip." Accordingly, he finds that the claim phrase "reprogrammable logic device" may encompass a group of discrete chips.

iv. "reprogrammable logic devices having . . . programmable I/O terminals which can be reprogrammably connected to selected ones of said functional elements"

Respondents argued that the "reprogrammable logic devices" of claim 1 and claim 15 must have "programmable I/O terminals" through which each functional element (BLP) can "be arbitrarily connected to any I/O pin on that chip. . . ." (RBr at 35-36). In support, respondents argued that the specification teaches that a "logic chip device" should have the ability to freely connect every I/O pin with any given functional element configured into said logic device, regardless of the particular functional element or I/O pin specified (RBr at 35). Complainant argued that "a 'programmable I/O terminal' within the meaning of claim 1 can connect to any subset of functional elements within the reprogrammable logic device." (CRBr at 9). The staff argued that "the claims at issue only require that the I/O pins be capable of connecting to selected functional elements." (SBr at 18) (emphasis in original).

The express language of claim 1 requires ". . . programmable I/O terminals which can be reprogrammably connected to selected ones of said functional elements ..." (emphasis added). Thus, claim 1 is not limited such that every I/O terminal must have the ability to freely connect to every functional element. While the specification does teach that a logic chip "should have the ability to freely connect I/O pins with the digital network, regardless of the particular network or which I/O pins are specified" (FF 429) and further teaches, with respect to the partial crossbar interconnect:

> The logic chip itself can offer an additional degree of freedom which crossbars do not exploit, because it has the ability to be configured to use any of its I/O

> pins for a given input or output of the logic network it is being configure for, regardless of the particular network. That freedom allows the possibility of the partial crossbar interconnect, which is the reason it is specified in the definition of the logic chip.
>
> * * * *
>
> . . . . Since the logic chip can be configured to use any I/O pin [that] may be assigned to the logic configured in a logic chip which is connected to a net, one I/O pin is as good as another.

(FF 434), significantly the specification also teaches the use of an electrically erasable programmable logic device (EEPLD) as a logic chip:

> Still another type of reconfigurable logic chip which could be used as a logic chip is the EEPLD. . . . A commercial example is the Lattice Generic Array Logic (GAL). . . . It offers freedom of connection of I/O pins to logic only among all input pins and among all output pins, so it partially satisfies that requirement. . . . It can, however, be used as a Realizer logic chip.

(FF 437). Hence, there is a teaching in the specification that complete freedom of connection is not required (FF 436, 437). Claim terms are to be construed in light of the specification. Respondents would read a feature of the preferred embodiment (i.e. the ability of a Xilinx FPGA to freely interconnect any I/O to any functional element) into claims 1 and 15 in issue (FF 435). This narrowing is improper, see e.g. Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 1571, 7 USPQ 1057, 1064 (Fed. Cir. 1988). Accordingly, the administrative law judge finds that the phrase "reprogrammable logic devices having . . . programmable I/O terminals which can be reprogrammably connected to selected ones of said functional elements" does not require complete interconnectivity between every I/O pin and every functional element.

v. "a plurality of reprogrammable interconnect devices"

Each of independent claims 1 and 15 contain the phrase "a plurality of reprogrammable interconnect devices." Respondents argued, with respect to the phrase "plurality[32] of reprogrammable interconnect devices" in claim 1 that "if an integrated circuit contains the reprogrammable interconnect between I/O terminals as described in the claim, it is an interconnect device, regardless of any other function it may perform." (RBr at 14) (emphasis in original). Complainant argued that "reprogrammable interconnect devices are devices which have been segregated from the logic devices in order to perform interconnect functions." (CFF 106). The staff argued that the "'reprogrammable interconnect devices" is "described in the claim as 'having I/O terminals and internal circuitry which can be reprogrammably configured to provide interconnections' between selected combinations of those I/O terminals." (SBr at 18).

In issue is whether a "reprogrammable interconnect devices" in the phrase "a plurality of reprogrammable interconnect devices" may "contain logic." The phrase "reprogrammable interconnect device" is not expressly defined in the specification. However, the specification describes "interconnect chip devices" as follows:

> Interconnect chips include crossbar chips, used in full and partial crossbar interconnects, and routing chips, used in direct and channel-routed interconnects. For a device to be useful as a Realizer interconnect chip:
>
> 1) It should have the ability to establish many logical interconnections between arbitrarily chosen groups of I/O pins at once, each interconnection receiving logic signals from its input I/O pin and driving those signals to its output I/O pin(s).
>
> 2) It should be electronically reconfigurable, in that its interconnect is defined electronically, and may be redefined to suit many different designs.

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[32] It is undisputed that the term "plurality" requires the presence of two or more reprogrammable interconnect devices.

> 3) If a crossbar summing technique is used to interconnect tri-state nets in the partial crossbar interconnect, it should be able to implement summing gates. (If not, other tri-state techniques are used, as discussed in the tri-state section.)
>
> The ERCGA devices discussed above, namely the LCA, the ERA and the EEPLD, satisfy these requirements, so they may be used as interconnect chips. Even though little or no logic is used in the interconnect chip, the ability to be configured into nearly any digital network includes the ability to pass data directly from input to output pins.

(FF 440). Thus, the specification teaches that "interconnect chips" may be physically identical to "logic chips." In the preferred embodiment, the interconnect chips are the same Xilinx FPGAs used as logic chips (FF 440). The distinction between a "logic chip" and an "interconnect chip" is the function assigned by the system software, i.e. that the interconnect chip uses "little or no logic" (FF 440). When an "interconnect chip" does implement logic, however, the specification teaches a specific purpose for this logic:

> The crossbar chip must have one or more logic elements for the summing gate. Crossbar summing deviates from the practice of putting all logic in the logic chips and none in the crossbar chips, but an important distinction is that the logic placed in the crossbar chip is not part of the realized design's logic. It is only logic which serves to accomplish the interconnection functionality of a tri-state net.

(FF 441).

In light of the claim language, as well as the specification, the administrative law judge finds that an "interconnect devices" in the phrase "a plurality of reprogrammable interconnect devices" are devices with the functionality called for in the claims, viz. "having I/O terminals and internal circuitry which can be reprogrammably configured to provide interconnections between selected ones of said I/O terminals." He further finds that, although said "interconnect devices" may have logic functionality, that logic functionality is limited to that which serves to accomplish interconnection functionality.

vi. **"connecting said programmable I/O terminals on said reprogrammable logic devices to said I/O terminals on said reprogrammable interconnect devices such that each of said reprogrammable interconnect devices is connected to at least one but not all of said programmable I/O terminals on each of said reprogrammable logic devices."**

Each of independent claims 1 and 15 contain the phrase:

> "connecting said programmable I/O terminals on said reprogrammable logic devices to said I/O terminals on said reprogrammable interconnect devices such that each of said reprogrammable interconnect devices is connected to at least one but not all of said programmable I/O terminals on each of said reprogrammable logic devices." [Emphasis added]

(FF 415, 418). Respondents argued that this language requires that every interconnect device on a logic board must be connected to every logic device on a logic board (RBr at 31). Complainant and the staff argued that each of claims 1 and 15 may be read on a subset of chips (SBr at 25-30, CBr at 38-39, 42).

The phrase in issue requires a fixed wire connection between at least one I/O terminal on each "reprogrammable interconnect device," and at least one but not all the I/O terminals on each "logic device." During prosecution of the '496 patent, applicants argued that:

> An electrically reconfigurable logic assembly incorporating Applicants' unique partial crossbar architecture is defined most broadly in independent claim 19 [issued claim 1]. The elements of claim [1] include reprogrammable logic devices with functional logic elements, reprogrammable interconnect devices and fixed electrical conductor arranged in a partial crossbar configuration for electrically connecting the reprogrammable logic devices to one another through the reprogrammable interconnect devices.

(FF 445). In issue is whether "said reprogrammable interconnect devices" as emphasized in the introductory portion of this section are all interconnect chips on a logic board, or if the claim can read on only a selected group of interconnect devices on a logic board, without considering additional "interconnect devices" that are not connected to each "logic device."

The claimed phrase in issue relates back to said "plurality of reprogrammable interconnect devices," and said "plurality of reprogrammable logic devices," see section iii., iv. and v., supra. The administrative law judge has previously found that claim 1 is not limited to "at least an entire logic board" as argued by respondents (see section ii., supra). Thus, claim 1 and claim 15 simply require each of two or more "interconnect devices" connected to at least one but not all pins of each of two or more "logic devices."

vii. "programmable gate arrays"

Claim 2 further limits claim 1 by requiring that "said reprogrammable logic devices comprise programmable gate arrays." (FF 416). Complainant argued that the phrase "programmable gate arrays" should "be broadly construed to cover integrated circuit devices, whether commercially available or custom-built, which provide an array of programmable logic resources and some interconnecting facility." (CFF 109). Respondents apparently argued that the claimed phrase in issue, "programmable gate arrays" should have I/Os that "can be tri-state buffers or bi-directional buffers." (RFF 66)[33]

The phrase "programmable gate arrays" is not defined in the specification of the '496 patent. However, the term "electronically reconfigurable gate array" or "ERCGA" is defined as:

> a collection of combinational logic, and input/output connections (and optionally storage) whose functions and interconnections can be configured and reconfigured many times over, purely by applying electronic signals.

---

[33] In response to CFF109, which presents complainant's interpretation of the phrase "programmable gate arrays," respondents objections are primarily directed to a comparison of features found in the Meta 128 chip to features of "commercial FPGAs" see RO 109, RFF 65, 66, and RRFF 54. However, it is unclear what definition respondents would give to the claim term "programmable gate arrays."

(FF 451). The administrative law judge finds that the phrase "programmable gate arrays" is defined by the definition of "ERCGAs" found in the specification. He finds no support in the claim language, specification, or prosecution history for respondents' argument that "programmable gate arrays" must have I/O pins that can be programed as "tri-state buffers or bi-directional buffers."

viii. "FPGAs"

Claim 3 further limits claim 1 such that "reprogrammable logic devices comprise FPGAs." Complainant argued that "FPGA" was a "field programmable gate array" and should be construed to cover "integrate [sic] circuit devices, whether commercially available or custom-built, which provide an array of logic resources and some interconnecting facility which can be programmed after the devices are manufactured." (CFF 111). Respondents argued that "one of ordinarily [sic] skill in that art would know that an FPGA is a general purpose, not a custom-built chip (RO 111).

The term "FPGA" is not expressly defined in the specification of the '496 patent. The examiner originally questioned whether the specification supported claims specifically drawn to the use of FPGA devices (FF 452). Applicants, during the prosecution of the '496 patent, argued that:

> [i]n a preferred embodiment of Applicants' invention, the ERCGAs are Xilinx XC3090 LCA chips. At the time Applicants' priority application was filed (on October 5, 1988), Xilinx LCAs were also known to those of ordinary skill in the art as FPGAs.

(FF 452). Hence, the description of the Xilinx LCA in the specification is the disclosure of an FPGA. A Xilinx LCA is described in the specification at col. 7, lines 61 to col. 8 line 20 as:

> An example of a reconfigurable logic chip which is suitable for logic chips is the Logic Cell Array (LCA) ("The Programmable Gate Array Handbook", Xilinx, Inc., San Jose, Calif., 1989). It is manufactured by Xilinx, Inc., and others. This chip consists of a regular 2-dimensional array of Configurable Logic Blocks (CLBs), surrounded by reconfigurable I/O Blocks (IOBs), and interconnected by wiring segments arranged in rows and columns among the CLBs and IOBs. Each CLB has a small number of inputs, a multi-input combinational logic network, whose logic function can be reconfigured, one or more flip-flops, and one or more outputs, which can be linked together by reconfigurable interconnections inside the CLB. Each IOB can be reconfigured to be an input or output buffer for the chip, and is connected to an external I/O pin. The wiring segments can be connected to CLBs, IOBs, and each other; to form interconnections among them, through reconfigurable pass transistors and interconnect matrices. All reconfigurable features are controlled by bits in a serial shift register on the chip. Thus the LCA is entirely configured by shifting in the "configuration bit pattern", which takes between 10 and 100 milliseconds. Xilinx 2000 and 3000-series LCA's "FPGAs" have between 64 and 320 CLBs, with between 56 and 144 IOBs available for use.

(FF 453). Thus, the administrative law judge finds that the term "FPGA" has what is described at col. 7, line 61 to col. 8, line 20 of the '496 patent (CX-6).

ix. "an interface structure arranged to provide signal paths for signals carrying information to or from designated ones of said functional elements in said reprogrammable logic devices"

Claim 15 has virtually the same language as claim 1. However, it also requires "an interface structure arranged to provide signal paths for signals carrying information to or from designated ones of said functional elements in said reprogrammable logic devices" (FF 455). Complainant argued that "the interface structure of claim 15 is a structure which enables the hardware logic emulation system of the '496 patent to interface with external systems for the purpose of exchanging signals." (CFF 113). Respondents argued that the term "interface structure" is "indefinite and undefined in the '496 patent." (RO 113). The staff argued that the "'496 patent specification describes an interface for user-supplied

devices and a preferred embodiment . . . and also describes I/O connections from the interface to the logic devices." (SBr at 21).

The '496 patent does not expressly define the phrase "an interface structure arranged to provide signal paths for signals carrying information to or from designated ones of said functional elements in said reprogrammable logic devices." The specification however does teach a "user-supplied device module" which performs the following functions:

> The user-supplied device module:
>
> 1) Provides a means of physically connecting user-supplied hardware devices.
> 2) Provides connections between the USDs and Realizer system logic and/or interconnection chips. Since the USDs fulfill roles in the design similar to logic chips, it is expedient to interconnect USDMs in the same way as logic chips.
> 3) Provides the ability to freely assign USD pins to interconnect pins, as the logic chips normally installed in the LChip location do.

(FF 456). In addition, the specification teaches:

> Each MA and MD logic chip has some I/O pins connected to the terminal block, and some connected to the interconnect. These chips are connected to the interconnect in the same manner described for memory module address and data path logic chips. Optionally, they may also be connected to the host interface bus and/or a common control bus, for purpose similar to their uses in memory modules, as shown.

(FF 456). Thus, the specification details that a "user-supplied device module" performs the function of the "interface structure" of claim 15 of the '496 patent. The administrative law judge finds that claim 15 requires a user-supplied device, as described in the '496 specification, which is arranged to "provide signal paths for signals carrying information to or from designated ones of said functional elements in said reprogrammable logic devices."

3. Validity Assuming No Assignor Estoppel

Respondents have argued that the asserted claims of the '473 patent and the '496 patent are invalid as "anticipated and made obvious" by the '353 patent and by the Xilinx XACTOR system. Respondents also rely on publication by Clos and Spandorfer in arguing the obviousness of the '473 and '496 patents (RBr at 39-46). Complainant argued that the '353 patent, as a matter of law, is not prior art under 35 U.S.C. § 102. (CRBr at 21). In addition, complainant argued that respondents' "validity argument is suffused with hindsight reconstruction of the prior art." (CRBr at 23). The staff argued that the claims at issue have not been shown invalid in light of the prior art (SRBr at 13).

Under 35 U.S.C. § 282, a patent is presumptively valid, and the heavy burden of proving invalidity rests squarely on the accused infringer. The accused infringer bears the burden by the significantly heightened standard of "clear and convincing evidence" to establish invalidity. Texas Instruments v. U.S. Intern. Trade Comm'n, 988 F.2d 1165, 1177, 26 USPQ.2d 1018, 1028 (Fed. Cir. 1993), Intel Corp., 946 F.2d at 834, 20 USPQ.2d at 1172. However, in the context of a motion for temporary relief, the statutory presumption of validity does not relieve a patentee who moves for temporary relief from carrying the normal burden of demonstrating that it will likely succeed on the merits. See Braiding, 970 F.2d at 882, 23 USPQ2d at 1626. On a motion for temporary relief, the patentee must show that the "alleged infringer's defense lacks substantial merit." Id.

a. 35 U.S.C. § 102

Anticipation "requires identity of invention: the claimed invention, as described in appropriately construed claims, must be the same of that as the reference, in order to anticipate." Glaverbe Societe Anonyme v. Northlake Marketing, 45 F.3d 1550, 1554, 33

USPQ.2d 1496, 1498 (Fed. Cir. 1995) (Glaverbe), Continental Can Co. USA, Inc. v. Monsanto Co., 948 F.2d 1264, 1267, 20 USPQ.2d 1746, 1748 (Fed. Cir. 1991). Further, the alleged anticipating reference must be enabling. In re Spada, 911 F.2d 705, 708, 15 USPQ.2d 1655, 1657 (Fed. Cir. 1990) ("The reference must describe the applicant's claimed invention sufficiently to have placed a person of ordinary skill in the field of the invention in possession of it".) References must be accepted for what they actually teach, not for what they could have taught in hindsight. Panduit Corp. v. Dennison Mfg., Co., 774 F.2d at 1095, 227 USPQ at 345-46 (Fed. Cir. 1985) (Panduit). Anticipation is a question of fact. Glaverbe Societe Anonyme, 45 F.3d at 1554, 33 USPQ.2d at 1498, Shatterproof Glass Corp. v. Libby-Owens Ford Co., 758 F.2d 613, 619, 225 USPQ 634, 637 (Fed. Cir. 1985).

i. The '473 And '496 Patents

In issue is whether the '353 patent is prior art (CBr at 26, RRBr at 15). Under 35 U.S.C. § 102(e) a patent is invalid if "the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent. . . ." (emphasis added). A patent becomes a reference under 35 U.S.C. § 102(e) only as of the patent's filing date, not on the date of conception or actual reduction to practice, Sun Studs, Inc. v. ATA Equip. Leasing, Inc., 872 F.2d 978, 983-4, 10 USPQ2d 1338, 1343 (Fed. Cir. 1989). The '353 patent issued from an application filed on December 2, 1988 (FF 466), while each of the '473 and '496 patents issued from an application filed on October 5, 1988 (FF 382, 412). Hence, pursuant to 35 U.S.C. § 102(e), the '353 patent would not be a reference.

"Amended Information Disclosure Statement" stated that the Sample '353 patent constitutes prior art because Sample et. al. conceived and reduced to practice prior to the applicants' conception of their partial crossbar structure. What was conceived and reduced to practice by Sample et. al. was a prototype logic emulation board. In view of the foregoing, the administrative law judge finds that respondents' are unlikely to succeed in establishing that the '353 patent is an effective reference under § 102(e) or § 102(g). However, in view of complainant's admission in the September 24, 1994 "Amended Information Disclosure Statement" taken with the actual conception and reduction of practice of the prototype logic emulation board (FF 468, 469, 472), respondents are likely to succeed in establishing the Sample et al. prototype, which is disclosed in the '353 patent, is prior art under §102(g).

Respondents rely on the Sample et al. prototype device (Rapid Prototyping Machine or RPM) which was first tested on [ ] filing date of the '473 patent (RRBr at 16). The entire '353 patent, including the RPM prototype, was before the examiner of the '496 patent (FF 414). It is undisputed that the RPM device is prior art (CBr at 25-26). The Sample et al. RPM device contained [ ]of Xilinx FPGAs connected using a "nearest-neighbor" architecture (FF 470). In the RPM device, there were[

](FF 469). In the RPM device, there was no FPGAs designated exclusively for either interconnect or logic functions. Each FPGA performed a mixed interconnect and logic function (FF 479, 475). Contemporaneous evidence demonstrates that each FPGA used at least some logic functions (FF 470, 478, 479).

Respondents further rely on the "XACTOR in circuit emulator," described in an article by Pardner Wynn, entitled "Designing With Logic Cell Arrays," as well as the 1986 Programmable Gate Array Book at 4-27 to 4-28 (RBr at 40). The Xilinx XACTOR device, as described in the 1986 Programmable Gate Array Book, at 4-27 to 4-28, was before the examiner of the '473 patent and the examiner of the '496 patent (FF 384, 414). The XACTOR is described as a PC based in-circuit emulator, using Xilinx FPGAs, permitting real time in-circuit emulation of up to four LCAs (FPGAs) simultaneously (FF 491). The XACTOR did not provide an interconnection between or among its FPGAs and none of the FPGAs were dedicated exclusively to either an interconnect or logic function (FF 492).

(a) Claim 8 Of The '473 Patent

Claim 8 of the '473 patent requires "at least one reconfigurable interconnect ERCLC(s)" that is "dedicated only to accomplishing interconnections," and any logic contained thereon must only serve to accomplish interconnection functionality. See "Claim Construction ('473 Patent)," section 2 a. vi., supra. The administrative law judge finds that a "reconfigurable interconnect ERCLC" is not disclosed by the Sample et al. RPM, either expressly or inherently[35] as seen from the description of the Sample et al. RPM, supra.

[35] Even accepting respondents' argument that the entire '353 patent is "prior art" under 35 U.S.C. § 102, that patent does not anticipate claim 8 of the '473 patent. Respondents have relied on an "illustrative" 3 x 3 array of FPGAs, as shown in Fig. 1b of the '353 patent, as well as the 2 x 2 array of FPGAs shown in Fig. 2 of the '353 patent, and their accompanying text. None of the FPGAs taught in the '353 patent are either a "reconfigurable interconnect ERCLC(s)" that is "dedicated only to accomplishing interconnections," with any logic contained thereon serving to accomplish interconnection functionality, as required by claim 8 of the '473 patent. Similarly, the '353 patent does not teach an "interconnect device" that is "dedicated only to accomplishing interconnections," with any logic contained thereon serving to accomplish interconnection functionality, as required by claims 1 and 15 of the '496 patent. Thus, assuming arguendo the entire '353 patent is "prior art" under 35 U.S.C. § 102, the administrative law judge finds that respondents are unlikely to succeed in establishing that either of the '473 or '496 patent claims in issue are

Similarly, he finds that the Xilinx XACTOR does not disclose a "reconfigurable interconnect ERCLC" as also seen from the description of the XACTOR, supra. Thus, he finds that respondents are unlikely to succeed in establishing that claim 8 of the '473 patent is invalid under 35 U.S.C. § 102 as anticipated by either the Sample et al RPM or the Xilinx XACTOR.

b. Claim 1, 2, 3 And 15 Of The '496 Patent

Each of independent claims 1 and 15 of the '496 patent require a plurality of "interconnect devices," "having I/O terminals and internal circuitry which can be reprogrammably configured to provide interconnections between selected ones of said I/O terminals." An "interconnect device" within the meaning of independent claims 1 and 15 may have logic functionality, however, that logic functionality is limited to that which serves to accomplish interconnection functionality, see "Claim Construction ('496 Patent)" section b. v., supra. The administrative law judge finds that the Sample et al. RPM device does not disclose an "interconnect device" within the meaning of claim 1 and claim 15 of the '496 patent, either expressly or inherently. Similarly, he finds that the Xilinx XACTOR does not disclose the claimed "interconnect device." Thus, he finds that respondents are unlikely to succeed in establishing that any of claims 1, 2, 3 or 15 are invalid under 35 U.S.C. § 102 as anticipated by the Sample et al. RPM prototype, or the Xilinx XACTOR.

b. 35 U.S.C. § 103

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anticipated by the '353 patent.

Respondents argued that the claims in issue of the '473 and '496 patents are "made obvious" under 35 U.S.C. § 103 by certain references. A patent is invalid under 35 U.S.C. § 103 if:

> the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Id. The test for obviousness requires four factual determinations, namely (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, such as commercial success, copying, or long-felt need. Graham v. John Deere Co., 383 U.S. 1, 17 (1966) (Graham); See also Glaverbe, 45 F.3d at 1555, 33 USPQ2d at 1499.

References in combination must suggest the invention as a whole. Absent a suggestion to combine references, one can do no more than piece the invention together using the patented invention as a template, which hindsight reasoning is impermissible. Texas Instruments v. U.S. Int'l Trade Comm'n, 988 F.2d 1165, 1178, 26 USPQ2d 1018, 1029 (Fed. Cir. 1993). Panduit, 774 F.2d at 1095, 227 USPQ at 348.

i. Scope And Content Of The Prior Art

The term "prior art" within the meaning of 35 U.S.C. § 103 is generally restricted to those things defined under 35 U.S.C. § 102. Chisum, Patent § 5.03[3][g][I]; see e.g. In re McKellin, 529 F.2d 1324, 1330, 188 USPQ 428, 433, (CCPA 1976) but see In re Fout, 675 F.2d 297, 300, 213 USPQ 532, 534 (CCPA 1982) (Party admissions are also a source of section 103 prior art).

Respondents, in support of its obviousness contentions with respect to the '473 and '496 patents, in their post hearing brief has relied on (1) the '353 patent, (2) the Xilinx XACTOR, and (3) the "Clos network". Each of the Sample et al. RPM and the XACTOR were described in "The '473 And '496 Patents" section 3 a. i. supra. The '353 patent has not been found to be prior art, but the Sample et al. RPM has been found to be prior art. Respondents, in certain proposed findings, cited a Schmitz article and two Wynn articles.

Clos Network

Respondents rely on a March, 1953 article by Clos, entitled "A Study of Non-Blocking Switching Networks," published in the Bell System Technical Journal, Vol. 32, No. 2 (RBr at 46). Respondents refer to the "partial crossbar" of the '473 patent as a "degraded Clos network." Id. The Clos article describes:

> a method of designing arrays of crosspoints for use in telephone switching systems in which it will always be possible to establish a connection from an idle inlet to an idle outlet regardless of the number of calls served by the system.

(FF 505). In addition, an October 31, 1965 Spandorfer report entitled "Synthesis of Logic Functions on an Array of Integrated Circuits" discloses the use of a Clos type switching network for connecting macrocellular arrays of logic gates to one another (FF 506). The Clos network is designed to make connections from one output to one input (FF 511). Respondents have referred to the combination of those articles as disclosing the "Clos network." (RBr at 44).

The Schmitz Article

The Schmitz article entitled "Emulation of VLSI Designs Using LCAs," was published on May 20, 1987 in VLSI Systems Design. The Schmitz article discloses four gate arrays,

including two LCAs and two PALs, connected using wrapped wire technology, for prototyping a design (FF 496, 497).

The Wynn Articles

The Wynn article, entitled "In-Circuit Emulation of ASIC-Based Designs," was published in VLSI Systems Design in October, 1986. That article teaches the use of Xilinx LCAs (FPGAs) to emulate the design of an application specific integrated circuit (ASIC) (FF 494). Specifically a single FPGA would be used in an emulation "pod" with up to four "pods" contemplated (FF 495). There was no connection between the FPGAs in the four emulation "pods," other than that provided by a target system (FF 492).

The Wynn article, entitled "Designing With Logic Cell Arrays," describes the structure and function of the Xilinx 2000 series FPGAs, also known as LCAs. That article compares custom chips versus off-the-shelf programmable chips. The Wynn article "Designing With Logic Cell Arrays" also taught an "XACTOR" emulator (FF 487, 488).

ii. Differences Between The Prior Art And The Claims At Issue ('473 Patent)

The prior art relied on by respondents falls under two general classes: (1) art which suggests the use of FPGAs to emulate circuit designs (Sample et al RPM, Wynn Articles, Schmitz Article), and (2) non-blocking networks (Clos article and Spandorfer report).

With respect to the Sample et al. RPM device, complainant has admitted that claim 6 of the '473 patent "was disclaimed because it would read on the prior non-partial crossbar Sample technology." (Tr. at 4701). Thus, complainant has taken the position that the additional limitations of dependent method claim 7, viz "providing a least one reconfigurable interconnect," and the additional limitations of dependent method claim 8, viz. "connecting

each of said reconfigurable interconnect ERCLC(s) to at least one but not all of the pins of each of said N ERCLCs" would distinguish claim 8 of the '473 patent from the Sample et al. RPM.

As discussed in section 3 a. i. supra, the principal distinction between the Sample et al. RPM system and claim 8 of the '473 patent is the designation of certain chips as "interconnect chips" and certain chips as "logic chips." Sample does not teach or suggest the use of a "reconfigurable interconnect ERCLC" as required by claim 8 of the '473 patent. Also, the XACTOR, the Wynn article and the Schmitz article each have at least this difference (FF 492, 495, 498, 500, 501).

The Clos article differs from claim 8 of the '473 patent because (1) it does not deal with hardware logic emulation systems (2) it is designed for use in a one-to-one environment of a telephone switching system, rather than the one-to-many situation of hardware emulation, and (3) it is a non-blocking network, where claim 8 of the '473 patent is directed to a blocking network (FF 444, 505). The Spandorfer report shows the use of a "Clos three-stage network" for connecting an array of logic cells (FF 506). However, the Spandorfer report (1) does not deal with hardware logic emulation, and (2) is a non-blocking network (FF 444, 448).

iii. Differences Between The Prior Art And The Claims At Issue ('496 Patent)

As discussed in section 3 a. i. supra, the principal distinction between the Sample et al RPM system (as well as the '353 patent) and claims 1, 2, 3 and 15 of the '496 patent is the designation between "interconnect devices" and "logic devices." The Sample et al RPM prototype does not teach or suggest the use of an "interconnect device" as required by the

claims in issue of the '496 patent. The XACTOR, the Wynn article and the Schmitz article each have at least this same difference (FF 492, 495, 498, 500, 501).

The Clos article and Spandorfer report differs from the claims in issue of the '496 patent for the reasons, supra, that said art differs from the claims in issue of the '473 patent.

iv. The Level Of Ordinary Skill In The Art

A person of ordinary skill in the art would have either (1) a bachelor's degree in electrical engineering or computer engineering, and possibly a graduate degree, or (2) equivalent level of experience to a bachelors degree if in fact that person did not have a degree, and several years of industrial experience in the design and development of digital systems (FF 516.

v. Objective Evidence Of Nonobviousness, Such As Commercial Success, Copying, Or Long-Felt Need

Complainant has relied on (1) consent judgement and admission of validity by PiE (2) the failure of others to make the invention, and (3) Butts' "invention story as objective evidence of nonobviousness (CBr at 27-30). Respondents argued that "the settlement of the PiE litigation does not support a finding of nonobviousness." (RRBr at 18).

Secondary considerations, or "objective indications of nonobviousness," such as long-felt need, commercial success, failure of others, copying, and unexpected results must be considered in a 35 U.S.C. § 103 determination. Graham, 383 U.S. at 17; Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc., 796 F.2d 443, 446, 230 USPQ 416, 419 (Fed. Cir. 1986), cert. denied 484 U.S. 823 (1987). For objective evidence to be accorded substantial weight, its proponents must establish a nexus between the evidence and the merits of the claimed invention. Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 1539, 218

USPQ 871, 879 (Fed. Cir. 1983). To the extent that the patentee demonstrates the required nexus, the objective evidence of nonobviousness will be accorded more or less weight. See Ashland Oil Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 306, 227 USPQ 657, 674 (Fed. Cir. 1985), cert. denied 475 U.S. 1017 (1986).

In this investigation there is evidence that PiE Design Systems (PiE), a former competitor of Quickturn, was sued by Quickturn for infringement of, inter alia, the '473 patent (FF 16, 26). PiE executed an "Admissions of Validity and Infringement and Stipulated Dismissal with Prejudice" on December 10, 1993, in which it admitted that the '473 patent "is valid and has been infringed by PiE" (FF 513). PiE however was also accused of infringing the '353 patent (FF 513), and PiE was acquired by Quickturn in a "reverse triangular merger" on June 30, 1993 as a result of its litigation with Quickturn (FF 513).

Complainant has submitted evidence that its first commercial product, the RPM, was based on the nearest-neighbor interconnect architecture (FF 19). Once Quickturn however discovered the partial crossbar interconnect architecture all further Quickturn products utilized the partial crossbar interconnect architecture, and the nearest-neighbor architecture

was displaced (FF 19)[36]. In addition, Quickturn was willing to purchase the '473 patent from Mentor, even when Quickturn already owned the '353 patent (FF 28, 29).

Based on the foregoing, the administrative law judge finds that objective evidence supports the non-obviousness of the '473 and '496 patents.

vi. Issue Of Obviousness ('473 Patent)

In analyzing invalidity under § 103, "the changes from the prior art . . . must be evaluated in terms of the whole invention, including whether the prior art provides any teaching or suggestion to one of ordinary skill in the art to make the changes that would produce the patentee's . . . device." Northern Telecom Inc. v. Datapoint Corp., 908 F.2d 931, 935, 15 USPQ2d 1321, 1325 (Fed. Cir.) cert. denied, 498 U.S. 920 (1990) (Northern Telecom).

The administrative law judge has found that respondents' arguments regarding the obviousness of claim 8 of the '473 patent "lack substantial merit" and do not raise a "substantial question" regarding the validity of the '473 patent. None of the references relied on by respondents teach or suggest the use of a separate reconfigurable interconnect

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[36] Butts testified regarding his discovery of the "partial crossbar" interconnect, that he started with a nearest neighbor architecture but:

> I found that personally unsatisfactory and I attempted to interconnect logic chips. I did a complete break and totally put the nearest-neighbor architecture aside and attempted to start from first principles to say "okay, I have logic chips, the logic chips have pins, they contains portions of the design and I wish to find a way to interconnect those logic chip pins. I went along a path of finding a way to maintain most of the connectibility of a full crossbar, at least for actual logic circuits, while not incurring the extreme costs of a full crossbar. I succeeded in the partial crossbar interconnect architecture (FF 514).

4. Unclean Hands

Respondents argued that complainant cannot be granted a temporary exclusion order because[

] Complainant argued that respondents' argument is based on the entirely erroneous notion that,[

] The staff argued that respondents are unlikely to establish that complainant [

]

The administrative law judge finds that[

] Moreover, the administrative law judge takes judicial notice of the fact that respondents never attempted to remove any portions of the public version of Motion No. 383-1 from the Secretary's public file[37].

5. Infringement

After the administrative law judge has construed disputed claim language he must determine whether the accused device is likely to fall within the scope of the asserted claims.

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[37] The Secretary maintains a public file of all filings for access by the public. She also maintains an official file which is the original documents that contain confidential information.

for use in a hardware logic emulator. Respondents' arguments amount to an attempt to "piece the invention together using the patented invention as a template. Such hindsight reasoning is impermissible." see e.g. Texas Instruments, 928 F.2d at 1177, 26 USPQ2d at 1029 (Fed. Cir. 1993).

vii. Issue Of Obviousness ('496 Patent)

All of the art relied on by respondents was before the examiner of the '496 patent (FF 414). The burden of establishing the invalidity of patent claims "is especially difficult when the prior art was before the PTO examiner during prosecution of the application." Hewlett-Packard Co. v. Bausch & Lomb, Inc., 15 USPQ2d 1525, 1527 (Fed. Cir. 1990), citing American Hoist & Derrick Co. v. Sowa & Sons, Inc., 725 F.2d 1350, 1359, 220 USPQ 763, 770 (Fed. Cir.), cert. denied, 469 U.S. 821 (1984). With respect to the Sample et al. RPM prototype, applicants argued during prosecution of the '496 patent that:

> [t]here is nothing in the Sample et al '353 patent which would suggest substituting Applicants' partial crossbar architecture for Sample at [sic] al's 'nearest-neighbor' architecture. Accordingly, Applicants' claims, all directed as they are to partial crossbar configurations, can be distinguished over the Sample et [al] '353 patent.

(FF 515) (emphasis added). The "Examiner's Statement of Reasons for Allowance" in the '496 prosecution history, dated February 16, 1995, states that:

> The examiner agrees that the prior arts of record fail to specifically disclose such a unique claimed **partial crossbar architecture** for use in a hardward [sic] logic emulation system.

(FF 446). In light of the foregoing, the administrative law judge finds that respondents are unlikely to succeed in establishing any of claims 1, 2, 3 or 15 of the '496 patent are obvious under 35 U.S.C. § 103.

H.H. Robertson, 820 F.2d at 389, 2 USPQ2d at 1929; Sofamor, 74 F.3d at 1218, 37 USPQ2d at 1531. To find infringement, an accused device must meet each claim limitation, either literally or under the doctrine of equivalents. Charles Greiner & Co. v. Mari-Med Mfg., Inc., 962 F.2d 1031, 1034, 22 USPQ2d 1526, 1528 (Fed. Cir. 1992).

a. The '473 Patent

In its Motion No. 383-1 for temporary relief, complainant asserted that the Meta Emulation Systems Series 500 and 500M devices (Meta system) infringe at least claim 8 of the '473 patent (CBr at 43).[38] Respondents argued that the Meta device does not infringe the '473 patent because it fails to meet numerous elements of those claims (RBr at 39). The staff argued that complainant will probably succeed in proving that in its normal, intended operation, the Meta device infringes claim 8 of the '473 patent (SBr at 34).

Referring to claim 8, rewritten in independent form, supra,[

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[38] Each of complainant, respondents and the staff agree that the Meta 500 and 500M devices are the same for purposes of infringement (FF 518). Thus, this entire analysis applies to both devices.

[39] Respondents argued that [

] As discussed in "Claim Construction" supra, the "input data" of claim 8 does not require any one-to-one correspondence with a users design. Thus, the fact

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]

Respondents argued that the Meta device does not literally infringe claim 8 of the 473 patent, because[

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[ ]

Complainant has argued that[ ][

] The staff argued that[

]

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that[

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[

] The claim 8 method step of "providing at least one reconfigurable interconnect ERCLC" contains a both a functional and structural recitation. Specifically, the administrative law judge has

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[40] Complainant's counsel argued that[

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construed a "reconfigurable interconnect ERCLC" as a device that must have logic capability, such as is found in an ERCGA. See "Claim Construction" supra section 2 a. vi. A "structural recitation in a method claim step [may be] construed as a limitation on the claim." Moleculon, 793 F.2d at 1271, 229 USPQ at 812, citing Austin Powder Co. v. Atlas Powder Co., 568 F.Supp. 1294, 1316 (D.Del 1983). [

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Complainant has further argued that "Claim 8 is plainly infringed under the doctrine of equivalents" (CBr at 45). [

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__]

Under the doctrine of equivalents, an accused product that does not fall literally within the scope of an asserted claim, may nonetheless infringe if its difference from the asserted claim is "insubstantial from the perspective of one of ordinary skill in the relevant art." Athletic Alternatives, Inc. v. Prince Mfg, Inc., 73 F.3d 1573, 1581 (Fed. Cir. 1996), citing Hilton Davis Chem. Co. v. Warner-Jenkinson Co., Inc., 62 F.3d 1512, 1518, 35 USPQ2d 1641, 1645 (Fed. Cir.) (in banc), petition for cert. granted 116 S.Ct. 1014, 134 L.Ed.2d 95 (1996) (Hilton Davis). A finding of infringement under the doctrine of equivalents "requires

proof of insubstantial differences between the claimed and accused products or processes. Often the function-way-result test will suffice to show the extent of the differences." Hilton Davis 62 F.3d at 1520, 35 USPQ2d at 1648. Moreover, "[t]he known interchangeability of the accused and claimed elements is potent evidence that one of ordinary skill in the relevant art would have considered the change insubstantial. Hilton Davis 62 F.3d at 1518, 35 USPQ2d at 1646 (emphasis added).[41]

The specification of the '473 patent teaches:

> For a device to be useful as a Realizer interconnect chip:
>
> 1) It should have the ability to establish many logical interconnections between arbitrarily chosen groups of I/O pins at once, each interconnection receiving logic signals from its input I/O pin and driving those signals to its output I/O pin(s).
>
> 2) It should be electronically reconfigurable, in that its interconnect is defined electronically, and may be redefined to suit many different designs.
>
> 3) If a crossbar summing technique is used to interconnect tri-state nets in the partial crossbar interconnect, it should be able to implement summing gates. (If not, other tri-state techniques are used, as discussed in the tri-state section.)

(FF 407). The specification also teaches that:

> The ERCGA devices discussed above . . . satisfy these requirements, so they may be used as interconnect chips. Even though little or no logic is used in the

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[41] Respondents have relied on Texas Instruments v. U.S. Int'l Trade Comm'n, 805 F.2d 1558, ___ USPQ2d ___ (Fed. Cir. 1986) (Texas Instruments), in which the court held that "it is the claimed invention as a whole that must be considered in determining whether there is infringement by the accused devices also considered as a whole." Id. at 1569. However, the portion of Texas Instruments relied on by respondents involved the application of "means plus function" claims under 35 U.S.C. § 112 ¶ 6, rather than the doctrine of equivalence. see Intel Corp., 946 F.2d at 842, 20 USPQ at 1170. Claim 8 in issue is not a "means plus function claim." Moreover, Texas Instruments does not supersede the "element-by-element" analysis, wherein "the 'substantially the same way prong of the test may be met if an equivalent of a recited limitation has been substituted in the accused device." Read Corp. v. Portec, Inc., 970 F.2d 816, 821, 23 USPQ2d 1426, 1431 (Fed. Cir. 1992), see also Hilton Davis 62 F.3d at 1520, 35 USPQ2d at 1648.

> interconnect chip, the ability to be configured into nearly any digital network includes the ability to pass data directly from input to output pins.
>
> * * *
>
> Crossbar switch device . . . or the crosspoint switch devices commonly used in telephone switches, may be used as interconnect chips.

(FF 408). The specification further teaches that:

> In the crossbar summing configuration, the summing OR gate is placed on the crossbar chip, making use of the fact that the crossbar chips in some embodiments are implemented with ERCGAs, such as LCAs, which have logic available. . . .

(FF 409) (emphasis added). Thus, the specification defines the functionality required for an "interconnect ERCLC" and further teaches that a "crossbar switch device" or "crosspoint switch device" could be substituted for an ERCGA (or ERCLC).

The claim 8 method step in issue requires "at least one reconfigurable interconnect ERCLC" to perform the function of "interconnecting the N ERCLCs." [

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ii. The Meta Device[

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Claim 8 of the '473 patent claims a method which provides "connecting each of said reconfigurable interconnect ERCLCs to at least one but not all of the pins of each of said N ERCLCs." Respondents argued that the Meta device does not meet this limitation because[

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As detailed in "Claim Construction ('473 patent)" section 2 a. vii. supra, claim 8 is directed to a "method comprising." While the use of the transition term "comprising" means that "recited elements are only a part of the device," see 2 Chisum, Patents, § 8.06[1][b] (1995), the mere use of the term "comprising" does not affect the scope of a particular structure recited in a claim. Moleculon, 793 F.2d at 1271, 229 USPQ at 812. Thus, while additional method steps or structures may be present in the accused device, the

transitional term "comprising" can not affect the claim phrase "connecting each of said reconfigurable interconnect ERCLCs to at least one but not all of the pins of each of said N ERCLCs." Id.

In issue is whether[

]

In view of the foregoing, the administrative law judge finds that[

]is an additional step which can

not avoid infringement, as "[t]he addition of features does not avoid infringement, if all the elements of the patent claims have been adopted, . . . Nor is infringement avoided if a claimed feature performs not only as shown in the patent, but also performs an additional function." Northern Telecom, 908 F.2d at 945, 15 USPQ2d at 1333; Moleculon 793 F.2d at 1264, 229 USPQ at 812; Chisum, Patents, § 18.04[4]; Stiftung, 945 F.2d at 1178; A.B. Dick, 713 F.2d at 703, 218 USPQ at 967-68 ("It is fundamental that one cannot avoid infringement merely by adding elements if each element recited in the claims is found in the accused device"); Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1057 (Fed. Cir. 1988) ("Adding features to an accused device will not result in noninfringement if all the limitations in the claims, or equivalents thereof, are present in the accused device"); Marsh-McBirney, Inc. v. Montedoro-Whitney Corp., 882 F.2d 498, 504 (Fed. Cir. 1989), vac. on other grounds 115 S.Ct. 775, reinstated in part 939 F.2d 969 (1991); Insta-Foam Products v. Universal Foam Systems, 906 F.2d 698, 702 (Fed. Cir. 1990).

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] [ ][

] The specification of the '473 patent teaches that:

> The logic chip itself can offer an additional degree of freedom which crossbars do not exploit, because it has the ability to be configured to use any of its I/O pins for a given input or output of the logic network it is being configured for, regardless of the particular network. That freedom allows the possibility of the partial crossbar interconnect, which is the reason it is specified in the definition of the logic chip.

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[42] Respondents also argued that complainant disclaimed [ ]during prosecution of the '496 patent. That argument is discussed with respect to the '496 patent, infra.

(FF 434). [

] Respondents

thus would require complainant to prove literal infringement by proving that the accused Meta system is not an adoption of the combined teachings of the prior art. This argument has no support in the law governing patent infringement. As the Federal Circuit has stated in Baxter Healthcare Corp. v. Spectramed Inc., 49 F.3d 1575, 1583, 34 USPQ2d 1120, 1126 (Fed. Cir.), cert. denied 116 S.Ct. 272, 133 L.Ed.2d 194 (1995) (Baxter):

> [t]here is no requirement that the accused device be nonobvious in light of the prior art, or otherwise be itself patentable. Literal infringement exists if each of the limitations of the asserted claim(s) read on, that is, are found in, the accused device. Questions of obviousness in light of the prior art go to validity of the claims, not to whether an accused device [literally] infringes.

Thus, to prove literal infringement, complainant is not required to prove that the accused Meta system is not "an adoption of the combined teachings of the prior art." Id.

Based on the foregoing, the administrative law judge finds that complainant is likely to succeed in establishing that the accused Meta device meets each limitation of claim 8 of the '473 patent either literally or under the doctrine of equivalents.

b. '496 Patent

In its Motion No. 383-1 for temporary relief, complainant asserted that the accused Meta device infringes at least claims 1, 2, 3 and 15, supra, of the '496 patent (CBr at 33).

Respondents argued that the Meta device does not infringe the '496 patent because it fails to meet "numerous" elements of those claims (RBr at 39). The staff argued that Meta's logic boards infringe independent claim 1, dependent claims 2 and 3 and independent claim 15 of the '496 patent (SBr at 34).

Referring to the claims in issue, supra, it is undisputed that[

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[43] At closing arguments, respondents' counsel argued as follows:

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[45] See section 5 a. i., footnote 40, supra.

] (FF 577). As a result the administrative law judge finds that the "interface structure . . ." limitation of claim 15 is literally met by the Meta device.

i. The Meta Device Meets The Claim 1 And Claim 15 Requirement That "Each Of Said Reprogrammable Interconnect Devices Is Connected To At Least One But Not All Of Said Programmable I/O Terminals On Each Of Said Reprogrammable Logic Devices"

Each of independent claims 1 and 15 of the '496 patent contains the phrase "each of said reprogrammable interconnect devices is connected to at least one but not all of said programmable I/O terminals on each of said reprogrammable logic devices." Respondents argued that[

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Claims 1 and 15 of the '496 patent claim an "electrically reconfigurable logic assembly comprising:" As noted supra "Infringement" ('473 patent), the term "comprising" means that the "recited elements are only a part of the device." 2 Chisum, Patents, §§ 8.06[1][b], 18.04[4] (1995); and the mere use of the term "comprising" does not affect the scope of a particular structure recited in a claim. Moleculon, 793 F.2d at 1264, 229 USPQ at 812. [

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Each of claims 1 and 15 require "a plurality of reprogrammable logic devices. . . ." and "a plurality of reprogrammable interconnect devices. . . ." The "plurality" requirement is met by at least two devices, see "Claim Construction" supra. The plain language of each of claims 1 and 15 refers to "each of said reprogrammable interconnect devices is connected to at least one but not all of said programmable I/O terminals on each of said reprogrammable logic devices." (emphasis added). [ ]

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The specification of the '496 patent also teaches a preferred embodiment wherein "Xchips," that are "reprogrammable interconnect devices" are connected to "Ychips," which are "reprogrammable interconnect devices." The "Ychips" in turn are connected to "Zchips," that are "reprogrammable interconnect devices." (FF 432). While the "Xchips" are connected to logic chips ("Lchips"), neither of the "Ychips" or the "Zchips" are connected to any logic chips (FF 432). [

] as "[t]he addition of features does not avoid infringement, if all the elements of the patent claims have been adopted, . . . Nor is infringement avoided if a claimed feature performs not only as shown in the patent, but also performs an additional function." Northern Telecom, 908 F.2d at 945, 15 USPQ2d at 1333; Moleculon 793 F.2d at 1264, 229 USPQ at 812; Chisum, Patents, § 18.03[4] Shamrock Technologies, Inc. v. Medical Sterilization, Inc., 903 F.2d 789, 793, 14 USPQ2d 1729, 1732 (Fed. Cir. 1990) ("The argument that infringement is precluded by adding a prior art step is fallacious."); Carl Zeiss

Stiftung v. Renishaw PLC, 945 F.2d 1173, 1179, 20 USPQ2d 1094, 1099 (Fed. Cir. 1991) ("an improvement upon a patented device does not necessarily avoid infringement"). [

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Respondents also relied on the following testimony of Butts:

> Q. And it would have been obvious to use a Clos network with logic for emulation, would it not?
>
> A. I can't speculate on what's obvious or not.
>
> Q. But it's not your invention?
>
> A. It's not my invention.

(Butts Tr. at 611). [

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]the following arguments made by applicants in a September 14, 1994 "Amended

Information Disclosure Statement" during prosecution of the '496 patent as evidence that [

]:

> Significantly, Applicants' partial crossbar architecture is a blocking architecture. . . . This is in distinct contrast to non-blocking connection schemes, where a connection path between any two remaining unconnected points in the system is always guaranteed regardless of the previous connection paths which have been established. Indeed, part of Applicants' inventive contribution to the field of logic emulation is the non-obvious recognition that a partial crossbar interconnection architecture, despite its blocking nature, will provide sufficient routing resources to realize a practical number of circuit-switched connection paths -- and a corresponding practical number of arbitrary logic circuits designs -- in a reconfigurable environment.
>
> * * *
>
> The Spandorfer reference does raise the question of whether logic cell connections can be made using a structure "which realistically permits a certain level of blocking", and then goes on to imply that the Clos-type network which interconnects Spandorfer's macrocellular array is a blocking network. (See Spandorfer, p. 3-13).
>
> Spandorfer's implication is incorrect. Putting aside the observation that Spandorfer fails to discuss any of the considerations and constraints associated with logic emulation -- and thus does not answer any question about whether blocking connectivity schemes would work in a logic emulation environment -- the three-stage Clos network which Spandorfer discusses in his reference is in fact a non-blocking network. (See, i.e., Clos, "A study of Non-Blocking Switching Networks," The Bell System Technical Journal, March 1953, pp. 406-424 . . .)"

Respondents also relied on the examiner's reason for allowance of the '496 patent:

> During the 10 August 1994 interview, applicants' representative repeatedly stated that the claimed invention is directed to an electrically reconfigurable logic assembly incorporating the unique **partial crossbar architecture** in a hardware logic **emulation system**. The examiner agrees that the prior arts of record fail to specifically disclose such a unique claimed **partial crossbar architecture** for use in a hardware logic emulation system.

(FF 446) (emphasis in original). [

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[46] [

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In view of the foregoing, the administrative law judge finds that complainant is likely to establish that the accused Meta device literally meets every element of claims 1, 2, 3 and 15 of the '496 patent.

6. Domestic industry

a. Economic Prong

Subsection (a)(3) of section 337 sets forth the following criteria for determining the existence of a domestic industry in patent-based investigations under section 337(a)(1)(B):

> [A]n industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the patent . . . concerned --
>
> (A) significant investment in plant and equipment;
>
> (B) significant employment of labor or capital; or
>
> (C) substantial investment in its exploitation, including engineering, research and development or licensing.

19 U.S.C. § 1337(a)(3). To satisfy the domestic industry requirement, a complainant need only show that it meets the requirement of any one of the three prongs of subsection (a)(3), Certain Plastic Encapsulated Integrated Circuits, Inv. No. 337-TA-315, Commission Opinion

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[47] [

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at 18 (1991). Neither respondents nor the staff contest complainant's argument that it satisfies the economic prong of the domestic industry requirement (FF 17).

The domestic requirement of section 337(a)(3) is satisfied if complainant produces the article in question in the United States. See In the Matter of Certain Methods of Making Carbonated Candy Products, Inv. No. 337-TA-292 (ID 1989), aff'd in relevant part, 55 Fed. Reg. 3281 (ITC 1990) (Carbonated Candy). The administrative law judge finds that complainant manufactures in the United States hardware logic emulation systems and components thereof at its facilities in California resulting from substantial investments in plant and equipment in connection with said manufacture (FF 18-26). Hence, the administrative law judge finds that complainant has a likelihood of success in establishing the economic prong of the domestic industry requirement.

b. Technical Prong

Complainant argued that the hardware logic emulation systems manufactured by Quickturn in the United States are covered by the claims of the '473 and '496 patents in issue; that complainant manufactured hardware logic emulation systems and components thereof at its facilities in California; and that the evidence has shown that that system is covered by the claims in issue (CFF 254, 277-279). The staff argued that complainant has shown that its hardware logic emulation systems practice the asserted claims in issue of the '473 and '496 patents. Respondents do not oppose the arguments that complainant's hardware logic emulation systems are covered by the claims in issue (FF 17).

The administrative law judge finds that complainant has satisfied its burden in establishing that the hardware logic emulation systems manufactured by complainant in the

United States are covered by the claims in issue. See FF 19. Accordingly, complainant has a likelihood of success in establishing the technical prong of the domestic industry requirement.

7. Irreparable Harm

Significant for determining whether there is a threat of immediate and substantial harm to the domestic industry in the absence of temporary relief for the period from August 5, 1996 to March 19, 1997 (the critical period), viz. the second factor for entitlement of temporary relief, are (1) the nature of the patent rights in issue; (2) the relevant U. S. industry for economic analysis; (3) the nature of the complainant and the respondents; (4) the life cycle of complainant's product in issue; (5) what bearing, if any, specific lost sales by respondents in the past both in the United States and internationally have on the harm that would be suffered by complainant in the absence of temporary relief; (6) price erosion; and (7) the issue of quantifiable harm. See Certain Radiotelephones, Inv. No. 337-TA-297, Order No. 21, Unreviewed Initial Determination on Temporary Relief at 141 to 147 (August 9, 1989).

Irreparable harm may be demonstrated either by an unrebutted presumption based on a strong showing of patent validity and patent infringement or by a factual showing. Id. See also Certain Pressure Transmitters, Inv. No. 337-TA-304, USITC Pub. 2392, Commission Opinion at 13, 16, 18 (October 303, 1990), aff'd sub nom, Rosemont, Inc. v. United States International Trade Comm'n, 910 F.2d 819, 15 USPQ2d 1569 (Fed. Cir. 1990) (Pressure Transmitters) and Electrical Connectors, Id. Courts faced with the "strong" showing of validity of a patent and its infringement have found irreparable harm merely from continued

infringement of the valid patent on the ground that the very nature of the patent right is the right to exclude others and once the patentee's patent has been held valid and infringed, the patentee should be entitled to the full enjoyment and protection of its patent rights. Smith Int'l, Inc. v. Hughes Tool Co., 718 F.2d 1573, 1582, 219 USPQ 686, 692 (Fed. Cir. 1983), cert. denied, 464 U.S. 996 (1983), (Smith Int'l) (citing Zenith Laboratories, Inc. v. Eli Lilly and Co., 460 F. Supp. 812, 825, 201 USPQ 524 (D.N.J. 1978)). Even when irreparable harm is presumed and not rebutted, it is still necessary to consider the balance of hardships and all of the competing equities between the parties before an injunction may be issued. H.H. Robertson v. United Steel Deck Inc., 820 F.2d 384, 390, 2 USPQ2d 1926, 1930 (Fed. Cir. 1987); Atlas Powder, 773 F.2d at 1233, 227 USPQ at 292; Nutrition 21 v. U.S., 930 F.2d 867, 869, 870, 18 USPQ2d 1347, 1350, 1351 (Fed. Cir. 1991) (Nutrition).[48]

Complainant argued that the record establishes that it is entitled to the presumption of irreparable harm and that respondents are unable to successfully rebut that presumption. It was also argued that, notwithstanding the presumption to which complainant is entitled, complainant is currently suffering, and is further threatened with suffering, substantial harms resulting directly from respondents' infringing activities; and that those current and threatened harms cannot be quantified and will immediately and irreparably affect complainant's viability as a going concern, and its reputation as the technology leader in the U. S. hardware logic emulation industry (CBr at 47).

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[48] The CAFC, in Nutrition, found that the movant Nutrition 21 had not established facts entitling it to a presumption of irreparable harm because the validity of the '927 patent in issue had never been tested in litigation and the district court made no finding that Nutrition 21 had made a clear showing that the '927 patent was valid.

The staff argued that complainant is entitled to a presumption of irreparable harm based on clear showings of patent validity and infringement and that as for actual threatened harm, the presumption of irreparable harm has not been rebutted by the respondents (SBr at 45, 46).

Respondents argued that complainant is not entitled to a presumption of irreparable harm and that complainant has not demonstrated any irreparable harm (RBr at 58).

a. Nature Of The Patent Rights In Issue

The nature of the patent rights in issue are critical in determining whether complainant is entitled to a presumption of irreparable harm and also for determining when past actions of respondents may be probative in showing any harm that respondents' actions will cause complainant in the critical period.[49] In issue, in complainant's Motion No. 383-1, are claim 8 of the '473 patent and claims 1, 2, 3 and 15 of the '496 patent. The '473 patent issued on July 30, 1991, more than four years prior to the filing of this complaint and Motion No. 383-1. The '496 patent issued on September 5, 1995 (FF 28, 48). Both the '473 and the '496 patents are derived from a chain of applications which includes an identical application. Thus the '473 patent is based on Serial No. 417,1196 filed October 4, 1989 which application in turn was based on a continuation-in-part Serial No. 254,463 filed on October 5, 1988 and now abandoned (FF 28). The '496 patent is based on Serial No. 270,234 filed July 1, 1994 which in turn is a continuation of abandoned Serial No. 175,981 filed December 30, 1993 which in turn was a continuation of abandoned Serial No. 698,734

[49] See Electrical Connectors at 90 where this administrative law judge held that complainants had no existing right prior to the January 24, 1995 issuance date of the patent in issue to exclude the respondents from the claimed subject matter in issue.

filed May 10, 1991, which in turn was a continuation-in-part of Ser. No, 417,196 filed October 4, 1989 and now the '473 patent. Serial No. 417,196 was a continuation-in-part of abandoned Serial No. 254,463 filed October 5, 1988 (FF 48). Accordingly, the specifications of the '473 and '496 patents are identical with the exception of the new matter introduced into Serial No. 698,734 and each is entitled to an October 5, 1988 filing date.

The '473 patent has been involved in prior concluded litigation. Thus Quickturn sued PiE Design Systems (PiE) for infringement of various patents including the '473 patent in the U. S. District Court, Northern District of Calif. In that litigation, PiE cited a substantial amount of prior art. While the district court made no finding with respect to validity and infringement of the '473 patent, PiE and Quickturn did execute a consent judgment in which PiE admitted that the '473 patent was valid and infringed and in which Quickturn dismissed with prejudice its complaint against PiE (FF 28, 513)[50].

In Smith Int'l the CAFC reversed a denial of a motion for entry of a preliminary injunction to prevent the further infringement of two patents and remanded the case with instructions to issue the preliminary injunction. The patents at issue in Smith Int'l had previously been declared valid, by the Ninth Circuit, and there was an admission that the patents had been infringed and were continuing to be infringed. The CAFC, in reversing the district court, stated that courts faced with strong showing of validity and infringement have found irreparable harm from continued infringement of a valid patent, citing, and agreed "with the reasoning in these cases," Zenith Laboratories, Inc. v. Eli Lilly and Co., 460 F. Supp. 812, 825, 201 USPQ 324-35 (D.N.J. 1978) (Zenith) and Teledyne Industries, Inc. v.

[50] This consent judgement was executed subsequent to Quickturn's acquisition of PiE (FF 28, 513).

Windmere Products, Inc., 433 F. Supp. 710, 7411, 195 USPQ 354, 378-79 (S. D. Fla. 1977) (Teledyne). In Zenith, the patentee had relied on the statutory presumption of validity and evidence of acquiescence with respect to the drug patent in issue to show validity. The district court found that the presumption of validity exists merely to give the patent grant substance and value; that it has no independent evidentiary value; and that it rather serves to place the burden of proof on the party who asserts invalidity. Id. The district court, however, found that the evidence before it was sufficient to show acquiescence even though the patent at issue was only five and a half years old[51]. It observed that there was demonstrated tremendous financial success and that the drug companies were highly competitive. As to infringement, the district court stated that soliciting orders for processing and selling the drug in issue had been admitted. In Teledyne the patentee sought a temporary injunction to prevent the marketing of a product on the grounds that the product infringes certain patents. The district court found that Teledyne had demonstrated its entitlement to a preliminary injunction based on claims of patent infringement. In so finding the district court found that the parties had been before the court "almost six months;" that numerous hearings on the issue of patent validity and infringement have been held; that the parties have "vehemently" presented their positions and both parties have submitted voluminous affidavits of experts arguing the technical merit of the patents and the pertinent prior art; that lengthy depositions of those experts have been filed during which they were subject to "provocative cross-examination; and that after all this, the "court is not so unfamiliar with the Teledyne

[51] The district court stated that public acquiescence in the validity of a patent is manifested by a lack of substantial challenge to the monopoly rights of the patentee under circumstances which would support an inference that the patent had been examined and deemed valid. Zenith 460 F. Supp. at 823, 201 USPQ at 331.

patents and the prior art that it cannot rule upon the probable validity of the patents or upon their probable infringement." The district court found that while the presumption of validity under 35 U.S.C. §282 is controverted somewhat although not removed by the fact that the patent has not been previously adjudicated valid, other facts may reinforce the presumption. Thus, although the patent was relatively new and had not been the subject of longstanding acquiescence, the invention appeared from the reaction in the marketplace, to be a significant step forward in the art and had been a tremendous commercial success; that until defendant's activity, the patentee was the sole source of the product in issue; and that defendant has paid the patentee the "faithful tribute of imitation." The district court concluded that this "evidence" suggests that in the brief time since its introduction, the patented device has been treated by all, except the alleged infringer, as fully protected under the patent laws. Teledyne, 433 F. Supp. at 714, 195 USPQ at 357. On the issue of infringement, the district court found that the evidence at least demonstrated likely infringement. Id. 433 F. Supp. at 732-734, 195 USPQ at 369-373.

i. Complainant Is Entitled To A Presumption Of Irreparable Harm

While there has been no prior determination by a court that the '473 and '496 patents are not invalid and are infringed, there has been an admission of validity of the '473 patent in a prior district court proceeding. Moreover, in Zenith, which reasoning the CAFC agreed with, there was no prior finding of validity or infringement by a federal court. Likewise in Teledyne, which reasoning the CAFC also agreed with, there was no such prior finding. In this investigation, as in Teledyne, the parties have intensely litigated the issues of patent validity and infringement. Prior to the hearing, there was a large amount of discovery which

included interrogatories, document production and lengthy depositions of a large number of witnesses There also has been eleven hearing days which generated some 4300 pages of transcript. Some 1500 exhibits have been received into evidence. Lengthy prehearing and post-hearing submissions were filed. Closing arguments on June 5, 1996 went from 8:00 am to about 10:00 pm with only a short lunch break and resulted in approximately 600 additional transcript pages. Moreover, all of the prior art cited by the respondents at the hearing was before the Patent Office in the prosecution of the '496 patent. Also, the terminal portion of the '496 patent, subsequent to the expiration date of the '473 patent, was disclaimed to avoid a double patenting rejection made by the examiner in light of claim 8 of the '473 patent. In addition, the invention in issue has achieved commercial success (FF 19). Accordingly, based on the foregoing and his analysis of the validity and infringement of the claims in issue, supra, the administrative law judge finds that there is a clear showing of likelihood of success on patent infringement and validity and complainant is thus entitled to a presumption of irreparable harm from continued infringement of the valid claims in issue in Motion No. 383-1. As seen from the foregoing analysis, he further finds that the presumption of irreparable harm has not been rebutted.

b. Relevant U. S. Industry For Economic Analysis

Complainant argued that the products which make up the relevant U.S. industry for the purpose of economic analysis in this investigation are limited to hardware logic emulation components and systems; that other design verification methodologies and tools, such as simulation, hardware acceleration and cycle-based simulation are not included in this relevant industry for this investigation because such tools are used by IC developers in conjunction

with, and not as substitutes for, one another and once an IC design reaches a certain size or level of complexity, those other technologies become substantially less effective than emulation (CFF 288). Respondents' economic expert Hoffman testified that the relevant market in this investigation should include alternative methods for chip verification that compete for the same project dollars with emulation which methods include simulation, accelerated simulation and internally designed verification systems (RX 755 at 10). The staff argued that because complainant presently supplies about ninety percent of all emulators sold in the United States, and because Mentor/Meta is the only competing supplier for high capacity emulators, any sales by Mentor and Meta can be assumed to be lost sales to complainant (SBr at 51, 52).

In determining the extent of harm that may be suffered by complainant, the administrative law judge must evaluate the threat to complainant's domestic industry. The domestic industry, for the purpose of determining irreparable harm, is defined by the claims in issue of the '473 and '496 patents. See Electrical Connectors, Unreviewed I.D. at 92-94; Pressure Transmitters, Comm'n Op. at 10; Circuit Board, Comm'n Op. at 28-30; Growth Hormones, Unreviewed I.D. at 89; Radiotelephones, Unreviewed I.D. at 141 to 147. In this investigation, the domestic industry is defined by claim 8 of the '473 patent and claims 1, 2, 3 and 15 of the '496 patent, each of which are directed to hardware logic emulation systems that employ the "partial crossbar" architecture, see "Claim Construction" supra. All of complainant' products use the patented "partial crossbar" (FF 19). Therefore, in evaluating irreparable harm, any harm to Quickturn is coextensive with harm to the domestic industry.

A "simulator" is a software program which executes an algorithm on a general purpose computer that attempts to simulate the function of a design for the purposes of verifying the functionality and timing of a design before it is sent to a foundry to become silicon (FF 105). A simulator accelerator is a hardware product that allows a software simulator to run at faster speeds than a software simulator on a work station (FF 106). A simulation accelerator and hardware accelerator are used interchangeably. Those devices are special purpose hardware systems which execute an algorithm for the purposes of verifying the functionality and timing of a design (FF 106).

Simulation and hardware acceleration devices run at speeds in the range of hundreds to the low thousands of cycles per second, which is several orders of magnitude slower than emulators which run in the low millions of cycles per second (FF 106, 110, 111). The fundamental differences between a hardware accelerator and an emulator relate to speed of operation, underlying technology, and application[52]. The speed differential between hardware accelerators and emulators is due to underlying technology differences. Emulators, unlike hardware accelerators, express the entire design, including interconnect, concurrently in reprogrammable hardware. Therefore, the entire design is processed every clock cycle. Hardware accelerators are characterized by "event queues" which process small parts of the design at a time and swap pieces back and forth out of memory. The application differences between hardware accelerators and emulators are also in large part dictated by the speed

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[52] Mentor announced to the world in December 1995 that its Sim Express™ which it made available to U.S. customers in January 1996 compiles designs faster on a single workstation than other emulators can on multiple (up to 75) workstations running in parallel and that the Sim Express™ design compilations, when performed on a single workstation, are typically 100 X faster than traditional emulation systems (FF 54).

difference. The speed of emulators enables them to be interfaced directly to a user's target system, if desired. Hardware accelerators are much too slow for this application and are generally used for regression testing, that is, verifying the same set of test vectors over and over again against evolving versions of a design, and functional verification only (FF 107).

A customer who is going to use an emulator would most likely use a simulator and/or hardware accelerator not as a substitute for an emulator but rather prior to using the emulator (FF 108). Thus, Quickturn's emulation product is used further into the design verification stage than any simulator, simulation acceleration or hardware accelerator (FF 109). Emulators are complimentary to simulators and hardware accelerators. Customers who consider emulators usually already use simulators and most use hardware accelerators as well. Those customers will continue to use simulators and hardware accelerators after they purchase an emulator as most design teams in the United States use simulation and hardware acceleration in conjunction with emulation, not instead of emulation (FF 110, 111). The issue to a potential customer of an emulation system is not whether to buy the system in preference to a simulator or hardware accelerator, but whether the benefit of using emulation in addition to other EDAs is warranted in view of emulation's relatively high costs compared to other EDA's (FF 110, 111, 125). When an ASIC (application-specific integrated circuits) reaches a certain size or complexity, technologies such as simulation, hardware acceleration and cycle based simulation are substantially slower than emulation (FF 112).

Designs of complexity under 100K gates can typically be managed without emulation, using hardware accelerators or simulators combined with respins of silicon if needed. Emulators are usually not viewed as cost effective below the 100K gate threshold, and for

designs above 100K gate complexity, hardware accelerators are usually sold to accounts that must have faster timing verification, whereas emulators are sold for higher speed functional verification and in-circuit emulation (FF 110).

A Mentor document states that [ ] (FF 113). Moreover, Mentor has taken the position that, [ ] (FF 93).

Another Mentor document, dated April 5, 1995 (FF 118), states that [ ] and also the following:

[

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* * *

has a slide 1 which states[

] Slide 2 states:

[

]

Slide 3 states:

[

]

Slide 4 is titled[ ] Slide 5 is titled[

] Slide 6, discloses that[

] Slide 8 titled[

] As to the former it states[ ]

As to the Sim Express™ it states[ ] Slide 9 states that[

] Thus Mentor, as seen supra, prior to

this investigation, believed that[ ]and that the

[

]

Meta further presented [

](FF 128).

Even Meta's Reblewski[

]

There is a relationship between integrated circuit (IC) complexity and the probability that an IC developer will purchase and use a hardware logic emulation system. That probability increases when the IC under development exceeds 100,000 gates (FF 121). Because of[

](FF 134). Meta's own literature recognizes[

]

[

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(FF 135).

The '473 and '496 patents explain how the disclosed hardware logic emulation system, also referred to as the Realizer System, can serve as the basis for "a new means of building a logic simulator" as follows (FF 136):

3. Realizer System Applications

3.1. Realizer Logic Simulation System

A logic simulator is a system, implemented in hardware or software, which receives an input design, a set of stimulus to the design and a direction to simulate for a period of time, and produces a set of responses which predict those that a real implementation of the input design would produce given the same stimulus. The stimulus and responses are in the form of logic state transitions of specified design nets at specified times. An important characteristic is that the simulator user provides only the description of a design in the form of the input design file, so the design may be changed and resimulated in short period of time.

Current software logic software simulator design practice is to use a computer software program, executing a sequential algorithm which predicts the design's operation ("An Introduction To Digital Simulation," Mentor Graphics Corp. Beaverton Oreg. 1989). Either the event-driven or compiled or compiled code algorithm, which are well known, are used. Current hardware logic simulator design practice is to build hardware which executes the same event-driven or compiled code sequential algorithms used in software simulators. The hardware gains its performance advantage only by exploiting parallelism in the algorithm and/or directly implementing special algorithmic operations, which are not possible for a general-purpose computer executing software. Current hardware logic simulators operate by executing an sequential algorithm which predicts the input design's responses.

A new means of building a logic simulator is based on the Realizer System. The Realizer logic simulator system receives a input design, which it converts into a configuration of the Realizer hardware's logic interconnect chips, using Realizer design conversion system. It receives a set of stimulus to the design and a direction to simulate for a period of time, applies that stimulus to the Realized design via Vector Memories, and collects a set of responses from the Realized design via Vector Memories. The response correspond to those that a real implementation of the input design would produce given the same stimulus, because an actual hardware realization of the design is observed responding to that stimulus.

This differs fundamentally from all current logic simulation systems, in that they execute a sequential algorithm which predicts the design's responses to stimulus, while the Realizer logic simulator operates a realization of the design to determine the design's responses to stimulus. The primary advantage is that the realized design generates responses many orders of magnitude faster than a sequential algorithm can predict responses (emphassis added).

Hence, the hardware logic emulation system of the Butts '473 and Butts '496 patents,[

]provides emulation capabilities and can also perform as a logic simulator (FF 118).

i. Domestic Industry Consists Of Hardware Logic Emulators

The administrative law judge finds that hardware logic emulators represent a threat to the domestic industry in this investigation for analysis purposes on the irreparable harm issue. This finding, as seen by the record supra, is supported not only by Mentor documents but also by the testimony of witnesses produced by complainant and respondents. While hardware logic emulators may perform as a logic simulator they are found to be unique in that they can also run at very fast speeds to perform emulation. Hence they are directed to potential customers who have to make the decision of whether the benefit of using emulation is warranted in view of the emulator's high costs when compared to other EDAs.

c. Nature Of Complainant And The Respondents

Critical elements for determining whether any irreparable harm is likely to occur to complainant in the critical period are the nature of complainant and respondents and the life span of complainant's product in issue.

i. Complainant Quickturn

Complainant Quickturn was founded in 1987 and made its first sales of emulation products in 1989 (FF 2). By an Asset Purchase Agreement dated February 28, 1992, Quickturn acquired, through payment to Mentor of $200,000 and Quickturn stock, all of Mentor's emulation system hardware and software in existence at that time, a prototype of an emulation system and exclusive ownership of the '473 patent and the Butts et. al. application

07/698,734 (the '734 application) which, through continuation practice, ultimately matured into the '496 patent (FF 28). The Asset Purchase Agreement included a Patent Assignment dated March 2, 1992 which contained express language that assigned to Quickturn the entire right, title and interest to all the inventions disclosed in the '473 patent and in the '734 application (FF 29).

Quickturn presently sells emulator product lines which include the System Realizer™, the Enterprise™ and the Mars™ Emulation systems along with accompanying software and peripheral products. Quickturn also provides and sells services for the set-up and on going use of its emulation products at customer sites (FF 138). Quickturn's System Realizer™ family of hardware logic emulators accounted for [ ]of Quickturn's fiscal year 1995 revenues (FF 142). The average list sales price of an emulation system sold in the domestic market by Quickturn for all types of System Realizer™ products is approximately[ ] (FF 172). As of December 31, 1995 Quickturn had more than[ ]million invested in fixed assets to operate its hardware emulation system business (FF 163). Quickturn presently has a total employee count of approximately[ ](FF 163). It has about [ ]people in its sales force in North America which includes[ ]account managers who are "salespeople down in the trenches." (FF 143).

After an original RPM (Rapid Prototype Machine) product was sold in 1990 by Quickturn and which was a nearest-neighbor product based on the '353 patent (FF 466), Quickturn's hardware logic emulators have used the partial crossbar interconnect architecture claimed in the '473 and '496 patents (FF 19). Although Quickturn has been in the business since 1987, it did not show a profit until[ ]and from its beginning through 1995, it

showed a net[ ](FF 162). In 1995 Quickturn's U. S. sales revenue for emulation was approximately[ ]million (FF 139, 152)[53]. While Quickturn's gross profits for the first quarter of 1996 were $15,963,000 compared to gross profits in the first quarter of 1995 of $12,453,000 (FF 159),[

](FF 160).

Quickturn has directly spent approximately[ ]million in the United States on research and the development of its hardware logic emulation technology. Such money does not include money spent acquiring technology from others (FF 145, 146). Research and development is the life blood of any company like Quickturn which has some[ ] research and development employees (FF 149). Quickturn depends upon its ability to bring out new products on a timely basis for its customers and anything that adversely impacts research and development can affect the ability of Quickturn to bring out new products which is essential to Quickturn's survival (FF 148, 149, 175). Money invested in Quickturn supports Quickturn's research and development and investors hope that Quickturn will develop a product that is acceptable and be rewarded. Investors in Quickturn [

](FF 151). Quickturn still has not gotten to a positive total profit position (FF 145). Also [ ]

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[53] The year 1995 was a good year for Quickturn and its target business model for each of the third and fourth quarters of 1996 calls for a gross profit margin of[ ]percent (FF 157, 170). Quickturn, however, is a public company and hence it has to plan for success. Very rarely will one see a company plan for its downfall and one of the reasons Quickturn made an aggressive 1996 plan is to[ ](FF 170).

[ ] A company such as Quickturn is concerned about its reputation in the stock market and the price of its stock because the stock itself can be used for capital in its dealings (FF 361). When Quickturn missed its quarterly revenue goals in 1994, Quickturn's stock price lost more than half of its value, dropping to approximately six dollars per share from a price range of twelve to fifteen dollars per share (FF 298). A drop in stock price can not only deprive Quickturn of access to investor funds (FF 175) but also can cause [

](FF 148, 298, 352-355, 360).

ii. Respondents Mentor/Meta

Respondent Mentor was established in 1981 and is in the integrated circuit (IC) and system design markets. Thus it designs, manufactures, markets and distributes electronic design automation (EDA) software[54] and provides professional service supporting its customers' complete design environments (FF 54, 266). Mentor, a world leader in electronic hardware and also in software design solutions (FF 54), has a broad design automation product line which includes design simulation and design verification products (FF 281). The company is a leader in worldwide EDA sales, with revenues of[ ]as reported for December 15, 1994 thru December 15, 1995 (FF 54, 246). Mentor's systems enable engineers and designers to analyze, design and test custom IC's, application-specific integrated circuits (ASICs), printed circuit boards, multichip modules, and other electronic systems and subsystems (FF 246).

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[54] Software is a series of computer instructions, viz. a computer program. An example of EDA software is [

] (FF 286).

Mentor, as of December 15, 1995, was the first EDA vendor to win the STAR (Software Technical Assistance Recognition) award and the only EDA vendor to win the award twice. The STAR award is given annually by the Software Support Professionals Association (SSPA) for service excellence. As of December 15, 1995 Mentor employed approximately[ ]people. In addition to its corporate office in Wilsonville, Oregon, Mentor has sales support, software development and professional services offices worldwide (FF 54).

Respondent Meta, a French company based in Paris France (FF 244), was[

]The Meta system uses [

](FF 244).

[

]

[

]by letter dated May 28, 1996 Mentor's counsel notified the administrative law judge that final approval has been received from the French government and that the acquisition of Meta by Mentor was completed in late May 1996 (FF 71).

A joint press release, dated December 14, 1995 from Mentor and Meta represented that Mentor, "one of the main electronic CAE suppliers" with a revenue over 356 million dollars, had just announced the acquisition of Meta which specialized in hardware emulation of integrated circuits; that the acquisition is scheduled to be finalized at the end of January 1996; that Mentor will commercialize Meta products throughout the world; that Meta evaluates the worldwide market of hardware emulation as up to 100 million dollars; that in order for the Meta emulation system to be exported, Meta needed a partner; that the strong engagement of Mentor towards co-design and concurrent design of hardware and software has been a determining element of Meta's decision to join Mentor because emulation is "a step to this process;" and that Mentor has indeed an extremely offensive strategy on co-design (FF 55).

On December 15, 1995 Mentor and Meta announced the introduction of the Sim Express™ hardware logic emulation machine which has been made available by Mentor to

U.S. purchasers since January 1996 (FF 53)[55]. The press release stated that the Sim Express™ is a best-in-class hardware emulator which offers designers 11X faster compile times than provided by "traditional emulation approaches;" that Sim Express™ will become available on a worldwide basis pending Mentor's acquisition of Meta which was scheduled to close January 1996; that Sim Express™ offers designers extremely high-speed design iterations through the compile-run-debug phases of emulation which capability allows designers to incorporate emulation at the gate level which is much earlier in the design process than traditional approaches; that the Sim Express'™ speed advantage enables designers to perform multiple design turns in a single day instead of waiting days or weeks to view the emulation results of a design change; that the Sim Express™ has a rich design debug environment; and that Sim Express™ is available from Mentor worldwide beginning January 1996 (FF 54). Mentor has existing plans to market and distribute hardware logic emulation systems in the United States (FF 245). In accordance with those plans Mentor has actively solicited sales, marketed and sold Meta emulation systems in the United States through its sales and support network (FF 58). Mentor intends to use its present sales force to market emulation products and Mentor[

]

[55] Mentor's U.S. list prices for the Sim Express™ [

](FF 54).

[

](FF 69, 70).

[

]

[56] [

]

[

](FF 84).

[

] Since the beginning

of 1996[

](FF 83). In 1996 Mentor/Meta

competed for sale of a hardware emulation system to[ ]In spite of the

fact that Quickturn[ ]to[ ]Quickturn lost out to

Mentor/Meta (FF 256 to 264).

Meta, in order to have the accused products imported into the United States,[

](FF 58).

Mentor has entered the hardware emulation business[

]

[

](FF 243).

iii. Quickturn For The First Time Has A Real Competitor In Mentor/Meta

Quickturn is the [ ]in emulation. However, while[

](FF 2, 4, 244)[57]. Thus Mentor and Meta plans to sell[ ]emulation units in the U.S. market in 1996 (FF 299, 301-304, 306). Those sales will have a revenue impact on Quickturn (FF 308). Quickturn is essentially a one product (emulators) company while Mentor/Meta in addition to marketing emulators in the United States designs, manufactures, market and distributes electronic design automation software (EDA). While Quickturn's fiscal year 1995 revenues totaled $81.8 million, which was derived from sales and support of hardware logic emulators (FF 140) and its current revenues in cash and investments are[ ]million (FF 141), Mentor had a yearly revenue of over[ ](FF 54, 246) and has current reserves in cash and investments of about[ ](FF 242). As compared to Quickturn, Mentor has approximately[ ]the available cash equivalent[ ] to [ ]million) and Mentor's customer base is something[ ]to Quickturn's less than [ ](FF 291). In terms of sales, Mentor is approximately[ ]bigger than Quickturn (FF 271). Mentor has[ ]in its U.S. sales force (FF 272, 281, 283). In slides presented to[ ]

[57] Mentor has acquired Meta (FF 71). Hence,[ ]

[ ](FF 297).

In the[ ]accounts where Mentor has installations of design automation software, potential customers of emulators have the opportunity to call Mentor before making a final decision about purchasing an emulator and this can happen even in cases where Quickturn's account manager had invested months selling Quickturn to the potential customer and helping the potential customer understand the value of emulation (FF 272, 280). Respondents Mentor/Meta are in the U.S. market with sales of emulators alleged to be superior to Quickturn's System Realizer™(FF 254, 255, 307, 364-374). Mentor also[ ](FF 286). While Quickturn has spent some[ ]in the United States on research and development of its hardware logic emulation technology (FF 145, 146) respondent Meta has spent approximately[ ]million to develop the accused product (FF 56)[58]. Respondent Meta was [ ](FF 57).

Mentor and Meta are also working on[ ](FF 68, 89). Mentor's acquisition of Meta[ ](FF 283). Thus,[ ]

[58] Quickturn's research and development expenditures in the first quarter of 1996 only amount to [ ] (FF 147).

(FF 241, 269, 287, 288). Quickturn does not have any software to sell.[59] Moreover, because of Mentor's design automation products which a customer is likely to need, Mentor is in a lot of accounts. In half of Quickturn's international accounts, Mentor has been selling software products to customers in those accounts for years (FF 269, 274). In addition, the accused products[ ] (FF 134). Hence, while a hardware logic emulation system[

](FF 108, 110, 118, 253). Prior to Meta/Mentor's entry into the U.S. market, the record does not show an emulator with those capabilities from any other alleged competitor of Quickturn.

d. Life Cycle Of Complainant's Product

In the domestic industry in issue, the sooner a company that is alleged to have superior technology gets into the emulation market, the larger its market share and its ability to compete in the market (FF 177, 372). The life cycle for hardware logic emulation system is approximately[ ]years and Quickturn's current hardware logic emulation system (the System Realizer™) was introduced in late 1994. [ ] There is testimony, in particular from Mentor/Meta[60] and a Mentor press release, that the accused emulators are[ ]to Quickturn's System Realizer™ emulator (FF 255, 307, 366-374); that the Sim Express™, which was

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[59] [

](FF 289).

[60] This included testimony from Mentor's CEO Rhines (FF 366) and Mentor's Kenney who testified on Mentor's sales ability.

introduced in January 1996,[

](FF 365, 366).

[

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[

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[

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i. Quickturn's System Realizer™ Is [ ]

[

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[

] It is close customer contact that leads to future follow-on sales (FF 351). Moreover, any delays in domestic sales as a result of competition from Mentor/Meta because of the alleged superior product of Mentor/Meta is as bad as an order lost, in terms of impact on the quarter in which the order was expected. [

]

[

]

Based on the foregoing, it is found that the domestic industry, illustrated by the System Realizer™ which accounted for[ ]of Quickturn's fiscal 1995 revenues (FF 142), is particularly sensitive to competition from the Mentor/Meta in the critical period.

e. Specific Lost Sales To Respondents

Both Mentor and Quickturn market their products through direct sales forces in the United States, and Mentor[

](FF 268). Specific sales Quickturn lost to respondents are relevant to the extent that they have bearing on the harm that would be suffered by the complainant in the critical period. It is undisputed that Bull in Arizona is using an accused product purchased from respondent Meta and which was installed at Bull's Arizona facility in approximately September 1995 (FF 77). [

]

[61] Field Application Engineers, also called FAEs, are engineers who participate in the process of selling Quickturn's products and provides services to customers to set up and maintain the emulation products that are involved in any sale (FF 126).

[

]

It is undisputed that[

](FF 256 to 264).

In the first quarter of 1996,[

](FF 312). When

Mentor/Meta wins a new account,[

]

[

]

Because of the relatively high cost of emulators,[

]

331). The time to complete a sale of an emulator can be as short as[ ]months, but the average Quickturn has seen is[ ]months. [

]

While any sales in the international market will not be affected by the issuance of any temporary exclusion order, sales in the international market have demonstrated[

] Mentor/Meta has presented their emulation product and attempted to sell it in

[ ]

[

] On the international scene[

](FF 324, 326).

With respect to other possible competitors in the U.S. hardware emulaton market, respondents' economic expert Hoffman (FF 85) concluded that Quickturn would not experience irreparable harm using the "narrow definition of the relevant market" of complainant's economic expert Folsom (FF 95). He testified that "the market is becoming much more competitive due to the recent entry by Synopsis merged with Arkos, Zycad, Aptix and Virtual Machine Works [VMW] merged with IKOS" (RX 755 at 8)[62]. The administrative law judge finds that the record establishes that those companies are not a competitive force in the relevant U. S. industry. Thus, Hoffman also testified that it was his understanding that the only companies that are currently delivering or are current suppliers of emulation systems are complainant, respondent Meta and VMW (FF 206).[

]those companies do not pose a serious threat to complainant because of their limited emulation

[62] The administrative law judge earlier in this initial determination has found that the domestic industry in this investigation consists of hardware logic emulators. See section 7 b. i., supra.

product lines and limited resources (FF 207). Thus, Quickturn has never lost an order to [ ](FF 207, 212, 213)[63] [64]

Quickturn has lost three sales because of competition from[

]

[63] [

]

[64] [

]

[

]

While respondents' Hoffman made reference to[

]

[

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[ ]

Having additional competitors in the hardware logic emulation marketplace[

] This has been shown by the presence of Mentor/Meta in the emulator market (FF 279, 323, 324, 334). Mentor/Meta has[ ]in international accounts[ ](FF 323,

324, 334). Moreover, even where[

]

[

]

Referring to[

]

[65] A prospective customer's criteria in selecting an emulator includes not only technical considerations but also customer support and the price aspect. The price aspect can be a strong bargaining tool (FF 338).

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g. Issue Of Quantifiable Harm

The possibility that adequate compensatory or other corrective relief will be available at a later date, in the ordinary course of litigation, may be a factor to consider in any claim of irreparable harm. Virginia Petroleum Jobbers Association v. FPC, 259 F.2d 921, 925 (D.C. Cir. 1958). Thus, such harm may not be irreparable if a complainant will have the possibility of obtaining monetary damages for the activities of any respondents. Loss from any price erosion or through lost sales may be quantifiable. See W.L. Gore & Associates,

Inc. v. Carlisle Corp., 198 USPQ 353, 358 (D. Del. 1978) and AMP Inc. v. Lantrans Inc., 22 USPQ2d 1448 (C.D. Calif. 1991); Electrical Connectors, Unreviewed ID at 103.

The nature of the patent grant, however, does weigh against holding that monetary damages will always suffice to make the patentee whole, Hybritech, 849 F.2d at 1456-57, 7 USPQ2d at 1200. Thus, Congress has authorized district courts in patent cases to grant injunctions "in accordance with the principles of equity to prevent the violation of any right secured by patent, on such terms as the court deems reasonable" on the ground that injunctive relief preserved the legal interest of the parties against future infringement which may have market effects never fully compensable in money. Hybritech, 849 F.2d at 1457, 7 USPQ2d at 1200.

Based on testimony of respondents' economic expert Hoffman, respondents argued that Quickturn will suffer no irreparable harm because the threatened injury can be quantified, and thus compensated for in damages. (RBr at 76-78). Hoffman's credibility however on this issue is suspect in that he testified (Tr. at 2554-56):

> Q. As you sit here today are you able to give us a definitive answer as to whether or not Quickturn would be irreparably harmed if it was deprived of all sales during the period of the investigation?
>
> A. Well, as I have said, I think you can, even in that implausible hypothetical. I think you can quantify it from the perspective of after the fact, and you understand what Quickturn was able to do from that point forward. Obviously if a different scenario prevails, you would want to apply that scenario.
>
> Q. Well, let me take the hypothetical one step further. If as a result of Mentor-Meta's competition during the investigatory period Quickturn is put out of business. Under your theory, that still would not constitute irreparable harm, would it?

A. Quickturn is put out of business and nobody buys the assets, nobody buys the installed base, nobody hires away the engineers and sales people?

Q. Assume that there's a fire sale and its assets are sold, it is liquidated.

A. It is liquidated. All right. However whatever it gets in the liquidation represents the actual scenario, what it would have achieved in terms of market value or long term profits discounted back to the present is the alternate scenario. You compare the two. Obviously that would be, you know, a number a lot bigger than any other hypothetical I could imagine, but it would be a number.

Q. Is it your testimony that since it's a number it's not irreparable harm; is that right?

A. You could quantify it, and I guess you might have a question as to whether Mentor is able to compensate that number at that point.

Q. All right. Assume that Mentor has a deep pocket and was able to pay it under your theory. Sir, I just want to get an answer to a question.

A. I think you have my answer, that, you know, the only question that I would have would be whether Mentor could pay it if that's not at issue as well, then we've quantified it and we have found the mechanism to compensate.

Q. And there would be no irreparable harm under your theory?

A. That's right. [emphasis added].

Hence, according to respondents' Hoffman even the ultimate injury to Quickturn of being forced out of business would not be irreparable harm because even that injury could be quantified and compensated.

In contrast to the testimony of Hoffman, as complainant's economic expert Folsom explained it is obvious that Mentor/Meta will have an impact on the prices which Quickturn can charge while the Meta products are being sold,[

] Thus if Quickturn has to cut

its prices because of competition from Mentor,[

] To measure the impact into the future would require that one be able to predict Quickturn's sales into the future as well as the long term price erosion. Based upon Folsom's years of experience he is confident that Mentor would take the position that those damages were "speculative" (FF 344). In addition, while Folsom agreed that price erosion can be quantified in the short run, as Folsom further testified (FF 345): "We don't know what's going to happen to Quickturn's market share in the future." Also, even short-term competition from Meta emulators that purchasers perceive (whether correctly or not) as technically superior to Quickturn's devices could result in the long-term injury to Quickturn's reputation as a technology leader. See RBr at 69, n. 35 where respondents argued that there is a "negative reputation of Quickturn"[ ]

Moreover, in issue are rights of two of complainant's U.S. patents. Complainant has made a clear showing of likelihood of success on infringement, validity and enforceability. When the movant has shown the likelihood that the acts complained of are unlawful, the temporary relief "preserves the status quo if it prevents future trespasses but does not undertake to assess the pecuniary or other consequences of past trespasses." Remedies for past infringement, where there is no possibility of other than monetary relief, and for prospective infringement "which may have market effect never fully compensable in money." Atlas Powder Co., 773 F.2d at 1232, 227 USPQ at 291. Protection of patents furthers a strong public policy advanced by granting relief[

]

In addition, the loss by Quickturn of a sale to Mentor/Meta can result in a loss of positive reputation and referrals to other potential customers. Also, loss of income from lost sales can cause its earnings to drop which not only would hurt Quickturn's reputation in the stock market but also deprive Quickturn of access to investor funds for research and development programs. Hence, Quickturn's market leadership may be lost (FF 175, 361). Moreover, when Quickturn loses a customer it loses communication that it would have had in working with that customer on a regular basis which is extremely difficult to measure (FF 350). The administrative law judge finds that such factors are not quantifiable.

Based on the foregoing, the administrative law judge finds that the potential harm to Quickturn, in the absence of temporary relief, cannot be quantified.

h. Quickturn Has Established Irreparable Harm To The Domestic Industry In The Absence Of Temporary Relief

Based on the foregoing, the administrative law judge finds that complainant has established that Mentor/Meta is its only real competitor; that Mentor/Meta has been successful in competing against Quickturn in the United States which is essentially a one product company; that Quickturn's System Realizer™ is particularly sensitive in that Meta can offer in the critical period a particular complete emulation solution in the market which Mentor/Meta has promoted as being able to compile circuit designs significantly faster than the emulator that Quickturn presently has on the market for 1996; that Mentor has significant monetary resources; that Mentor[

]that Mentor has an established customer base, access to large sales force and is well established in the United States. Based on those factors he further finds

"tiny French company[ ]and that Mentor has spent considerable time and money to develop a business relationship with Meta so that Meta could provide its customers with a new and unique capability (RBr at 79).

The staff argued the potential harm to respondents from the grant of temporary relief can be considered to be insignificant when viewed in light of complainant's high probability of success on the merits and the threat to complainant of irreparable harm absent temporary relief (SBr at 54).

Quickturn is the innovator which brought hardware logic emulation to the United States IC and ASIC industry. Society, in general, has benefitted from Quickturn's technological advances and the availability of those advances to the chip industry. Quickturn has not been repaid for its investment in research and development and its promotional expenditure in bringing its products to the industry (FF 194). Moreover, Quickturn's sole product line is hardware logic emulators. Meta's emulation technology was developed[

](FF 57, 194). Mentor is a leader in worldwide electronic design automation (EDA) software sales and in 1995 had revenues of over[ ]which exceeded[

](FF 54, 55). Meta is no longer a "tiny French company" but rather has been absorbed by Mentor (FF 71). Moreover,[

](FF 290).

Mentor also[

]

[

](FF 375).

Mentor further recognized[

](FF 376).

Based on the foregoing the administrative law judge finds that the balance of harms strongly favors a grant of temporary relief.

9. Public Interest

Regarding the last factor for consideration in any motion for temporary relief, complainant argued that the patent system exists because it is in the public interest; and that section 337's protection against unfair imports exists because it is in the public interest (CBr at 71).

Respondents argued that the public interest in this investigation weighs heavily in favor of denying Quickturn's Motion No. 383-1 because of the harm a temporary exclusion order would cause to the U.S. industries such as semiconductors, multimedia and telecommunication (RBr at 83).

The staff argued that Quickturn is capable of supplying the hardware logic emulation requirements of domestic users; that there is no significant likelihood that temporary relief would substantially impact the industries that purchase hardware logic emulation systems; that it is in the public interest to issue temporary relief to protect a domestic industry's valid and exclusive rights in its intellectual property; and that the statute provides, that in the event of the grant of temporary relief, respondents will be permitted to import the devices under bond and therefore the domestic industry, if it wants to, will have access to the Meta emulators (SBr at 55, 56, Tr. at 4941).

Section 337(e)(1) provides that the Commission may exclude articles from entry into the United States during an investigation "unless, after considering the effect of such exclusion upon the public health and welfare, competitive conditions in the United States economy, the production of like or directly competitive articles in the United States, and United States consumers, it finds that such articles should not be excluded from entry," 19 U.S.C. § 1337(e)(1). Typically in a patent infringement case, the focus of the Commission's public interest analysis should be whether there exists some critical public interest that would be injured by the grant of temporary relief. See Hybritech, 849 F.2d at 1458.

The administrative law judge finds no such critical public interests that would be injured. Thus between 1995 and early 1996, while there has been broad acceptance of

emulation into the EDA market which had not been there before and Quickturn has sold approximately 100 emulation systems in the U.S. market in 1995 (FF 194-196), only a small percentage of the U.S. semiconductor industry uses emulation, due to the high cost of emulators (FF 197). Only about 5% to 10% of semiconductor design projects are suitable for emulation (FF 198). In addition, only about 1 to 2% out of some 20,000 semiconductor design projects in the United States actually use emulation (FF 199). Moreover, Quickturn has greatly lowered the price of emulation products over time and has consistently had this as its company goal. Thus, from a price of about[ ]per gate in 1990-1991, Quickturn steadily reduced the price to about[ ]per gate in 1994, and it is now just under[ ]per gate (FF 200)[66].

Quickturn's emulation system is further capable of serving any of the United States semiconductor industry projects in 1996 which need and can justify the price of emulation. In addition, Quickturn has the capacity to manufacture more systems than could be produced in 1996 (FF 178, 179, 202) and hundreds of U.S. companies use Quickturn emulation products (FF 203).

As to the alleged superiority of the accused emulators, in actual use of an emulation, compile time generally accounts for less than[ ]of the usage time of an emulator (FF 204). Also, the statute provides that in the event of the grant of temporary relief, respondent can import the accused devices under bond. See 19 U.S.C. § 1337(e).

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[66] A current family of Quickturn's System Realizer™ products sells in increments of 250,000 emulation gates. Even though Quickturn does not price on a per gate basis, it's convenient to simply state that the whole family has an average price per gate and thus a 250,000 emulation gate system would sell for just under $1 per gate or just under $250,000 (FF 201).

Finally, a firm owning patents should have the capacity to expand output in response to increases in market demand, and thereby improve its financial position and engage in future product development (FF 205). In light of the record to date, public policy also favors the granting of temporary relief because complainant has established a reasonable likelihood of success in both infringement and validity of the patents in issue. See Smith Int'l, 718 F.2d at 1581.

Based on the foregoing, the administrative law judge finds that the public interest weighs in favor of granting Motion No. 383-1.

10. Bonding

a. Complainant's Bond

Under sections 337(e)(2) and (f)(1), the Commission may require the complainant to post a bond as a prerequisite to the issuance of a temporary exclusion order or a temporary cease and desist order. Commission rule 210.52(c) provides that the Commission, in determining whether to require a bond as a prerequisite to the issuance of temporary relief, will be guided by federal district court practice under Rule 65(e) of the Federal Rules of Civil Procedure (Fed. R. Civ. P.) which governs the posting of bonds in the context of preliminary injunctions. 59 Fed. Reg. 67622-67629 (Dec. 30, 1994). Said Rule 65(c) states in pertinent part that:

> No restraining order or preliminary injunction shall issue except upon the giving of security by the applicant, in such sum as the court deems proper, for the payment of such costs and damages as may be incurred or suffered by any party who is found to have been wrongfully enjoined or restrained.

The purpose of the bond requirement under Fed. R. Civ. P. Rule 65 is to protect the enjoined party from costs and damages resulting from a wrongful injunction while fixing the

movant's liability for such an order. Continuum Co. Inc. v. Incepts, Inc., 873 F.2d 801, 803 (5th Cir. 1989).

Complainant argued that it should not be required to post a bond as a prerequisite to the issuance of temporary relief. It is argued that the pertinent statute provides, by use of the phrase "may require," discretion in the Commission as to whether any bond will be imposed and the Commission recognizes this discretion, citing Commission rule 210.68(a). Complainant argued that courts have used the following factors to determine whether or not to quire a bond: (1) the possible loss to the enjoined party, (2) the hardship a bond will have on the movant, and (3) the impact a bond would have on the enforcement of federal rights, citing Smith v. Board of Election Commr's For Chicago, 591 F.Supp. 70, 72 (N.D. Ill. 1984) which cited Crowley v. Local No. 82, Furniture and Piano Moving, 679 F.2d 978 (1st Cir. 1982) (Crowley) rev'd on other grounds, 467 U.S. 526, 104 S.Ct. 2557, 81 L.Ed. 457 (1984) and Temple University v. White, 941 F.3d 201, 219-20 (3d Cir. 1991). It is argued that "[i]n cases where the likelihood of success is extraordinarily high, this factor may be an additional reason not to require bond," citing Crowley, 679 F.2d at 1000, n. 25, and that application of the facts in this investigation to such guidance supports a conclusion that there should be no bond from Quickturn; and that if Quickturn is required to post a bond, it should not exceed $250,000. (CBr at 71 to 73).

Respondents argued that, although a complainant may not need to post bond where equitable consideration as no likelihood of harm to the respondents or indigence exist, neither situation applies here; that Quickturn with over $80 million in sales and $40 million

in cash reserves is not indigent; and that Mentor and Meta will be significantly harmed if temporary relief issues. (RBr at 87).

The staff argued that the purpose of requiring a complainant to post a temporary relief bond is to deter frivolous motions on temporary relief and the use of such motions to harass respondents, citing Certain Crystalline Cefadroxil Monohydrate, Inv. No. 337-TA-293, Commission Opinion at 9 (January 19, 1990); that the evidence of validity and infringement is strong; that Quickturn is a small entity with limited financial reserves; and that Mentor and Meta, in view of their prior dealings with Quickturn, had reasonable opportunity to consider the subject patents in issue prior to importing the accused goods into the United States, and all parties had reasonable opportunity to prepare for these temporary relief proceedings. Accordingly, the staff argued for a relatively small complainant's bond in amount equal to [

]that the best evidence for estimating respondents' likely profits in the domestic emulation market during the next seven months is the historical experience of Quickturn; that over the last three years, Quickturn's annual net profit margin has been[ ]and Quickturn's average per unit sales revenues in 1995 were[ ]the staff noting that the information regarding respondents' sales and profits is "unreliable;" and that[

]which can be rounded up to[ ] Accordingly, the staff considered $200,000 an appropriate amount of bond for complainant to be required to post to obtain temporary relief.

In view of the strong showing that complainant has made with respect to validity and infringement of the claims in issue; the fact that Mentor and Meta had reasonable opportunity to consider the claims in issue prior to importing the accused goods into the United States, the disparity in size and available resources as between Quickturn and Mentor/Meta coupled with Mentor's resolve to enter the U.S. hardware logic emulator market, and the discretion the administrative law judge has with respect to whether complainant should post a bond, the administrative law judge finds that no bond should be required of Quickturn.

b. Respondents' Bond

Section 337 requires that the Commission determine and impose on respondents subject to temporary relief a bond "sufficient to protect the complainant from any injury," 19 USC § 1337(e)(1) and (j)(3); Commission rule 210.50(a)(3). Complainant argued that in the circumstances of this investigation, the bond should be set at a minimum of[ ]percent of the sales price of any emulation products imported or sold, or services provided, by respondents during the pendency of the temporary relief (CBr at 76).

Respondents argued that their bond should be no more than 11.1 percent on sales of imported Meta devices. It is argued that according to Quickturn's 1995 Annual Report, Quickturn's operating profits for 1995 were 14.3% of sales; that the potential actual loss to Quickturn, however, should be based on Quickturn's sales price, not respondents' sales price; that in one case involving head-to-head competition between Mentor and Quickturn

[ ]

and that applying this same differential to respondents' future importations, the lost operating

profits to Quickturn, expressed as a percentage of respondents' sales, would be[ ] [ ] (RBr at 88).

The staff argued that the purpose of requiring respondents to post bonds if they desire to continue the importation and sale of goods otherwise prohibited by temporary relief is to compensate a complainant for any injury caused by the respondents' continued activities; that Mentor is a relatively large entity with substantial financial reserves, and that Meta is presumably able to tap those financial reserves in order to post a bond; and that the alleged substantial advantage in the compilation speed of the Meta systems over the Quickturn systems which situation, coupled with Mentor's financial and marketing resource, potentially places Quickturn at a competitive disadvantage which threatens to irreparably injure Quickturn during the temporary relief period, especially by inflicting long-term losses thereafter. Accordingly, the staff argued that a substantial respondents' bond be set; that although the evidence does not lend itself to a ready quantification of the amount of bond that would compensate complainant for its harm, there is at least evidence as to an amount that would tend to counteract any price erosion effects from respondents' competition; that the bond should be set in an amount equal to the difference between the discounts Quickturn typically offers in the absence of emulation competition and the discounts Quickturn offers when faced with competition from Mentor and Meta; that Quickturn's Moore testified that Quickturn's discounts begin at about[ ]but increase to[ ]when Quickturn is faced with competition from Mentor and Meta and that taking the difference, respondents should be subjected to a bond of[ ]of the entered value of each Meta emulator imported during the temporary relief period. (SBr at 58, 59).

Unlike the situation with respect to whether a complainant should post a bond, respondents must have a bond imposed if they are to continue to be active in the United States market during the period of temporary relief. There is the indication that respondents will be active in such market, especially in view of the alleged superiority of the Meta device over the Quickturn device. Based on Moore's testimony that when there is no competing product Quickturn would provide a discount in the approximate range of[ ] percent on average but with the Meta device, considering the features it would advertise as superiorities over Quickturn's System Realizer™, the discount would be a [ ] percent figure (FF 176), and taking the difference of the discount when there is no competing product and the discount when Quickturn is competing with Meta, the administrative law judge finds that Mentor/Meta should be subject to a bond of 25% of the entered value of each Meta emulator imported during the temporary relief period.

11. Remedy

Section 337 of the 1988 Trade Act, as amended, authorizes the Commission to grant temporary relief in the form of an exclusion order, a cease and desist order or both. Complainant argued that it has provided ample evidence that respondents are engaged in significant sales and solicitation activities in the United States, have made numerous offers for sale of Meta's emulation systems and intend to import Meta's emulation systems pursuant to any completed sales; that although an exclusion order would prohibit actual importation of Meta's emulations systems into the United States, no exclusion order can stop the damaging solicitation and marketing activities of Mentor. Hence, it is argued that respondents, unless stopped, will continue to engage in activity which constitutes actual infringement; and that to

the extent that Mentor continues to demonstrate Meta's emulation systems using contributorily infringing software components of those systems in the United States, infringement under 35 USC §§ 271(b) and (c) will continue, notwithstanding the issuance of any temporary exclusion order. Hence, complainant argued that the Commission should issue both a cease and desist order and an exclusion order as temporary relief. (CBr at 78, 79).

Respondents argued that there is no basis for a temporary cease and desist order because [ ] and that to the extent that Quickturn requests a cease and desist order to prevent general sales and marketing activities such relief would be outside the Commission's statutory jurisdiction (RBr at 86).

The staff recommended that the appropriate remedy in the temporary relief proceedings is a temporary limited exclusion order directed to Meta emulation systems, in assembled or unassembled form, covered by the asserted patent claims; and that the Commission should also issue a temporary cease and desist order which would prohibit respondents from the selling (except under bond) of Meta emulators present in the United States at the date of entry of temporary remedial order. The staff argued that any relief should not prohibit respondents' marketing and sales activities related to Meta emulators that might be imported or sold under bond and should not cover any replacement parts (SBr at 57; SRBr at 20) See also FF 82.

The administrative law judge concurs with the staff's recommendations.

VIII. FINDINGS OF FACT

A. The Parties

1. Complainant

1. Quickturn is a business entity incorporated under the laws of the State of Delaware, with its principal place of business at 440 Clyde Avenue, Mount View, California. (CX-2, ¶4).

2. Quickturn was founded in 1987. It pioneered the emulation market, Quickturn made its first sales of emulation products in 1989 (Moore, CX-212, Q&A 17; Ostby, CX-211, Q&A 21; Folsom, CX-216, Q&A 22; CX-15 at 6).

3. [

]

4. Respondents' economic expert Hoffman agreed that Quickturn is the market leader in hardware logic emulation systems. (Hoffman, Tr. at 2377).

5. Mr. Folsom estimated that Quickturn commands about[ ]of the domestic market for hardware logic emulation systems; Dr. Hoffman referenced estimates in the[ ]range. (Folsom, Tr. at 3780-81; Hoffman, Tr. at 2411).

6. Quickturn designs, manufactures and sells hardware logic emulation systems. (CX-2, p. 3, ¶5).

2. Respondents

7. Meta is a French company located at 4 Rue Rene Razel, Saclay, France 91400 (Mentor/Meta response to complaint (CX-55, CX-56) p. 4, ¶9).

8. Mentor is a U.S. company incorporated under the laws of Oregon, and its

headquarters are located at 8005 S.W. Boechman Road, Wilsonville, Oregon 97070-9733. (Mentor/Meta response to complaint (CX-55, CX-56) p. 3, ¶7).

B. Importation

9. At least one Meta hardware logic emulation system has already been imported into the United States. (CX-55, CX-56, p. 20, ¶94).

10. One emulation system manufactured by Meta has been imported into the United States by Bull Information Systems in Phoenix, Arizona (Mentor/Meta response to complaint (CX-55, CX-56, p. 5, ¶13).

11. Mentor has imported a Meta hardware logic emulation system into the United States and installed it at Mentor facilities in Oregon (Mentor/Meta response to complaint (CX-55, CX-56, p. 6, ¶16).

C. The Products At Issue

12. Hardware logic emulation systems can consist of reconfigurable logic devices and "interconnect resources" which are programmed primarily via software to emulate an integrated circuit design, resulting in substantial savings of time and money during the design of integrated circuits (CX-55, CX-56, p. 2, ¶5).

13. Hardware logic emulators may be particularly useful in verifying designs for application-specific integrated circuits (ASICs), custom chips and multi-chip systems (CX-55, CX-56, p. 3, ¶6).

D. Prior District Court Proceedings

14. In the summer of 1995, Quickturn prepared and filed a complaint in the District Court for the Northern District of California (Civil Action No. C95-01934 EFL), charging Meta with infringement of United States Letters Patent No. 5,109,353 (Sample '353

patent), United States Letters Patent No. 5,329,470 (Sample '470 patent) and the '473 patent (CX-55, CX-56), p. 6, ¶18).

15. On October 27, 1995, Mentor filed a declaratory judgment action against Quickturn in the District Court for the Northern District of California (Civil Action No. C95-03867 SI), alleging that Quickturn's Sample '353 patent, the '473 patent and Sample '470 patent are invalid and not infringed by Meta's hardware logic emulation systems. Mentor's declaratory judgement complaint was served on Quickturn on December 18, 1995. Quickturn has since moved to strike a number of Mentor's allegations, and seeks a more definitive statement with respect to other of Mentor's allegations (Mentor/Meta response to complaint. Mentor subsequently dismissed this action and filed a declaratory judgment action in the District of Oregon. Quickturn then filed suit against Mentor and Meta in the Northern District of California (CX-55, CX-56, p. 6, ¶19).

16. Quickturn sued Pie Design System (PiE) on various patents including the '473 patent (CX-5) in the U.S. District Court, Northern District of Calif. PiE cited substantial amount of prior art in that litigation, which was cited to the PTO in the prosecution of the '496 patent and made of record in the '496 patent (CX-6). PiE and Quickturn executed a consent judgment in which inter alia PiE admitted that the '473 patent inter alia was valid and has been infringed and Quickturn dismissed with prejudice its complaint against PiE. (CX-61 at QM48295-48300)

E. Domestic Industry

17. Respondents are not disputing the existence of a requisite U.S. industry under the terms of section 337 in the temporary relief phase of this investigation, with respect to Quickturn's current products being covered by the patents in issue and with respect to

Quickturn satisfying the economic requirements section 337. (Tr. at 1732-1733).

18. Quickturn's research and development facilities, as well as its manufacturing plants, are located within the United States and are engaged in commercial quantity manufacturing of hardware logic emulation systems. (Ostby CX-211; CX-2, complaint, pp. 43-45, ¶¶ 101-105).

19. After the original RPM (Rapid Prototype Machine) product was sold in 1990 and which was a nearest-neighbor product, Quickturn's hardware logic emulators have used the partial crossbar interconnect architecture. Claim charts CDX-9, CDX-10, CDX-11, CDX-12 and CDX-13 read the claims in issue on those emulators. (Butts CX-210, Q&A 61, CDX-9 to 13, Sample Tr. at 1223; Moore CX-212, Q/A 18, 22).

20. Quickturn manufactures and sells four kinds of hardware logic emulation products which includes the Enterprise™, the System Realizer™ , the Logic Animator™ and the MARS™ III Emulation System. (CX-2, ¶ 34; CX-28, ¶2).

21. Quickturn's principal product is the System Realizer™ family of hardware logic emulators (RX-134, Quickturn 1995 Annual Report at 4).

22. Quickturn's Enterprise™ emulation systems, which include the Model LC60 and the Model 330, can emulate IC designs having anywhere from[ ]logic gates. The Enterprise™ Model LC60 is a portable logic emulation system with a capacity of up to[ ]logic gates. The Enterprise™ Model 330 is an expandable emulation system with up to[ ]logic boards, each of which has a capacity of[ ]gates. (CX-2, ¶ 35; CX-28, ¶¶ 10-14).

23. Each logic board in both the Model LC60 and Model 330 emulation systems of Quickturn supports logic chips and switch chips. The logic chips are commercial FPGAs

(field programmable gate arrays) manufactured by a company called Xilinx. The switch chips are Proprietary Multiplexing Interconnect Chips (MICs) which interconnect the FPGAs, using a partial crossbar interconnect architecture. Multiple logic boards in the Model 330 are linked via a second level of MIC switch chips. Enterprise™ emulation systems include automatic partitioning and routing software, a target interface structure and debugging capability in the form of a pattern generator and logic analyzer are also supplied. (CX-28, ¶¶ 10-14 and Attachments D and E thereto; CX-2, ¶ 36).

24. Quickturn's Realizer™ product line consists of several models starting with the System Realizer™ Model M250 through the System Realizer™ Model M3000. The System Realizer™ Model M250 can emulate a circuit design with up to[ ]gates. The Model M3000 offers a total capacity of up to[ ]emulation gates. (CX-2, ¶ 37; CX-28, ¶¶ 15-19).

25. All models of Quickturn's Realizer™ emulation system have logic boards with Xilinx FPGA logic chips and custom MIC switch chips interconnected via a partial crossbar architecture. Multiple logic boards can be connected to one another through a second level interconnect composed of MIC switch chips. Realizer™ emulation systems are equipped for automatic partitioning and routing, and have a debugging module and target interface structure. (CX-28, ¶¶ 15-19 and Attachments F-H thereto; CX-2, ¶ 38).

25a. The Logic Animator™ is a[ ]emulation gate capacity product. Like the Enterprise™ and Realizer™ emulation systems, the Logic Animator™ makes use of logic boards with Xilinx FPGA logic chips and custom MIC switch chips interconnected in partial crossbar fashion. Logic Animator™ emulation systems include partitioning and routing software, a target interface and debugging capability. (CX-28, ¶¶ 20-22 and Attachment I

thereto; CX-2, ¶ 39).

26. The MARS™ III emulation system was originally developed by Pie Design Systems (PiE) which Quickturn had sued for alleged infringement of certain patents including the '473 patent. (CX-23). The system has been manufactured and supported by Quickturn since Quickturn acquired PiE. MARS™ III emulation systems are capable of dealing with circuit complexities of between[ ]logic gates. Logic modules in the MARS™ III feature Xilinx FPGA logic chips and Xilinx FPGA switch chips, and a partial crossbar interconnect architecture. Individual logic modules are linked through a second level switch chip interconnect. A target interface and a logic analyzer and tester are included with the MARS™ III emulation systems. (CX-28, ¶¶ 23-27 and Attachment J thereto; CX-2, ¶ 40).

F. Quickturn's Acquisition In 1992

27. Although Mentor's principal product is now electronic design automation software, for a period from the late 1980s to the early 1990s Mentor was also involved in research and development activities relating to hardware logic emulation systems (CX-55, CX-56, p. 3 ¶7).

28. By an Asset Purchase Agreement dated February 28, 1992, Mentor sold to Quickturn all of Mentor's emulation system hardware and software in existence at that time, a prototype of an emulation system, an exclusive ownership of the Butts '473 patent and to the Butts et al. application Serial No. 07/698,734 (the '734 application) which, through continuation practice, ultimately matured into the Butts '496 patent. By the terms of this Asset Purchase Agreement, Mentor transferred its entire hardware logic emulation business (including intellectual property rights) to Quickturn in exchange for $200,000 and Quickturn

stock. The Agreement read in part:

> 3. Liability and Warranty Disclaimers.
>
> 3.1 Liability Disclaimer. Neither Seller nor any of its officers, directors, partners, agents, servants, employees, stockholders, successors, subsidiaries, assigns and/or affiliates (Affiliates) shall be liable to Purchaser, or to any purchaser or user of any products made, used or sold by Purchaser using the Technology for any injury, loss, cost (including professional fees) or damages of any kind suffered by Purchaser or such purchaser or user. Purchaser acknowledges and agrees that the consideration for the rights under this Agreement reflect the allocation of risks provided by this limitation of liability. IN ADDITION, NEITHER SELLER NOR ANY OF ITS AFFILIATES SHALL IN ANY EVENT BE LIABLE TO PURCHASER OR ANY OTHER THIRD PARTY FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL DAMAGES ARISING OUT OF OR IN CONNECTION WITH THIS AGREEMENT, REGARDLESS OF THE THEORY OF THE RELEVANT CLAIM OR ACTION.
>
> 3.2 Warranty Disclaimer. Except as set forth in Section 7.1, Seller transfers the Technology without any warranty or representation and on an "AS IS, WHERE IS" basis. Both parties acknowledge that Purchaser is an expert and the recognized industry leader in the field of emulation technology. SELLER EXPRESSLY DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR THAT THE TECHNOLOGY OR THE OTHER ASSETS ARE OF ANY CERTAIN QUALITY, WILL PERFORM IN ANY PARTICULAR MANNER OR PRODUCE ANY PARTICULAR RESULTS, OR THAT THE TECHNOLOGY OR THE OTHER ASSETS ARE SUITABLE OR ADEQUATE FOR THE PURCHASER'S REQUIREMENTS. Seller also disclaims any warranty as to the validity or enforceability of the patent and patent applications assigned to Purchaser under this Agreement.

(CX-9; CX-55; CX-56, p. 3, ¶8).

29. The Asset Purchase Agreement of February 28, 1992, included, as an attachment, a patent Assignment dated March 2, 1992, which assigned the '473 patent and the '734 application to Quickturn. The Assignment of March 2, 1992, contained express language which assigned to Quickturn the entire right, title and interest to all the inventions

disclosed in the '473 patent and in the '734 application. (CX-9). The assignment read:

> WHEREAS, Mentor Graphics Corporation, an Oregon corporation, having offices at 8005 SW Boeckman Road, Wilsonville, Oregon 97070-7777, is the sole and exclusive owner of the following patents and patent applications (Patents):
>
> U.S. Patent 5,036,473 issued July 30, 1991
> U.S. Application Serial No. 07/698,734, filed 5/10/91:
> U.S. Application Serial No. 07/474,675, filed 2/6/90;
> U.S. Application Serial No. 07/424,075, filed 10/19/89;
> EPC Application Serial No. 89911412.8, based off PCT Application Serial No. US89/04405, filed 10/4/89;
> Japanese Application Serial No. 509,588/89, based off PCT Application Serial No. US89/04405, filed 10/4/89; and
> Canadian Application Serial No. 2,025,096, filed 9/11/90; and
>
> WHEREAS, Quickturn Systems, Inc., a corporation organized under the laws of the state of California, having a place of business at 325 Middlefield Road, Mountain View, California 94043, is desirous of acquiring the entire right, title and interest and to said Patents and the inventions covered thereby;
>
> NOW, THEREFORE, be it known that for good and valuable consideration, said Mentor Graphics Corporation does hereby sell, assign, transfer and set over unto the said Quickturn Systems, Inc. the entire right, title and interest in and to said inventions and said Patents, and any reissue or reissues thereof which may be granted, the same to be held and enjoyed by the said Quickturn Systems, Inc. for its own use and benefit, and for the use and benefit of its successors, assigns, or other legal representatives to the end of the term for which said Patents are or may be granted or reissued as fully and entirely as the same would have been held and enjoyed by said Mentor Graphics Corporation, if this assignment and sale had not been made; together with all claims for damages by reason of past infringement of said Patents, with the right to sue for, and collect the same for its own use and benefit, and for the use and benefit of its successors, assigns or other legal representatives.
>
> THIS ASSIGNMENT dated and effective as of March 2, 1992.

30. Mentor's outside patent counsel in a letter dated July 31, 1990 to Mentor (CRX-47) stated in part:

> We have been searching periodically to try and locate a foreign patent publication indicating whether and when Quickturn filed a patent application. We just found it. The European Patent Office published a European patent application by Quickturn on June 13, 1990 as published specification EP

372,833. From this European specification we learned that Quickturn filed a US patent application on December 2, 1988.

Mentor filed its first application on Mike Butts' invention on October 4, 1988, beating Quickturn by nearly two months.

31. In a declaration in support of Quickturn's Motion No. 383-1 for temporary relief executed on January 23, 1996, Butts stated in part (CX-45):

> 1. I am the Michael R., Butts who is named as one of the co-inventors in U.S. patent No. 5,448,496 (hereinafter "the Butts '496 patent'), which issued on September 5, 1995. I am currently employed by Quickturn Design Systems, Inc., at Quickturn's facility in Hillsboro, Oregon, where I hold the position of senior staff engineer. Prior to joining Quickturn in March of 1992, I was employed by Mentor Graphics Cor. ("Mentor") as an engineer.
>
> * * *
>
> 3. I am fully familiar with the inventions claimed in the Butts '496 patent. Claim 1 is an independent apparatus claim directed to a reconfigurable logic assembly with a "partial crossbar" interconnect architecture for electrically connecting reprogrammable logic devices to each other through reprogrammable interconnect devices. Claims 2 and 3 are dependent claims based on Claim 1. Claim 2 defines the reprogrammable logic devices of Claim 1 as programmable gate arrays. Claim 3 defines the reprogrammable logic devices of Claim 1 as FPGAs. Claim 15 is another independent apparatus claim which adds an interface structure to the reconfigurable logic assembly of Claim 1.
>
> 4. The inventions defined in Claims 1, 2, 3 and 15 of the Butts '496 patent are inventions that I intended to claim in the Butts '496 patent, and they are inventions that were fully disclosed in and supported by the '734 application.
>
> 5. I invented the subject matter of Claims 1, 2, 3 and 15 of the Butts '496 patent during the period that I was employed by Mentor. The '734 application, which fully disclosed and supported the inventions of Claims 1, 2, 3 and 15, was filed while I was at Mentor. My co-inventor on the '734 application, Jon A. Batcheller, who was also a Mentor employee at the time the '734 application was filed, contributed to inventions defined in claims other than Claims 1, 2, 3 and 15 of the Butts '496 patent.
>
> 6. Pursuant to my employment agreement with Mentor, I assigned all of my inventions as disclosed in the '734 application (and its predecessor applications) to Mentor. Attachments A, B and C hereto reflect the

> assignment of rights to my inventions. In this regard, the inventions defined in Claims 1, 2, 3 and 15 of the Butts '496 patent are inventions that I fully intended to convey and did in fact convey to Mentor by way of the assignments in Attachments A, B and C.

32. A terminal disclaimer was filed in the '496 patent to disclaim the terminal part of the '496 patent term which extends beyond the July 30, 2008, expiration date of the co-owned '473 patent. The first page of the '496 patent states that "The portion of the term of this patent subsequent to Jul. 30, 2008 has been disclaimed." This terminal disclaimer was filed pursuant to the requirement of the patent examiner based on the presence of claim 8 in the issued '473 patent. (CX-6, CX-61, QM48254-55). In an August 19, 1994 "Preliminary Amendment," complianant's counsel stated that:

> As discussed with the Examiner via telephone on August 17, 1994, Applicants are filing herewith a Terminal Disclaimer for the above identified application. This Terminal Disclaimer appears necessary because of the presence of claim 8 in Applicants' issued U.S.Patent No. 5,036,473. (CX-61 at QM48253).

G. Quickturn's Possible Acquisition of Meta

33. Quickturn considered a relationship with Meta's Reblewski and Lepape as early as August 1990, when they were still working for Dune Technologies. At that time, Quickturn wanted to "work with these guys", believing that "their main contribution will be the[

] (RX-55, p.QM57433).

34. In a portion of 1994 an 1995, Quickturn and Meta engaged in discussions about[ ] (CX-55, CX-56, p. 4, ¶10).

35. Quickturn's Zafar met with Meta's Reblewski in France on or about April 28, 1994. In preparing for that meeting, Quickturn stated that[

[

]

37. In the discussions between Meta and Quickturn in 1994 and 1995, Meta revealed technical information regarding the operation and development of the Meta system. The technology was described orally to Quickturn's Sample and Zafar by Meta's Reblewski, and both Sample and Zafar also observed a Meta System prototype while in France. (Reblewski, RX-698, Q/A 31).

38. CX-28 is a declaration of Stephen P. Sample executed January 17, 1996, which was submitted by Quickturn, as Exhibit 24 in support of Quickturn's Motion No. 383-1 for temporary relief. The declaration has attachments (A) thru (Q). The declaration with attachments is on the public record at the Commission. Attachment Q is titled "Meta Emulation System Basic Architecture." Sample testified as to that attachment Q (Tr. at 1165):

Q. [

]

A. [

]

39. As to conversations between Quickturn's Sample and Meta's Reblewski, Sample testified (Tr. at 1178-1180):

Q. [

]

42. Quickturn signed a non-disclosure agreement with Meta, agreeing not to use the confidential information provided by Meta for any purpose other than the evaluation of the proposed business relationship. (RX-109). The non-disclosure agreement between Quickturn and Meta was executed at or near a fax date of June 1, 1994 (RX-239; Ostby Tr. at 1623 to 1625).

43. In the fall of 1994, the President of Quickturn, Lobo, traveled to Meta and expressed a continued interest in arranging a business deal between Quickturn and Meta, stating that he would be personally responsible for such an arrangement (Reblewski, RX-698, Q/A. 25).

44. [

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45. [

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46. [

]

47. The Quickturn/Meta discussions broke off in the summer of 1995, when[

](CX-55, CX-56 p. 4, ¶10).

H. Bull As A Customer Of Meta and Mentor's Acquisition Of Meta

48. [

]

49. [

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50. [

]

51. [

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52. [

]

53. On December 15, 1995, Mentor and Meta announced the introduction of the Sim Express™ hardware logic emulation machine. The Sim Express™ machine has been made available by Mentor to U.S. purchasers since January 1996. (CX-74, CX-88, CX-90).

54. A Mentor press release dated December 15, 1995 (CX-74) titled "SIMEXPRESS EMULATOR AVAILABLE WORLDWIDE" reads:

Mentor Graphics Corporation and Meta Systems today introduced SimExpress™ a best-in-class hardware emulator, which offers designers 100X faster compile times than provided by traditional emulation approaches. SimExpress™ extremely short design iteration times are facilitated by a unique architecture based on a full-custom IC designed specifically for hardware emulation.

SimExpress™ will become available on a worldwide basis pending Mentor Graphics' acquisition of Meta Systems which is scheduled to close January 1996. (See "Mentor Graphics To Merge with Meta Systems," Dec. 15, 1995.)

"SimExpress™ offers designers extremely high-speed design iterations through the compile-run-debug phases of emulation. This capability allows designers to incorporate emulation at the RTL or gate level, which is much earlier in the design process than traditional approaches," said Frederic Reblewski, Meta Systems' president and founder.

"With SimExpress™, we focused our efforts on optimizing the entire emulation process, not just fast runtimes," added Reblewski. "Early in the product's development it became obvious that we could not achieve our goals using off-the-shelf FPGAs. Once we made the leap to full-custom ICs, we were able to deliver performance and functionality unmatched by any of our FPGA-based competitors."

Dramatically Reduced Design Compile Times

Partitioning a design into multiple programmable chips and then routing the interconnect between those chips is a complex task. The architecture of the chip and its interconnect resources has a huge impact on the efficiency of the compiler that must partition and route the design.

SimExpress™ design compilations, when performed on a single workstation, are typically 100X faster than traditional emulation systems. SimExpress™ compiles designs faster on a single workstation than other emulators can on multiple (up to 75) workstations running in parallel. This speed advantage enables designers to perform multiple design turns in a single day instead of waiting days or weeks to view the emulation results of a design change.

Rich Design Debug Environment

One of the major benefits of hardware emulation, when compared with building an actual prototype, is the ability to view inside the design to isolate the source of a problem. The SimExpress™-on-chip logic analyzer takes simultaneously providing visibility to every net in the design. This eliminates the need to predetermine which nets to view prior to the design compile and no requirement to suffer a lengthy re-compile should additional nets be required during debug.

Total design visibility speeds the debug phase of the design iteration loop by presenting the user all the data needed to isolate a problem. It also frees the designer from the task of predetermining which nets will be viewed during debug and from the task of inputting the list of nets.

Leveraging Hardware Emulation Throughout the Design Process
SimExpress'™ fast design iteration enables designers to spend more time utilizing the emulation hardware and less time waiting for the design to be compiled. These features, when combined with the ability to emulate both RTL and gate-level designs, and high-speed fault emulation, promote the use of emulation throughout the design process. SimExpress™ is not restricted to the final verification phase of design.

Price And Availability
SimExpress™ is available from Mentor Graphics worldwide beginning January 1996. U.S. list prices start at $100,000 for a 50,000-gate configuration. Software is available on SUN OS, SUN Solaris, and HP platforms.

Meta Systems (Saclay, France) was established in 1991. The founding members of the company have focused their research and development on speeding hardware emulation design turns through the use of full-custom ICs, rather than take the traditional approach of using commercial FPGAs.

Established in 1981, Mentor Graphics Corporation (NASDAQ:MENT) designs, manufactures, markets and distributes electronic design automation (EDA) software and provides professional services supporting its customers' complete design environments. The company is a leader in worldwide EDA sales, with revenues of $370,117,000 over the last reported 12 months. Mentor Graphics is the first EDA vendor to win the STAR (Software Technical Assistance Recognition) award, and the only EDA vendor to win the award twice. The award is given annually by the Software Support Professionals Association (SSPA) for service excellence. The company currently employs approximately 2,045 people worldwide. In addition to its corporate office, Mentor Graphics has sales, support, software development and professional services offices worldwide. The company's headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.

55. A joint press release (CX-10, CX-11) dated December 14, 1995 from Mentor and Meta read:

MENTOR GRAPHICS ACQUIRES THE FRENCH COMPANY META SYSTEMS

Mentor Graphics, one of the main electronic CAE suppliers (with a revenue over 356 million dollars) has just announced the acquisition of the French

Company Meta Systems, specialized in hardware emulation of integrated circuits. The conditions of the acquisition, which is scheduled to be finalized at the end of January 96, have not been disclosed. Meta Systems, employing 13 people, will remain in France and will operate as an independent subsidiary of Mentor Graphics. Mentor Graphics will commercialize Meta products throughout the world, but the commercial marketing will continue to be ensured in France. Meta Systems, which has nearly reached 30 million Francs in 1996, is expecting a revenue of approximately 60 million francs (12 M$) for next year, with 40% achieved in Europe. The company evaluates the worldwide market of hardware emulation up to 100 M$, a market held at 80% by the American Company Quickturn Design Systems.

Meta Systems was founded in 1991, but its launch in the free market is only dated March 1994 (refer to Electronique Hebdo of March 10, 1994), as it previously worked exclusively for the Ministry of Defense. Since then, its activity for the military sector has strongly decreased. Due to an original technology mainly based on FPGAs developed by themselves, and to a particular architecture (refer to Electronique International Hebdo dated November 24, 1994). Meta Systems has developed high performance systems which have valued into a quick success on the French market. But in order to be exported, the company needed a partner. "The strong engagement of Mentor Graphics towards co-design and concurrent design of hardware and software has been a determining element of decision for us to join Mentor Graphics," explained Meta Systems, as emulation is "a step to this process". Mentor Graphics has indeed an extremely offensive strategy on co-design, through its project Systems On Silicon (SOS) initiative. It is mainly within the scope of this strategy that Mentor Graphics has recently bought Microtec Research (cf. EIH dated October 12, 1995), a company specialized in real time systems and development tools for embedded softwares.

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58. Mentor has existing plans to market and distribute Meta hardware logic emulation systems in the United States. In accordance with these plans, [

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]by letter dated May 28, 1996 Mentor's counsel notified the administrative law judge that final approval has been received from the French government and that the acquisition of Meta by Mentor was completed "last week." (ALJ Ex. 1).

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77. In mid-1995, a French affiliate of Bull HN Information Systems, Inc. of Billerica, Mass. (Bull) sought bids from both Quickturn and Meta for an emulation system to be imported from France into the United States. Meta was successful and the Meta emulation system arrived at Bull's facility in Phoenix in approximately September 1995. (CX-55, CX-56, p. 5, ¶14).

78. [

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79. [

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80. A reference account is a customer who is using an emulator and is willing to discuss its experience with that emulator with other companies who may be considering purchasing the same emulator. (Kenney Tr. at 2245).

81. [

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82. [

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design engineer for Application Specific Integrated Circuits ("ASICS") until 1987. Moore then worked for Daisy Systems as a field applications engineer and technical manager selling simulation and hardware acceleration products. (Moore CX-212, Q&A 1-6).

89. In 1990, Moore began working with Quickturn and has held the positions of Account Manager, Regional Manager, Area Sales Director, North America Director of Sales and Vice President of North America Sales, and Moore's duties and responsibilities have included management of the sales force and field applications engineers which sell and support Quickturn's emulation products. Moore reports to Keith Lobo, the President and CEO of Quickturn. Quickturn's entire North America Sales Force reports to Moore through its Area Sales Directors and its Application Engineering Managers. (Moore CX-212, Q&A 7-16).

90. William E. Cibulsky joined Quickturn in May 1994. He is presently the Vice President of International Operations for Quickturn, a position he has held since January 1, 1995. Cibulsky reports to Keith Lobo, the President and CEO of Quickturn. Cibulsky's responsibilities include the management and coordination of Quickturn's international operations and sales activities. Cibulsky also previously held the position of Quickturn's Vice President of North American Sales. (Cibulsky CX-213, Q&A 1-5).

91. Cibulsky graduated from Fairfield University in Fairfield, Connecticut, with a Bachelor of Science degree in mathematics. Upon graduating from college in 1968, Cibulsky joined the Air Force, where he flew as a pilot for nine years, until 1977. In 1976, Cibulsky received a Master's degree from the University of Southern California in Systems Management. Cibulsky has held various other sales and sales management positions at various technology firms since 1977 when he left the Air Force, including positions at SBC,

Digital Equipment Corporation, Apollo Computer, Solomon Design Automation, Vantage Analysis Systems, Inc., Zycad and Arcsys. (Cibulsky CX-213, Q&A 7-11).

92. Cibulsky previously worked at Zycad from 1990 to 1993, and he held the positions of Vice President of North American Sales, Vice President Worldwide Sales, and General Manager European Operations. Accordingly, Cibulsky became familiar with Zycad's operations and its simulation and hardware acceleration products. (Cibulsky CX-213, Q&A 24-27).

93. Raymond K. Ostby is presently Chief Financial Officer and Vice President of Finance and Administration at Quickturn. Ostby's present responsibilities are to plan, organize, direct and control financial and administrative activities at Quickturn. Ostby reports to Keith Lobo, the President and CEO of Quickturn. (Ostby CX-211, Q&A 1-2, 7-8).

94. Ostby received a Bachelor of Science degree in Business Administration with an emphasis in finance from the University of Montana in 1971 and a Master of Business Administration degree from the University of Montana in 1972. In 1976 and 1977, Ostby did further graduate study in stochastic modeling at the University of California, Berkeley, in a Ph.D. program. From June 1985 to June 1991, Ostby was Vice President and Chief Financial Officer at Atmel, a semiconductor chip company, and from June 1991 to September 1993, he was Vice President and Chief Financial Officer of Force Computers. (Ostby CX-211, Q&A 3, 6).

95. James Mack Folsom has been employed by Glassman-Oliver Economic Consultants, Inc. for seventeen and one-half years. Folsom holds a Bachelor of Business Administration degree with a major in Marketing from the University of Georgia. Folsom

attended graduate school at the University of Georgia and at Vanderbilt University, where he completed all the requirements for a Ph.D. in Economics except for the thesis. Folsom majored in Industrial Organization Economics. Folsom is a member of the Southern Economics Association. (Folsom, CX-216, Q&A 1-8).

96. Folsom taught as an instructor at Vanderbilt in the summer of 1959. Beginning in the fall of 1959, Folsom went to Duke University as an instructor. He later became an assistant professor, and was at Duke from 1959 to 1964. During Folsom's last year at Duke he was not teaching but doing research. In September 1964, he went to work as an economist in the Division of Economic Evidence at the Federal Trade Commission (FTC). Folsom stayed at the FTC until December 2, 1978, occupying various positions, including head of the Division of Economic Evidence. This group provides economic input to the antitrust mission of the FTC. Folsom later became Deputy Director of the Bureau of Economics and acting Director of Economics. (Folsom, CX-216, Q&A 9-10).

97. Examples of Folsom's publications include a report he wrote with others when serving as Acting Director of the Bureau of Economics on line-of-business reporting, which is essentially requiring firms to report profits by business activity. He also published a comment on an article in the Agricultural Economic Journal dealing with the state of competition in food retailing and food manufacturing. (Folsom CX-216, Q&A 11).

98. Folsom did work for AMD when they acquired MMI, so Folsom became familiar with some of the products in the semiconductor industry. (Folsom, CX-216, Q&A 12-15).

99. Based on Folsom's experience and credentials, Folsom was qualified as complainants' economic expert in this investigation. (Tr. at 1690-1691).

100. Folsom began work in this investigation on March 26, 1996 and made the following preparations in order to express his opinions on the economic issues in this case. He reviewed and analyzed publicly available documents on emulation, the depositions of Dragani, Garrity, Tarlecki, and Hoteling (Account Managers for Quickturn), Mentor's Kenney, complainant's Ostby, Quickturn's Cibulsky, Lobo (President of Quickturn) and Huang (Executive Vice President of Engineering at Quickturn), Walter Rhines (President of Mentor), Zafar (Vice President Marketing at Quickturn), complainant's Moore, Antle (Consultant and Member of Board of Directors at Quickturn), Tung (Vice President and General Manager of HSD at Mentor), and Reblewski (President of Meta, Volume 3 only) and the exhibits marked therein. Folsom also reviewed the complaint and Motion No. 383-1 for Temporary Relief, along with the appended exhibits. Folsom attended the deposition of Mentor's economic expert Hoffman. In addition, Folsom had discussions with Ostby about complainant's financial data and attended a sales conference at complainant. Folsom had general discussions with complainant's sales staff about how hardware logic emulation systems are sold. Folsom also reviewed sales, financial, marketing and business plan materials of Mentor, Meta and complainant. (Folsom CX-216, Q&A 17-18).

101. Folsom's opinions are based on his assumption that Meta's hardware logic emulation systems, which Mentor is selling and offering for sale in the United States, infringe the patents owned by Quickturn involved in Motion No. 383-1. (Folsom CX-216, Q&A 19).

1. The Relevant Market For Economic Analysis

102. The hardware logic emulation system industry in the United States is an attractive U.S. industry in terms of potential because Integrated Circuits (ICs) and

Application Specific Integrated Circuits (ASICs) are becoming more complex, and in turn the demand for hardware logic emulation systems, which are useful in the design verification of complex products, is expected to grow. [

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103. The hardware logic emulation domestic industry is growing faster than the EDA (Electronic Design Automation) industry. (Folsom, CX-216, Q&A 36; CX-88, p.5).

104. [

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105. A simulator is a software program which executes an algorithm on a general purpose computer for the purposes of verifying the functionality and timing of a design. A simulator is a software product that attempts to simulate the function of a design before it is sent to a foundry to become silicon. (Moore CX-212 at 31, Cibulsky CX-213 at 15).

106. A simulator accelerator is a hardware product that allows a software simulator to run at faster speeds than a software simulator on a work station. Simulation accelerator and hardware accelerator are used interchangeably. Those devices are a special purpose hardware system which executes an algorithm for the purposes of verifying the functionality and timing of a design. IKOS and Zycad are companies which offer those types of devices. They run at speeds in the range of hundreds to the low thousands of cycles per second,

which is several orders of magnitude slower than emulators. (Cibulsky CX-213 at 15-16; Moore CX-212 at 32).

107. The fundamental differences between a hardware accelerator and an emulator relate to speed of operation, underlying technology, and application. Emulators run in the low millions of cycles per second, approximately a thousand times faster than hardware accelerators. This speed differential is due to underlying technology differences. Emulators, unlike hardware accelerators, express the entire design, including interconnect, concurrently in reprogrammable hardware. Therefore, the entire design is processed every clock cycle. Hardware accelerators are characterized by "event queues" which process small parts of the design at a time and swap pieces back and forth out of memory. The application differences between hardware accelerators and emulators are in large part dictated by the speed difference. The speed of emulators enables them to be interfaced directly to a user's target system, if desired. Hardware accelerators are much too slow. Hardware accelerators are generally used for regression testing, that is, verifying the same set of test vectors over and over again against evolving versions of a design, and functional verification only. (Moore CX-212 at 32).

108. For a customer who is going to use an emulator, it would most likely use a simulator and/or hardware accelerator prior to using the emulator. (Kenney Tr. at 2213).

109. [

] Emulators run at speeds which are several orders of magnitude faster than simulators or hardware accelerators. (Cibulsky CX-213 at 16).

110. Emulation products generally do not compete with simulators or hardware

accelerators. Designs of complexity under 100K gates can be managed without emulation, using hardware accelerators or simulators combined with respins of silicon if needed. Emulators are usually not viewed as cost effective below the 100K gate threshold. Above 100K gate complexity, hardware accelerators are usually sold to accounts that must have faster timing verification, whereas emulators are sold for higher speed functional verification and in-circuit emulation. (Moore CX-212 at 33).

111. Emulator is some 10,000 times faster than a hardware accelerator and some 100,000 times faster than the software simulation. Given the speed differential, the accelerator and software simulator are not in direct competition with the emulator. That means that if the price of the emulator goes up, people would not turn to the accelerator or software simulation. (Folsom Tr. at 1718-1721).

112. Every person who has purchased a hardware logic emulation system from Quickturn also has a simulator, so they are not substitutes for one another. When an ASIC (application-specific integrated circuits) reaches a certain size or complexity other technologies such as simulation, hardware acceleration and cycle based simulation, are substantially slower than emulation. Hence these other technologies do not compete in the domestic industry for hardware logic emulation systems having a capacity of 100,000 emulation gates or greater. (Folsom CX-216 at 16, 17).

113. [

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114. Hardware emulation is about 10,000 times faster than current hardware accelerators such as the ZYCAD XP family and Mentor's Hoffman has no basis for

disagreeing with this. (Tr. at 2441 to 2443).

115. [

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116. Mentor's Hoffman has referenced "competition from alternatives" and stated that [

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117. Referring to the preceding finding,[

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[ ]

121. There is a relationship between integrated circuit (IC) complexity and the probability that an IC developer will purchase and use a hardware logic emulation system. That probability increases when the IC under development exceeds 100,000 gates. (Folsom, CX-216, Q&A 46; CX-205 p. 14; Moore, CX-212, Q&A 100).

122. Quickturn's emulation products do not compete with simulators, simulation accelerators or hardware accelerators because Quickturn's emulation product is used further into the design verification stage than any of these products. Emulators run at speeds which are several orders of magnitude faster than simulators or hardware accelerators. (Cibulsky CX-213 at 16; Cibulsky, CRX-49 at 7,8).

123. Hardware logic emulators having a capacity of 100,000 emulation gates or more are sufficiently different from other design verification options that they represent a U.S. industry for economic analysis purposes. (Folsom CX-216 at 13; Folsom CRX-50 at 9, 10).

124. Emulators are complementary to simulators and hardware accelerators. All customers who consider emulators already use simulators and will continue to do so, and most use hardware accelerators as well. Most design teams in the United States use simulation and hardware acceleration in conjunction with emulation, not instead of emulation. (Cibulsky CRX-49 at 7, 8).

125. The issue to a potential customer of an emulation system is not whether to buy it in preference to a simulator or hardware accelerator, but whether the benefit of using emulation in addition to other EDAs is warranted in view of emulation's relatively high costs compared to other EDAs. (Moore CRX-50 at 8, 9).

126. [

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127. Mentor's Kenny in his direct testimony (witness statement) (RX-700) stated:

Q18. Has Mentor Graphics offered for sale any emulation products manufactured by Meta Systems.

A. Yes.

128. [

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129. [

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130. [

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[

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131. Each of the respondents in its response to the complaint stated that for the past two years, "Meta has been designing, manufacturing and selling hardware logic emulation systems known as the Meta-Series 100, Meta-Series 500 and Meta-Series 500M Emulation Systems" (CX-55, CX-56, p. 4, ¶9).

132. A Quickturn Enterprise versus Meta Benchmark comparison was done in early 1994. The design was approximately 70 K gates. It took 26 minutes to compile on Meta versus[ ]on Enterprise. Operating speed was 1.2 Mhz on Meta versus[ ]on Enterprise. (RX-29, p. QM 57701).

133. The major usage of the Meta emulation system is to verify the correctness of the design of a new circuit (McCluskey CX-214, Q&A 16; CX-132, page 2). (CFF118).

134. [

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135. [

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136. The Butts '473 and '496 patents explain how the Butts' hardware logic emulation system -- also referred to as the Realizer System, see, e.g., Butt '496 patent, Col.

1, lines 33-36 (CX-6) -- can serve as the basis for "a new means of building a logic simulator":

3. Realizer System Applications

3.1. Realizer Logic Simulation System

A logic simulator is a system, implemented in hardware or software, which receives an input design, a set of stimulus to the design and a direction to simulate for a period of time, and produces a set of responses which predict those that a real implementation of the input design would produce given the same stimulus. The stimulus and responses are in the form of logic state transitions of specified design nets at specified times. An important characteristic is that the simulator user provides only the description of a design in the form of the input design file, so the design may be changed and resimulated in short period of time.

Current software logic software simulator design practice is to use a computer software program, executing a sequential algorithm which predicts the design's operation ("An Introduction To Digital Simulation," Mentor Graphics Corp. Beaverton Oreg. 1989). Either the event-driven or compiled or compiled code algorithm, which are well known, are used. Current hardware logic simulator design practice is to build hardware which executes the same event-driven or compiled code sequential algorithms used in software simulators. The hardware gains its performance advantage only by exploiting parallelism in the algorithm and/or directly implementing special algorithmic operations, which are not possible for a general-purpose computer executing software. Current hardware logic simulators operate by executing an sequential algorithm which predicts the input design's responses.

A new means of building a logic simulator is based on the Realizer System. The Realizer logic simulator system receives a input design, which it converts into a configuration of the Realizer hardware's logic interconnect chips, using Realizer design conversion system. It receives a set of stimulus to the design and a direction to simulate for a period of time, applies that stimulus to the Realized design via Vector Memories, and collects a set of responses from the Realized design via Vector Memories. The response correspond to those that a real implementation of the input design would produce given the same stimulus, because an actual hardware realization of the design is observed responding to that stimulus.

> This differs fundamentally from all current logic simulation systems, in that they execute a sequential algorithm which predicts the design's responses to stimulus, while the Realizer logic simulator operates a realization of the design to determine the design's responses to stimulus. The primary advantage is that the realized design generates responses many orders of magnitude faster than a sequential algorithm can predict responses.

See, e.g., Butts '496 patent, col. 67, lines 1-55 (CX-6, emphasis added). Hence, the hardware logic emulation system of the Butts '473 and Butts '496 patents,[

]provides emulation capabilities and can also perform as a logic simulator.

137. The hardware logic emulation system of the Butts '473 and Butts '496 patents is a design and debug verification tool, the goal of which is to provide a functional realization of user's circuit design:

> The present invention relates to the use of electronically reconfigurable gate array logic elements (ERCGAs) and more particularly relates to a methodology that includes interconnecting a plurality of such logic elements, and converting electronic representations of large digital networks into temporary actual operation hardware form using the interconnected logic elements for the purposes of simulation, prototyping, execution and/or computing.

See, e.g., Butts '476, Col. 1, lines 19-29 (CX-6, emphasis added). Thus, the hardware logic emulation system of the Butts '473 and Butts '496 patents has some functionality traditionally attributed to software simulation tools, and can be used to actually design and debug the user's circuit design, like a computer software simulator. At the same time, the Butts hardware logic emulation system can run at very fast speeds to perform emulation. See Butts '473 patent, Col. 69, line 49-Col. 76, line 52 (CX-5) and Butts '496 patent, Col. 67, line 1 to Col. 74, line 22 (CX-6).

2. Nature Of Quickturn And Effect Of Mentor/Meta

138. In 1990, Quickturn was selling an emulation product called RPM (Rapid Prototype Machine) which was a "nearest neighbor" product. Quickturn presently sells emulator product lines using the partial crossbar interconnect architecture which includes the System Realizer™, Enterprise™ and the MARS™ III Emulation Systems along with accompanying software and peripheral products. Quickturn also provides and sells services for the set-up and on going use of its emulation products at customer sites (Moore CX-212, Q/A 18, 22; Butts CX-210, Q/A 61). Its fiscal year 1995 revenues totaled $81.8 million (RX-134 at 4).

139. In 1995, Quickturn's U.S. sales revenue for emulation was approximately[ ] million. Quickturn's U.S. sales target for 1996 is approximately[ ] (Moore CX-212, Q&A 23-26; Ostby CX-211, Q&A 10).

140. Quickturn's fiscal year 1995 revenues of $81.8 million, compared to sales of $65.5 million in 1994, were derived from sales and support of hardware logic emulators. (RX-134, Quickturn 1995 Annual Report at 1, 4, 15).

141. Quickturn's current revenues in cash and investments total[ ]million. (CX-15 at 9).

142. The System Realizer™ family of hardware logic emulators accounted for 83% of Quickturn's fiscal year 1995 revenues. (RX-134, Quickturn 1995 Annual Report at 15).

143. Quickturn has about[ ]people in its sales force in North America and that includes approximately[ ]account managers who are "salespeople down in the trenches." Quickturn has roughly in North America[ ]applications engineers, four applications engineer managers and four area sales directors. (Moore Tr at 1527, 1528).

144. Field Application Engineers, also called FAEs, are engineers who participate

in the process of selling Quickturn's products and provide services to Quickturn's customers to set-up and maintain the emulation products Quickturn sells. (Moore CX212 at 9).

145. Quickturn has invested millions of dollars in research to develop emulation systems, and it hopes "to get that money back." [

] (Folsom, CX-216, Q&A 27, 120).

146. Quickturn has directly spent approximately [ ]million in the United States on research and the development of its hardware logic emulation technology. This does not include money spent acquiring technology from others. Those sums are summarized on an annual basis as follows:

Year	Amount ($K)
1988	[ ]
1989	[ ]
1990	[ ]
1991	[ ]
1992	[ ]
1993	[ ]
1994	[ ]
1995	[ ]
Total	[ ]

(CX-15 ¶ 16; Folsom, CX216, Q&A 23).

147. Quickturn's R&D expenditures in the first quarter of 1996 were[ ] million, compared to[ ] million in the first quarter of 1995. (RX-729, p. QM108464).

148. If Quickturn cannot invest sufficiently in R&D, Quickturn will not be able to keep up with emulation competitors and will not be able to meet the needs of future customers. Perhaps more importantly, if Quickturn loses revenue dollars to Meta, it will mean that Quickturn will miss its quarterly revenue targets. [

]

[

] (Moore CRX-50 at 25, 26).

149. Research and development is the life blood of a company like Quickturn. Quickturn has[ ]research and development employees as compared to[ ]sales and marketing employees. Quickturn depends upon its ability to bring out new products on a timely basis for its customers, and anything that adversely impacts R&D will irreparably harm the ability of Quickturn to bring out new products that are essential to its profitable survival. (Ostby CX-211 at 4 to 6; Folsom CX-216 at 42).

150. Entry into the hardware logic emulation domestic industry is now apparently poised to occur at a rapid pace. As a result, Quickturn's investment in its patents and hardware logic emulation technology[

] (Folsom CX 216 at 43).

151. For Quickturn, investors put out money for Quickturn's research and development. They do so with the hope that Quickturn will develop a product that was acceptable. The investors hoped to be rewarded. [

] (Folsom CX-216 at 54).

152. Quickturn's sales in North America in 1995 were $56.1 million, compared to total sales of $48.6 million in 1994. (RX-134, p. 1).

153. Quickturn projected in its[ ]that its own revenues would grow by about[ ](RX-119, JX-10, Lobo Tr. at 7-68, 176).

154. Quickturn's gross profit for the first quarter of 1995 was[

] (Tr. at 1631-1632, 1648; RX 729, QM 108464).

155. Quickturn's gross profit in the first quarter of 1996 was[ ]accounting for cost-of-goods sold, maintenance costs, service costs, other costs, and overhead absorbed [ ](Tr. at 1631-1632, 1648; RX-729, p. QM108457).

156. Quickturn's gross profit on United States sales of product was[ ]during the first quarter of 1996, compared to[ ]for international sales during the same period. (RX-729, p. QM108457).

157. Quickturn's target business model for each of the third and fourth quarters of 1996 call for a gross profit margin of[ ] (RX-729, p. QM108461).

158. Quickturn's gross margin target for United States emulation product sales is [ ] (Tr. at 1558).

159. Quickturn's gross profits for the first quarter of 1996 were $15,963,000, compared to gross profits in the first quarter of 1995 of $12,453,000. (RX-729, p. QM108448).

160. [

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(Folsom, CX-216, Q&A 28; Folsom, RX-51, Q&A 8; Hoffman, RX-702, Q&A 42).

161. [

] (Folsom, Tr. at 1701-1702).

162. Although Quickturn has been in business since 1987, its annual report did not

[

](Ostby, CX-211 at 6; Folsom, CX-216 at 12).

163. As of December 31, 1995, Quickturn had more than[ ]million dollars invested in fixed assets to operate its hardware emulation system business. From 1987 to the present, Quickturn's principal facilities have been located in Northern California in the United States. Quickturn presently has[ ]employees in the United States. At the hearing Otsby estimated[ ]employees in the United States.(Ostby, CX-211, Q&A 19, 20, 22, 23; Tr. at 1602).

164. Quickturn's annual production of hardware logic emulation systems has increased each year. Quickturn's estimated production schedule from 1989 to the present is:

Year	Production Volume
1989	[ ]
1990	[ ]
1991	[ ]
1992	[ ]
1993	[ ]
1994	[ ]
1995	[ ]

(CX-15 ¶ 17; Folsom, CX216, Q&A 24).

165. Quickturn's annual worldwide revenue from sales of hardware logic emulation systems and related services has increased since 1989, as is shown in the following table:

Year	Sales ($ Million)
1989	1.3
1990	6.6
1991	12.8
1992	25.8
1993	54.9
1994	65.5
1995	81.8

(CX-15 ¶ 18; Folsom, CX216, Q&A 25).

166. The international (non-U.S.) market for emulators is growing faster now than is the U.S. market. From 1994 to 1995, the U.S. sales of Quickturn grew by[ ]while at the same time, international sales of Quickturn grew by[ ] The first quarter 1996 U.S. sales of Quickturn increased by[ ]compared to first quarter 1995 U.S. sales [ ]while a comparison of the same periods for Quickturn's international sales shows an increase of[ ] (RX-729, p. QM108453).

167. Quickturn's worldwide sales strategy is to sell its entire package of emulation product, services and solutions to all customers who have a need for emulation. Quickturn's major international customers[

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Q29. [

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Q31. [

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(Cibulsky, CX-213, Q&A, 12-20, 29-35).

168. [

] (Cibulsky, CX-213, Q&A 21).

169. Quickturn's Annual Report notes that "international markets represent an increasingly important part of the electronics industry." (RX-134, p. 4).

170. [ ]

(Tr. at 3467- 3471):

Q. [

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[

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171. In 1995, roughly[ ]of Quickturn's sales were outside the United States. (Ostby, Tr. at 1602).

172. The average sales price of an emulation system sold in the domestic market by Quickturn for all types of System Realizer™ products is approximately[ ] (Moore, CX-212 at 26).

173. When Mentor/Meta wins a new account,[

]

[

] (Moore CX-212 at 27).

174. The whole of economic theory that Folsom has been taught all of Folsom's life is that having additional competitors in the marketplace does not help the firms that are currently selling the product. Instead, it tends to reduce prices and hurt the firms which are currently selling the product. (Folsom Tr at 1815).

175. [

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(Ostby CX-211 at 5).

* * *

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177. Speed, in bringing out new products, is often the name of the game in the computer industry. [

]

[

] (Folsom CX-216 at 41, 42).

178. Hoffman agreed with Quickturn's projections that it will be able to satisfy at least an additional 25% increase in demand during 1996. (Hoffman, Tr. at 2388-2389).

179. [

] (Folsom CX-216, Q&A 115; Tr. at 1387, 1845; Moore CRX-50, Q&A 36).

180. [ ](Zafar JX-7 at 67).

181. [

] (RX-720).

182. [

] (RX-720).

183. [

]

[ ] (RX-720).

184. [

] (RX-152, p. QM580001; Moore Tr. at 1518-21).

185. [

] (Zafar JX-7 at 121).

186. [

] (Moore JX-5 at 196-197).

187. [

] (Moore JX-5 at 198).

188. [

] (Moore Tr. at 1527).

190. [

] (Moore Tr. at 1527).

191. [

] (Zafar JX-7 at 67).

192. [

] (Moore JX-5 at 197, Tr. at 1526).

193. [

]

(Zafar JX-7 at 67).

194. [

] (Folsom CX-216 at 53; CX-76, p. 7).

195. Between 1995 and early 1996, there has been broad acceptance of emulation into the emulation market which had not been there before. (Hoffman, RX-755, Exhibit H12).

196. Quickturn sold approximately[ ]emulation systems in the U.S. market in

1995. (RX-702, Exhibit H15).

197. Only a small percentage of the U.S. semiconductor industry uses emulation due to the high cost of emulators. (Moore CRX-50 at 8).

198. About[ ]of semiconductor design projects are suitable for emulation. (Tr. at 1398).

199. About[ ]out of some[ ]semiconductor design projects in the United States actually use emulation. (Tr. at 1385, 1386, 1397-1398).

200. Quickturn has greatly lowered the price of emulation products over time and has consistently had this as its company goal. From a price of about[ ]per gate in 1990-1991, Quickturn steadily reduced the price to about[ ]per gate in 1994, and it is now just under[ ]per gate. (Ostby Tr. at 1605-1610).

201. As to the term one gate of a[ ]machine, Ostby testified (Tr. at 1606 to 1608):

[

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[

]

202. Quickturn's emulation system is capable of serving any of the United States semiconductor industry projects in 1996 which need and can justify the price of emulation. In addition Quickturn has the capacity to manufacture more systems than could be produced in 1996. (Moore CRX-50 at 23).

203. Hundreds of U.S. companies use Quickturn emulation products. (RX-294, p. QM75448).

204. In real use of an emulation, compile time accounts generally for less than[ ] of the usage time of an emulator. (Cibulsky Tr. at 1343).

205. Public interest deals with more than just the possibility that consumers may purchase a product at a lower price because if that is the measure of public interest, one

would virtually always find that an additional seller is preferred in terms of competition in the market. There is another aspect of the public interest which deals with whether a firm owning patents has the capacity to expand output in response to increases in market demand, and thereby improve its financial position thus engaging in future product development.

[ ]

(Folsom CX-216 at 55).

3. Companies Other Than Mentor/Meta

206. It is Hoffman's understanding that the only companies that are currently delivering or are current suppliers of emulation systems are Quickturn, Meta and VMI (Tr. at 2565, 2568).

207. Moore testified (CX-212 at 8, 9):

Q. [ ] [

]

[

]

208. Synopsys is alleged to be developing a hardware emulation system to sell by the end of 1996. The 1995 total revenue of Mentor, Synopsys, Zycad, IKOS (VMW parent) and Aptix, according to Folsom, is:

	Millions	Year
[		]
Synopsys, Inc.	[ ]	1995
Zycad Corp.	[ ]	1995
IKOS (VMW parent)	[ ]	1995
Aptix	N/A	

(Folsom CX-216 at 45-46).

209. As to Quickturn's philosophy on a company who declares itself to be a competitor Moore testified (Tr. at 3553 to 3556):

[

]

[

]

210. Folsom testified as to companies, other than Mentor/Meta, competing with Quickturn (Tr. 4091 to 4095):

[

]

VMW

211. VMW (Virtual Machine Works) is a new company that introduced an emulation system in January 1996. (Kenney Tr. at 2247).

212. With respect to any competition between Quickturn and VMW, Moore testified (CX-212 at 17 to 18):

Q. [ ]

A. [

]

215. [

] (Moore CRX-50 at 5, 6).

216. [

] (Moore Tr. at 3503).

217. [

](JX-7, Zafar at 127).

218. [

] (JX-5,

Moore at 228-229).

Aptix

219. [

] (Moore CX-212 at 15, CRX-50 at 4).

220. With respect to Aptix Moore testified (Tr. at 3525 to 3529):

Q. [

]

Q. [

]

221. [

] (Moore CX-212 at 14).

222. [

] (Moore CX-212 at 14).

223. [

] (Moore CX-212 at 15).

224. [ ]

(Moore CX-212 at 15).

225. [

]

(Tr. at 3482, 3483):

[ ]

[

]

226. [

](Tr. at 1571-72):

Q. [

]

Zycad

227. [ ](Cibulsky CRX-49 at 3; Tr. at 1380-81, 3524).

228. [ ]

[

] (Moore CX-212 at 17).

229. [ ](Moore Tr. at 1450).

230. [ ](JX-4, Cibulsky at 140-41).

Hewlett-Packard and Synopsys/Arkos

231. [ ](Moore CX-212 at 19).

232. [ ] [ ] (Tr. at 4922).

233. [ ](CX-216, Folsom Q/A 102).

234. [ ](Moore CX-212, Q/A 61-62).

235. [ ](Moore Tr. at 1431).

236. [ ]

[ ](Moore Tr. at 1431-32).

237. [

](Moore Tr. at 1432).

238. [

] (Tr. at 4891).

239. [

](Moore Tr. at 1448-49).

Chip Express

240. As to the company Chip Express, Moore testified (Tr. at 1451 to 1453):

Q. [

]

4. Nature Of Mentor/Meta

241. Quickturn's Cibulsky, its Vice President of International Operations, on Mentor and Meta and on international sales and on bundling testified (Tr. at 1331, 1332, 1392 1393):

Q. [

]

245. In a relatively short period of time, approximately within the last twelve months, Mentor/Meta has shown its ability to effectively compete and take sales away from Quickturn, both in the United States and internationally. Mentor/Meta has also indicated to its sales force that it will aggressively compete with Quickturn for the sale of emulation products in the United States. (Moore CX-212 at 20). [

]

246. Mentor designs, manufactures, markets and services electronic design automation software for the integrated circuit (IC) and systems design markets. Its systems enable engineers and designers to analyze, design and test custom ICs, application-specific integrated circuits (ASICs), printed circuit boards, multichip modules, and other electronic systems and subsystems (CX-15, attachment C).

247. [

]

248. There are only two companies of which Cibulsky is aware that are selling emulation systems outside of the United States, namely Meta and Zycad. Of those two companies, Cibulsky testified that only Meta is a meaningful competitor for Quickturn, and that Zycad has only a minor international presence (CX-213 at b; Tr. at 1325).

249. Cibulsky also is aware of[ ]talking to a customer. (CX-213 at 6; Tr. 1325).

250. In a relatively short period of time, Quickturn has encountered Meta , or Mentor/Meta together, in many of Quickturn's major emulation accounts around the world, [ ] Mentor and Meta have been very active in their sales effort, both in terms of pursuing potential customers[

] Thus Mentor/Meta has presented their product in a number of Quickturn major accounts, namely,[

] (Cibulsky CX-213 at 7, 8).

251. Quickturn received information that[ ]

[ ] (Cibulsky Tr. at 1295, 1296).

252. In the international market, Quickturn's initial price quote to SGS Thomson was [

]

253. Kenney testified (Tr. at 2216, 2217):

Q. Assume there is a design project for a given chip. Also assume that a Meta device is sold to the project team designing that chip, and we have already agreed that that will occur earlier in the design cycle than would the sale of an emulator because they haven't really reached the emulation stage yet; isn't that right?

A. Yes.

Q. In such circumstances, it's also true, isn't it, that the customer would be foreclosed to another vendor, for example Quickturn, who wanted to sell it an emulator for that project because it already had an emulator for that project; isn't that right?

A. If when the emulator was purchased for simulation purposes, the customer had the foresight to purchase all of the emulation capability they required for the later emulation process, they would not have need for additional emulation hardware.

Q. And you would expect your sales people to help the customer understand the desirability of having that additional subject matter; isn't that right?

A. Yes.

254. [

]

[

] (Moore CX-216 at 11, 21).

255. [

] (Folsom CX-216 at 34; CX-74).

256. [

]

257. Meta has bid against Quickturn[ ]with Meta or Mentor and Meta together winning[ ]of those bids. (Cibulsky, CRX49, Q&A 18). This does not include the recent situation at UB Networks where Mentor, in competition with Quickturn, has won the deal with a Meta System. (Folsom CX-216 at 27; Moore CX-212 at 11, 24).

258. Within the past two months, Mentor has defeated Quickturn at the UB

[

] (Moore CRX-50 at 17).

266. [

] (Moore Tr. at 1848; Moore CX-212, Q&A 70).

267. [

] (Folsom, CX-216, Q&A 83).

268. Both Mentor and Quickturn market their products through direct sales forces in the United States. [

] (Folsom CX-216, Q&A 51, 52, CX-191, pp. 15, 17).

269. One of the product managers[ ]mentioned[ ]that Mentor is going to allow Phillips to buy the Mentor emulation system off of their software agreement with Phillips corporate. [

]

[

] (Cibulsky Tr. at 1392, 1393).

270. [

]

271. [ ]

(Folsom, CX-216, Q&A 53, 54; CX-191).

272. Mentor has hundreds of people in its U.S. sales force, which is much larger than Quickturn's sales force. As a result, [

] Mentor account managers have smaller territories and therefore fewer accounts to cover per salesperson. [

] In the hundreds of accounts where Mentor has installations of design automation software,[

] (Moore, CX-212, Q&A 34, 35, and 38).

273. Meta had only ten or twelve sales people prior to its venture with Mentor. (Cibulsky, Tr. at 1366).

274. [ ]

[

] (Moore, CX-212 at 10, 12).

275. Mentor has engaged in promotional activities in the United States, aimed at selling Meta emulation systems to its U.S. customers. (CX-55, CX-56, p. 5, ¶12).

276. [

] (Moore CX-212 at 23).

277. [

] (Folsom CX-216 at 42).

278. Mentor is discussing emulation systems with Cabletron,[ ] (JX-3, Hotaling at 113-115).

279. Moore testified on Motorola and price reduction:

[

][ ].

280. Another reason why Mentor/Meta is competitive with Quickturn is Meta's installed base of emulation products with existing customers in France and the United States, [

] (Moore CX-212 at 10).

281. Mentor has a broad design automation product line which includes design simulation and design verification products which a customer is likely to need. (Moore, CX-212, Q&A 34, 35, 40). [

]

[

]

282. [

]

283. [

]

284. Mentor is "a world leader in hardware and also in software design solutions." (Rhines JX-17, p. 34).

285. [

]

286. [

]

287. [ ]

[

] (Folsom CX-216 at 28).

288. [

]

(CRX-3).

289. In the short run, the price of the software can be cut far more than the price of the hardware can be cut. This is because margins on software are much higher than margins on hardware -- in many cases margins on software are on the order of 90%,[

] (Folsom CX-216 at 29).

290. [

]

291. [

]

[ ]

292. [

]

293. [

]

294. In the United States in 1995, the[ ]largest customers of Quickturn (those over $1 million in purchases) accounted for[ ]of Quickturn's domestic sales. The[ ] largest customers accounted for[ ]of Quickturn's domestic sales. Since marginal profits on Quickturn sales are about[ ]if Quickturn does not cut prices, losing three of those largest customers could[ ] (Folsom CX-216 at 25-26).

295. [

] (Lobo JX-10 at 176).

296. [

]

[

] (Folsom CX-216 at 32; Moore CRX-50 at 15, 16; Cibulsky CRX-49 at 13).

297. [

]

298. [

] (Moore CX-212 at 22).

299. [

]

300. [

]

301. [ ]

309. [

]

310. Because of the relatively high cost of emulation products,[

] (Cibulsky CX-213 at 14).

311. In the two year period 1994 and 1995,[

] (Cibulsky, CX-213 at 9; Tr. at 1248-1249).

312. In the first calendar quarter of 1996,[

] (CX-213 at p. 9; Tr. at 1249).

313. In the first calendar quarter of 1996, [

] (Cibulsky Tr. at 1250, 1310-1319, 1391-1392).

314. [

] (Cibulsky Tr. at 1393).

315. [

]

(Folsom CRX-51 at 12; Cibulsky CRX-49 at 11, 12).

316. RX-141 is a Mentor document titled "SI Valley Area Sales Forecast (Q1 '96).

317. As to encounters in Silicon Valley between Quickturn and Mentor/Meta, Moore testified (Tr. at 1593 to 1596):

Q. [ ], [

]

Q. [

]

318. On head-to-head competitions between Quickturn and Mentor/Meta, Moore testified (Tr. at 1588-1590):

[ ]

319. [

]

320. [

]

321. Quickturn is running into Mentor in competition [

]

(Folsom, CX-216, Q&A 66).

322. [

] (Cibulsky, CX-213 at

13).

323. [

] (Cibulsky, CX-213 at 7, 8).

324. [

]

Each of those customers stated that Quickturn's emulation solution was sufficient to meet the customers' needs. (Cibulsky CX-213 at 9). [

]

(Cibulsky CX-213 at 10). [

]

(Cibulsky CX-213 at 11).

325. [

] (Cibulsky CX-213 at 12).

326. [

]

[

] (Cibulsky CX-213 at 11).

327. [

] (Cibulsky CX-213 at 12).

328. [

]

[

]

[

](Cibulsky CRX-49 at 11-12).

329. [

] (Cibulsky CRX-49 at 11-12).

330. [

]

331. [ ] Thus Moore testified (Tr. at 1357 to 1361):

[

]

[

]

332. [

] (Folsom CX-216 at 43).

333. [

] (Moore CX-212 at 26).

334. [

]

[ ] (Moore CX-212 at 24).

335. [

] (Moore Tr. at 1560, 1561).

336. [

]

[

]

337. On cross-examination Folsom testified (Tr. at 3799 to 3801):

Q. [

]

338. [

] [

] (RX-189). With respect to criteria that a prospective buyer takes into consideration in the purchase of an emulator, Moore testified (Tr. at 1504 to 1506):

[

]

[

]

339. On head-to-head competition in the international scene Cibulsky testified (Tr. at 1302 to 1305):

Q. [

]

Q. [

]

340. [

] (Cibulsky CRX-49 at 11; Folsom CX-216 at 31; CX-208; CX-209).

341. [

]

[

] (Moore CX-212 at 19-21; Folsom CX-216 at 26; CX-208; CX-209).

342. With respect to a price impact on Quickturn as a result of Mentor's activity, Folsom testified (CX-216):

A.70: [

]

[

]

343. [

] (Moore Tr. at 1470).

344. [

] (Folsom CX-216 at 38, 39).

345. With respect to the quantitative nature[ ]Folsom testified (Tr. at 1818, 1819):

Q. [

]

[

]

346. [

] (Folsom Tr. at 4107-4108).

347. Quickturn sold systems to Siemens A.G. in 1996. It did encounter Mentor/Meta as a competitor with respect to the sale to Siemens. [

] (Cibulsky Tr. at 1312, 1313).

348. In the first quarter of 1996,[ ]

[

] (Moore CX-212 at 27; Folsom CX-216 at 40, 41).

349. [

] (Moore CX-212 at 27).

350. [

] (Moore CX-212 at 27; Folsom CX-216 at 40).

351. [ ]

[

] (Folsom, Tr. at 1849-1850).

352. [

] (Moore CX-212 at 90).

353. [

] (Moore CX-212 at 28, 29).

354. [

] (Cibulsky CX-213 at 12).

355. [

] (Cibulsky CX-213 at 12, 13).

356. One former Quickturn Field Application Engineer, Cyril Ecochard, has already left to work for Meta Systems. (Cibulsky CX-213 at 13).

357. Mentor is recruiting Quickturn Field Application Engineers, and has called some of them through a Chicago based recruiter who has offered them positions with Mentor. (Moore CX-212 at 21).

358. [

] (Moore CX-212 at 20).

359. [

] (Folsom CX-216 at 39).

360. [

] (Moore CX-212 at 31).

361. [

] (Ostby Tr. at 1639; Ostby CX-211 at 5; Moore CX-212 at 31).

362. [

] (Folsom, CX-216 at 21).

363. [

]

(Folsom CX-216 at 21; RX 134 at 4).

364. [

] (Folsom Tr. at 1859, 1860).

365. [

]

366. [

]

367. [

]

[

]

368. The Meta device helps industries, including semiconductors, multimedia and telecommunictions, design and debug chips in less time, allowing faster time to market. Also many customers interested in purchasing a Meta device are interested because of functionalities that Quickturn simply does not have. (Rhines RX-701 at 11-12).

369. [

]

370. The Meta device has the performance available from emulators. (Kenney RX-700 at 9).

371. Mentor/Meta has superior technology in the emulation market. If it cannot sell emulators because of the issuance of a TEO, such delay will allow Quickturn to develop a next generation of product using custom integrated circuit technology like Meta's. (Kenney RX-700 at 22, 23).

372. The sooner a company, with what is alleged as superior technology, gets into the emulation market, the larger its market share and its ability to compete in that market. (Peltzer RX-703 at 5-6).

373. Traditional emulators use chips, generally known as FPGAs, to test the circuit design. The FPGA is an alternative to computer software in that they were designed to

simulate the logic functionalities of a circuit. Because an FPGA is not lines of code of a software program to be read by a computer, but an actual semiconductor chip, it performs at much faster speeds than a computer software simulator. The traditional emulator's functionality (i.e., what tasks it can perform), however, is much narrower and traditionally it has been used for the purpose of in-circuit verification. Thus, emulators have been used to test what the engineer believes is his or her final design. One of the reasons emulators traditionally have been used solely for in-circuit verification is that there is an extremely long period of time taken to compile the circuit information into the FPGAs, sometimes in the order of days. In addition, traditional emulators have not had debugging capabilities. [

]

374. As to any faster compile time of the Meta emulator, Folsom testified (Tr. at 1866 to 1868):

[

]

J. Claim Construction

377. Mr. Steven Sapiro is an independent consultant involved in hardware design, software design, software project management, strategic marketing for software projects and business development for small companies. He received a BSEE from the City College of New York in 1969, specializing in semiconductor theory and integrated circuit design. He spent about seven years as an MOS integrated circuit designer and embedded systems designer working on automotive, appliance and military circuits. He is member of the Circuit Systems Organization of the IEEE. He has chaired several conferences, developed two different technical seminars, and published over 20 articles on circuit design, design automation and electronic design automation. He has also written two books, one on design automation which talked about the different facets of the electronic design process, and another on the topic of fault simulation as part of the electronic design process (Sapiro, CX-215, Q&A 3-10). Mr. Sapiro's chip design experience includes using logic simulation and bread boarding chips to verify correct functionality. (Sapiro, CX-215, Q&A 11-14). Sapiro has been qualified as complainant's expert in the electronic design automation field (Sapiro, Tr. at 873).

378. Dr. Edward J. McCluskey is a senior professor in the electrical engineering and computer science departments at Stanford University in California, where he teaches

courses in logic design, testing and computing. He received his BS, MS and doctorate degrees in electrical engineering from MIT, and an honorary degree from the Institute Nationale Polytechnique Grenoble. He has had extensive experience over the years in the field of computers, logic design and networks. He worked for Bell Telephone Laboratories during the 1950s, and has consulted for IBM, Data General, LSI Logic and others. He is active in numerous professional organizations, including the IEEE and has also received numerous awards in recognition for his contributions to the field of engineering and computing (McCluskey, CX-214, Q&A 2-10). McCluskey has had extensive experience with interconnection networks, starting with his work at Bell Telephone Laboratories and continuing with his work in the field of fault-tolerant computing. His consulting work has involved gate array design, including the design of circuitry to be realized on Xilinx field programmable gate arrays, and the engineering of a synthesis system to design gate arrays and he taught courses in switching logic design, and has written text books in the field of logic design which have been very widely accepted and used as texts in many other schools. He also co-authored a book on digital computer design (McCluskey CX-214, Q&A 11-13). McCluskey was qualified as complainant's expert in network design, logic design and computer engineering (McCluskey, Tr. at 886, 1024-1025).

379. Dr. Andrew Wolfe, who testified as an expert witness for respondents, received a B.S. in Electrical Engineering and Computer Science from the Johns Hopkins University in 1985. Thereafter, he received a Masters Degree in Electrical and Computer Engineering and a Ph.D. in Computer Engineering from Carnegie Mellon University in 1992. (Wolfe, RX-705 at Q 1). Wolfe was employed as an electrical engineer for Touch Technology, Inc. from 1983-85, where he designed or managed the design of all of that company's electronics and developed some software. He later worked as a project consultant

with Carol Touch Division of AMP, Inc. in Roundrock, Texas. During that employment, which lasted from 1986 through 1987, he designed electronics and firmware for Touchscreen Systems, which included the design of a mixed-signal application specific integrated circuit (ASIC). In the summer of 1989, Dr. Wolfe was employed as a senior electrical engineer at ESL-TRW Advanced Technology Division in Sunnyvale, California, where he designed ILP and multi-processor architectures for high performance signal processing. He also designed a field programmable gate array (FPGA) based interface for a multiprocessor system. Thereafter, Wolfe was a Vice President and founder of The Graphics Technology Company and held that position until the subsidiary, Touch Technology, Inc., was sold in 1995. Presently, Wolfe is an assistant professor at Princeton University, both teaching and doing research in computer architecture, certain digital systems, and optimizing software compilers. (Wolfe, RX-705 at Q 2). Dr. Wolfe has substantial experience in designing reconfigurable computing systems using FPGAs to provide that reconfigurability. Wolfe has also used FPGAs for computer system development at ESL and in teaching at Princeton. (Wolfe, RX-705 at Q 3). Wolfe was qualified as respondent's expert in logic circuits, logic circuits containing FPGAs, and reconfigurable computer and simulation systems. (Tr. at 3369-3370)

380. Brian Von Herzen has a bachelor's degree in physics *magna cum laude* from Princeton University, a master of science degree in computer science from California Institute of Technology in 1984 and a PhD in computer science from California Institute of Technology granted in 1988. (Von Herzen, RX-704 at Q 2). Since then he has had experience in design and development of semiconductor chips. (Von Herzen, RX-704 at Q 4 & 5). Von Herzen was qualified as respondents' expert in the field of semiconductor chip design processes. (Von Herzen, Tr. at 2619-2623).

381. Mr. Peltzer received a BA in math and physics from Knox College in Illinois

in 1960. He received an MS in physics from New Mexico State University in 1964 and an MBA from the University of Phoenix in 1990. (Peltzer, RX-703 at Q 2). Peltzer was qualified as respondents' expert in the U.S. semiconductor industry, the trends of the U.S. semiconductor industry, and also the use of tools in the semiconductor industry by the chip designer, and the effect for such use of those tools in the semiconductor industry. (Peltzer, Tr. at 2659).

1. The '473 Patent

382. The '473 patent, entitled "Method of using Electronically Reconfigurable Logic Circuits," issued on July 30, 1991. It is based on Application Serial No. 417,196, filed October 4, 1989. This application was a continuation-in-part of Application Serial No. 254,463 filed on October 5, 1988, now abandoned. The named inventors are Michael R. Butts of Portland, Oregon and Jon A. Batcheller of Newburg, Oregon (CX-5).

383. The application leading to the issuance of the '473 patent (CX-5) was prosecuted not by complainant's attorneys but by Mentor's patent attorneys, the firm of Klarquist, Sparkman, Campbell, Leigh & Whinston (CX-60). Rights to the issued '473 patent were transferred from Mentor to Quickturn by an Asset Purchase Agreement dated March 2, 1992 (CX-9). An instrument of assignment was executed in favor of Quickturn by Mentor on February 28, 1992, and filed in the United States Patent and Trademark Office on March 18, 1992 (CX-41 referred to in April 29, 1992 disclaimer of claims), concerning the '473 patent the only thing Mentor's patent attorneys did subsequent to the assignment was the filing of a letters of correction (Tr. at 4814).

384. References considered by the Patent Office during the prosecution of the '473 patent included, inter alia, the Xilinx 1986 Databook (RX-4), the Wynn article "Designing with Logic Cell Arrays" (RX-54). The Xilinx XACTOR is described in the Xilinx 1986

Databook (RX-4 at 4-27 and 28).

385. By letter dated April 29, 1992, Quickturn disclaimed claims 1, 6, 13, 14, 16, and 17 of the '473 patent (RX-48).

386. Claim 8 of the '473 patent in issue is a dependent claim which progressively incorporates limitations from independent claim 1, dependent claim 6, and dependent claim 7. Claim 8 claims:

> 8. The method of claim 7 which further includes:
>
> connecting each of said reconfigurable interconnect ERCLC(s) to at least one but not all of the pins of each of said N ERCLCs.
>
> (CX-5).

387. Independent claim 1 of the Butts '473 patent reads as follows:

> 1. A method comprising the steps:
>
> providing first and second electrically reconfigurable logic circuits (ERCLCs);
>
> providing first input data representative of a first digital logic network, said input data including primitives comprised of boolean logic gates, and nets interconnecting said primitives;
>
> automatically partitioning said first input data into first and second portions;
>
> providing the first portion of the partitioned first data to the first ERCLC so a first portion of the first digital logic network represented thereby takes actual operating form on the first ERCLC;
>
> providing the second portion of the partitioned first data to the second ERCLC so a second portion of the first digital logic network represented thereby takes actual operating form on the second ERCLC;
>
> interconnecting the first and second ERCLCs so that at least one net specified in the first input data extends between the first and second ERCLCs;
>
> providing second input data representative of a second digital logic network entirely unrelated to the first digital logic network except that

both include primitives comprised of boolean logic gates, and nets interconnecting said primitives, and both are to take actual operating form on the same ERCLCs;

automatically partitioning said second input data into first and second portions;

providing the first portion of the partitioned second data to the first ERCLC so a first portion of the second digital logic network represented thereby takes actual operating form on the first ERCLC;

providing the second portion of the partitioned second data to the second ERCLC so a second portion of the second digital logic network represented thereby takes actual operating form on the second ERCLC;

interconnecting the first and second ERCLCs so that at least one net specified in the second input data extends between the first and second ERCLCs.

(CX-5).

388. Dependent claim 6 of the '473 patent reads as follows:

6. The method of claim 1 which further includes:

(a) providing N ERCLCs;
(b) partitioning the first input data into N portions;
(c) providing each portion of the partitioned data to the ERCLC to which it corresponds, so the portion of the digital logic network represented thereby takes actual operating form on said ERCLC;
(d) interconnecting the N ERCLCs so that each of the ERCLCs is connected to at least one other of the ERCLCs and so that each of the nets specified in the input data is implemented; and
(e) repeating steps (b) through (d) for the second input data.

(CX-5).

389. Dependent claim 7 of the '473 patent reads as follows:

7. The method of claim 6 in which the ERCLCs each include a plurality of pins, and in which the interconnecting steps include:

providing at least one reconfigurable interconnect; and

connecting each of said reconfigurable interconnects to at least one but not all of the pins of a plurality of said N ERCLCs.

(CX-5).

390. Claim 8 of the '473 patent, rewritten in independent form to include all of the limitations of the antecedent claims in the chain of dependency, reads as follows:

A method comprising the steps of:

(a) providing N electrically reconfigurable logic circuits (ERCLCs), the ERCLCs each includ[ing] a plurality of pins;

providing first input data representative of a first digital logic network, said input data including primitives comprised of boolean logic gates, and nets interconnecting said primitives;

(b) automatically partitioning said first input data into N portions;

(c) providing each portion of the partitioned data to the ERCLC to which it corresponds, so the portion of the digital logic network represented thereby takes actual operating form on said ERCLC;

(d) interconnecting the N ERCLCs so that each of the ERCLCs is connected to at least one other of the ERCLCs and so that each of the nets specified in the input data is implemented

the interconnecting steps include providing at least one reconfigurable interconnect and connecting each of said reconfigurable interconnect ERCLC(s) to at least one but not all of the pins of each of said N ERCLCs; and

providing second input data representative of a second digital logic network entirely unrelated to the first digital logic network except that both include primitives comprised of boolean logic gates, and nets interconnecting said primitives, and both are to take actual operating form on the same ERCLCs;

(e) repeating steps (b) through (d) for the second input data.

(CDX-6).

391. Claim 13 of the '473 patent reads:

The method of claim 1 which further includes:

(a) providing N ERCLCs;

(b) topologically arranging said N ERCLCs in a regular multi-dimensional

array, thereby establishing relatively neighborings ERCLCs;

(c) directly interconnecting neighboring ERCLCs;

(d) partitioning the first input data into N portions;

(e) providing each portion of the partitioned data to the ERCLC to which it corresponds, so the portion of the digital logic network represented thereby takes actual operating form on said ERCLC;

(f) interconnecting the N ERCLCs as required to implement the nets specified in the first data, said interconnecting including interconnecting non-neighboring ERCLCs by establishing interconnections through ERCLCs that intervene between said non-neighboring ERCLCs; and

(g) repeating steps (d) through (f) for the second input data.

The Claim Term "ERCLC"

392. The first method step defined in Claim 8 of the '473 patent requires "providing N electrically reconfigurable logic circuits (ERCLCs), the ERCLCs each includ[ing] a plurality of pins." The term "ERCLCs" is not defined or used in the specification of the '473 patent. The term "ERCLC" first appeared in an amendment, dated December 20, 1990, filed during the prosecution of U.S. Patent Application Serial No. 417,196 (CX-60 at QM47092), which ultimately matured into the '473 patent (CX-5). The term "ERCLC(s)" replaced the term "ERCGA(s)" or "electronically reconfigurable gate array," which had been present in the claim language up to that point (CX-60 at QM47084-47091). The term "additional ERCGA to serve as a" was deleted from claim 5 and claim 7.

393. "ERCGA" is a term employed in the specification of the Butts '473 patent, and is defined as:

> an electronically reconfigurable gate array, that is a collection of combinational logic, and input/output connections (and optionally storage) whose functions and interconnections can be configured and reconfigured many times over, purely by applying electronic signals

(CX-5, col. 2, lns. 3-8).

394. According to the December 20, 1990 Amendment:

> The term electronically reconfigurable gate array 'ERCGA' has been revised to read 'electronically reconfigurable logic circuit (ERCLC)' to make clear that the invention may be practiced with reconfigurable logic circuits that are not technically "gate arrays."

(CX-60 at QM47092). Applicants further argued:

> Dependent claim 6 has been amended to specify that the reconfigurable interconnects need not be ERCLCs.

395. The capabilities of a reconfigurable "logic chip device" are generally described as in the '473 patent as follows:

> For a device to be useful as a Realizer logic chip, it should be an electronically reconfigurable gate array (ERCGA):
>
> 1) It should have the ability to be configured according to any digital logic network consisting of combinational logic (and optionally storage), subject to the capacity limitations.
>
> 2) It should be electronically reconfigurable, in that its function and internal interconnect may be configured electronically any number of times to seek many different logic networks.
>
> 3) It should have the ability to freely connect I/O pins with the digital network, regardless of the particular network or which I/O pins are specified, to allow the Realizer System partial crossbar or direct interconnect to successfully interconnect logic chips.

(CX-5, col. 7, lns. 32-47).

396. The specification of the '473 patent makes reference to three examples of reconfigurable logic chips. Those examples include the "Logic Cell Array (LCA)" manufactured by Xilinx, and others; the "electrically reconfigurable array" or ERA, manufactured by Plessey; and the electrically erasable programmable logic device (EEPLD), and example of which is the Lattice Generic Array Logic (GAL). (CX-5, col. 7, ln 48 to col.

8, ln. 48). The specification, in describing the EEPLD, indicated that:

> It offers freedom of connection of I/O pins to logic only among all input pins and among all output pins, so it partially satisfies that requirement.

(CX-5, col. 8, lns. 44-46).

397. "N" recited in method claim 8 of the '473 patent is an integer value which typically refers to a positive integer value (Butts, Tr. at 263; Wolfe, RX-705 at Q 8).

398. With respect to the meaning of the term "N" recited in claim 8, respondents' Wolfe could not differentiate between claim 6 and claim 1 or claim 7 and claim 8 if "N" were read as equal to two in claims 6, 7 and 8 of the '473 patent. Thus Wolfe testified:

Q. Claim 6 calls for N ERCLCs; is that correct?

A. That's correct.

Q. I believe in your testimony you said you thought N could be more than one?

A. Yes.

Q. Would that mean that N could be two?

A. I believe that's correct.

Q. If N is equal to two in claim 6, can you tell me, is there any difference between claim 6 and claim 1? And please feel free to take your time, Dr. Wolfe.

A. Given that claim 6 has to incorporate all of the language of claim 1 for the specific case where N equals two, I don't see any differences right now.

Q. So if we want to differentiate claim 6 from claim 1 in some fashion, N has to be more than two, doesn't it?

A. In my reading, claim 1 covers devices with two ERCLCs and claim 6 covers devices with two or more ERCLCs.

Q. Right. But if we're going to differentiate between claim 1 and claim 6, N should be at least three because claim 1 already covers two devices; is that correct?

A. As I said, I don't understand the patent law involved, but I certainly can differentiate between two and two or more.

JUDGE LUCKERN: He's not asking you as a patent man, but just looking at this claim from a technical standpoint, would you agree that N has to be more than two if you want to say there's a difference between claim 1 and claim 6, that is N in claim 6 has to be more than two. Otherwise you as a technical person are saying that claim 1 and claim 6 are the same. That's what I'm asking you.

* * *

THE WITNESS: If N is two in claim 6, it appears to cover the same thing as claim 1. If N is more than two in claim 6, it appears to cover something different than claim 1.

* * *

Q. But if N is a number three or more, then you can differentiate between claim 1 and claim 6, correct?

A. That's correct.

Q. And you can also differentiate between claim 7 and claim 8, correct?

A. Correct.

Q. And the way in which you would differentiate between claim 7 and claim 8 if N is a number three or greater, is to say that in claim 7 the reconfigurable interconnect would be able to connect to two of the logic devices, but it wouldn't have to connect to the third, correct?

A. That's correct.

Q. And in claim 8 the reconfigurable interconnect would connect to all three of the logic devices, correct?

A. Yes.

(Wolfe, Tr. at 2853-2854).

The Claim Term "First Input Data"

399. With respect to the language of claim 1 that required "providing first input data representative of a first digital logic network," McCluskey did not understand that

limitation to require any one-to-one correspondence with a user's design. Thus, he testified:

> . . . what do you understand the language that appears at line 7 of column 89 through line 9 [of the '473 patent] which says
>
> * * *
>
> Q. It says, Interconnecting the first and second ERCLCs so that at least one net specified in the first input data extends between the first and second ERCLCs.
>
> Now, I want to know whether the Butts invention as set forth in claim 1, as you understand it, as a technical person, not a patent attorney, requires the user's design represented in input data to have at least one net specified in that input data extending between two logic devices.
>
> A. I don't believe that the claim intends to have any such restriction, that the net referred to in the claim must correspond exactly to a net in the user's input specification. I think it's clear from -- I think it's clear that the user's input specification need not have such a net.
>
> * * *
>
> Q. Okay. Look to column 88, Dr. McCluskey, at lines 61 through 64, and I'll read that into the record: "Providing first input data representative of a first digital logic network, said input data including primitives comprised of Boolean logic gates and nets interconnecting said primitives."
>
> Do you see that?
>
> A. I do.
>
> Q. Earlier you told us using current design methodology with higher level languages, those things are not specified?
>
> A. The input specification of the design may not be in the language in terms of individual gates, but this, if I could just finish, these four sentences that you just read and that we're looking at, <u>says the input data representative of a design</u>, not -- I mean, <u>it just represents the design</u>. I don't think that that requires that it enumerate the design in this language or in terms of these primitives, and the discussion in the patent specifically points out that the input data doesn't have to be in terms of elementary gates, and it discusses the transformation into elementary gates.
>
> Q. Okay. What I'm referring to is the language of claim 1 of the Butts '473 patent, which of course is CX-5, and specifically the definition of

of the input design as a result of design conversion, others do not.

(CX-5, col. 10, lns. 7-11) (emphasis added). The '473 patent specification, at Cols. 48-50, further teaches, with respect to the preferred embodiment, that:

> 2.2. Primitive Converter
>
> The purpose of primitive conversion is to convert the primitives in the design data structure from host-specific primitives, such as the Mentor Graphics QuickSim primitives, into logic chip-specific primitives which can be issued in the netlist files, compatibly with the ERCGA netlist conversion tool. Some of this conversion is simple and direct, involving only a replacement of primitive type and pin names. Other conversion is more complex. Specific references made below are to the preferred embodiment, which uses Mentor Graphics QuickSim host-specific primitives as found in the Mentor Graphics input design file, and Xilinx LCA logic-chip-specific primitives.
>
> When a gate in the design has more inputs than is allowed in the logic chip-specific gate primitive, it is replaced by a network of gates, with equivalent functionality, each of which has an acceptable number of inputs. To do such a replacement, the primitive and pin records for the gate are removed and primitive and pin records for the new gates, and net records for the new nets inside the network, are added and linked to the pin and net records for the pins and nets which connected to the replaced gate (FIG. 45a).
>
> When a flip-flop in the design has functions not available in the logic chip-specific flip-flop primitive, it is replaced by a network of gates with equivalent functionality.

(CX-5, col. 48, lns. 3-30, col. 49, lns. 27-30). The specification of the '473 patent also teaches:

> The nets between the logic or crossbar chip's I/O buffer and the I/O pin, the nets between the AND gates and the summing gate(s) of a tri-state sum of products, and the nets passing up and down the interconnect when crossbar summing is used, all are related to a single net in the design, but are distinct nets in the netlist files. Variations of the actual net name are used when issuing the interconnect primitives to the netlist files so as to provide distinct net names for each of these interconnect functions.

(CX-5, col. 59, lns. 56-65) (emphasis added). Thus, while some of the conversions taught for the preferred embodiment may be direct, other conversions involve replacing the user design primitives with functional equivalents Id.

401. The specification of the '473 patent (CX-5, col. 45, lns. 38-66) describes a preferred "Realizer Design Conversion System" procedure as follows:

> It takes the input design file as input, and creates a configuration file and correspondence table file as output, which are used by the various applications to configure and use the Realizer hardware. To convert an input design:
>
> 1) Read the design into the memory data structure with the design reader.
>
> 2) Convert the primitives in the design data structure from host EDA system-specific primitives, into logic chip primitives which can be issued in the netlist files compatibly with the ERCGA netlist conversion tool.
>
> 3) Use the partitioner to determine which logic chip each primitive will be configured into.
>
> 4) Use the netlisting and interconnection system to generate netlist files for each logic and interconnect chip in the Realizer hardware system.
>
> 5) Use the ERCGA netlist conversion tool repeatedly, converting each netlist file into a corresponding configuration file.
>
> 6) Use the configuration file collector, which is a simple method which collects the configuration data from each logic and interconnect chip's configuration file into a single configuration file for this design, which is used to configure the Realizer hardware.
>
> The method for design conversion described here applies to converting the combinational logic gates and flip-flops in the input design, except as noted. Variations of these method are used to convert the special-purpose element primitives.

402. The automatic partitioning step of claim 8 in the '473 patent involves the computer-aided assignment of primitives of the input data to the various ERCLCs. The preferred embodiment of the '473 patent follows a process known as "clustering," involving a number of specific details (CX-5, col. 53, lns. 54-56).

403. The specification of the '473 patent (CX-5, col. 53, lns. 41-63) describes Partitioning as:

> The Realizer hardware is composed of a hierarchy of units and sub-units: boards containing logic chips, boxes containing boards, racks containing

boxes, and so forth. Each unit has its own capacity for logic and for interconnections to other units. Designs to be realized are partitioned (i.e. subdivided) into multiple clusters of primitives according to this hierarchy. There is a set of partitions for boxes, sized according to the logic and connection capacity of each box. Each of those partitions is divided into subpartitions for the boards, and so on, down to partitions small enough to be programmed into a single logic chip. The same partitioning methodology is applied at each level of the hierarchy in turn.

The goals of partitioning are:

1) to assign each primitive to a box, a board and a logic chip.

2) To keep the number of nets connecting to a partition below the interconnect ability of the unit (box, board or logic chip),

3) To keep the amount of logic used by the partition within the limits of the unit, and

4) To minimize the total number of partitions and therefore the number of units used.

The Claim Terms "Interconnecting" and "Interconnect ERCLC"

404. The specification of the '473 patent teaches "nearest neighbor" and "crossbar" interconnects. Among the "nearest neighbor" class are "direct interconnect" and "channel routing." Among the "crossbar" interconnects are the "partial crossbar." (CX-5).

405. The specification of the '473 patent teaches both direct and indirect connections between logic chips. Thus, the specification reads:

> In the direct interconnect, all logic chips are directly connected to each other in a regular array, without the use of interconnect chips. The interconnect consists only of electrical connections among logic chips.

(CX-5, col. 11, lns. 32-35) (emphasis added). Figure 2 of the '473 patent is a "schematic block diagram of a direct interconnect system." (CX-5, col. 4, lns. 52-53). The specification also teaches that:

> The channel-routing interconnect is a variation of the direct interconnect, where the chips are divided into some which are not used for logic, dedicated only to accomplishing interconnections, thus becoming interconnect chips, and

> the others are used exclusively for logic, remaining logic chips. In particular, logic chips are not directly interconnected to each other, but instead connected only to interconnect chips.

(CX-5, col. 13, lns. 6-13) (emphasis added). A "schematic block diagram of a channel-routing-interconnect system" is shown in Figure 3 of the 473 patent. With respect to the "partial crossbar interconnect," the specification teaches:

> The pins of each crossbar chip are connected to the same subset of pins from each of every logic chip. Thus, crossbar chip 'n' is connected to subset 'n' of each logic chip's pins. . . . Each logic chip/crossbar chip pair is interconnected by as many wires, called paths, as there are pins in each subset.

(CX-5, col. 15, ln 65 - col. 16, ln. 6). Figures 6 and 7 of the '473 patent are examples of a partial crossbar interconnect system (CX-5, col. 4, lns. 60-63). The specification teaches with respect to Figs. 6 and 7:

> The general pattern [of the partial crossbar] is shown in FIG. 6. Each line connecting a logic chip and a crossbar chip in this figure represents a subset of the logic chip pins. Each crossbar chip is connected to a subset of the pins of every logic chip. Conversely, this implies that each logic chip is connected to a subset of the pins of each every crossbar chip. The number of crossbar chips need not equal the number of logic chips, as it happens to in these examples. It does not in the preferred implementation.
>
> FIG. 7 shows an example, interconnecting the same four logic chips as in FIGS. 1 and 2. Four crossbar chips with eight pins each are used. Each crossbar chip connects to the same two pins of each logic chip. Crossbar chip 1 is connected to pins A and B of each of logic chips 1 through 4. Crossbar chip 2 is connected to all pins C and D, chip 3 to all pins E and F, and chip 4 to all pins G and H.

The specification also teaches:

> An 'interconnect' is a reconfigurable means for passing logic signals between a large number of chip I/O pins as if the pins were interconnected with wires.

(CX-5, col. 1, lns. 62-64) (emphasis added). The "partial crossbar" is used in the preferred embodiment of the '473 patent. Those Figures 2, 3, 6 and 7 of the '473 patent are as follows:

A. I said that the device shown in figure C was a device which meets the language of the claims of claim 7.

Q. Right. And you also said you couldn't find that device in the Butts patents; is that correct?

A. That's correct. I think there are lots of devices that meet the requirements of the claim language that are not taught anywhere in the patent.

Q. I see. But this is one of them in particular, diagram C of RX-751. You believe that according to your interpretation of claim 7, and I guess for that matter claim 8, that the diagram labeled C is covered, but you can find it nowhere in the Butts patent, correct?

A. Other than the claims language, that's correct.

(Wolfe Tr. at 2858-2860).

407. The specification of the '473 patent teaches:

Interconnect Chip Devices

Interconnect chips include crossbar chips, used in full and partial crossbar interconnects, and routing chips, used in direct and channel-routed interconnects. For a device to be useful as a Realizer interconnect chip:

1) It should have the ability to establish many logical interconnections between arbitrarily chosen groups of I/O pins at once, each interconnection receiving logic signals from its input I/O pin and driving those signals to its output I/O pins(s).

2) It should be electronically reconfigurable, in that its interconnect is defined electronically, and may be redefined to suit many different designs.

3) If a crossbar summing technique is used to interconnect tri-state nets in the partial crossbar interconnect, it should be able to implement summing gates. (If not, other tri-state techniques are used, as discussed in the tri-state section.)

(CX-5, col. 8, ln. 54 - col. 9, ln. 3).

408. The specification of the '473 patent teaches, with respect to "interconnect chip devices":

> The ERCGA devices discussed above, namely the LCA, the ERA and the EEPLD, satisfy these requirements, so they may be used as interconnect chips. Even through little or no logic is used in the interconnect chip, the ability to be configured into nearly any digital network includes the ability to pass data directly from input to output pins. The LCA is used for corssbar chips in the preferred implementation of the Realizer system.
>
> Crossbar switch devices, such as the TI 74AS8840 digital crossbar switch (SN74AS8840 Data Sheet, Texas Instruments, Dallas, Tex., 1987), or the crosspoint switch devices commonly used in telephone switches, may be used as interconnect chips. However, they offer a speed of reconfiguration comparable to the speed of data transfer, as they are intended for applications where the configuration is dynamically changing during operation. This is much faster than the configuration speed of the ERCGA devices. Consequently, such devices have higher prices and lower capacities than the ERCGAs, making them less desirable Realizer interconnection chips.

(CX-5, col 9, lns. 4-24).

409. The specification of the '473 patent teaches the following use of the logic capacity of an interconnect chip:

> 1.2.3.3. Crossbar Summing Configuration
>
> In the crossbar summing configuration, the summing OR gate is placed on the crossbar chip, making use of the fact that the crossbar chips in some embodiments are implemented with ERCGAs, such as LCAs, which have logic available, as shown in FIG. 14.
>
> Each logic chip needs one pin if it is a driver, and/or one pin if it is a receiver. The crossbar chip must have one or more logic elements for the summing gate. Crossbar summing deviates from the practice of putting all logic in the logic chips and none in the crossbar chips, but an important distinction is that the logic placed in the crossbar chip is not part of the realized design's logic. It is only logic which serves to accomplish the interconnection functionality of a tri-state net.

(CX-5, col. 19, lns. 42-56).

410. Patent claim 7 of the '473 patent in the prosecution of the '473 patent was identified as application claim 8, patent claim 8 was identified as application claim 9, and patent claim 5 was identified as application claim 6. (CX-60 at QM47184).

411. The preferred embodiment of the '473 patent is described as follows:

To distinguish among crossbar chips in a Realizer system, the partial crossbar interconnect which interconnects logic chips is called the X-level interconnect, and its crossbar chips are called Xchips. The interconnect which interconnects logic boards is called the Y-level interconnect, and its crossbar chips are called Ychips. In the X-level interconnect, the I/O pins of each logic board are divided into proper subsets, using the same division on each logic board. The pins of each Ychip are connected to the same subset of pins from each of every logic board. As many Ychips are used as there are subsets, and each Ychip has as many pins as the number of pins in the subset times the number of logic boards.

* * *

A specific example is the preferred embodiment:

The partial crossbar interconnect is used hierarchically at three levels across the entire hardware system.

A logic board consists of up to 14 logic chips, with 128 interconnected I/O pins each, and an X-level partial crossbar composed of 32 Xchips. Each Xchip has four paths to each of the 14 Lchips 956 total), and eight paths to each of two Ychips, totaling 512 logic board I/O pins per board.

A box contains one to eight boards, with 512 interconnected I/O pins each, and a Y-level partial crossbar composed of 64 Ychips. Each Ychip has eight paths to an Xchip on each board via logic board I/O pins, and eight paths to one Zchip, totaling 512 box I/O pins per box.

A rack contains one to eight boxes, with 512 interconnected I/O pins each, and a Z-level partial crossbar composed of 64 Zchips. Each Zchip has eight paths to a Ychip in each box via box I/O pins.

(CX-5, col. 23, lines 44-62).

2. The '496 Patent

412. The '496 patent, entitled "Partial Crossbar Interconnect Architecture for Reconfigurably Connecting Multiple Reprogrammable Logic Devices In A Logic Emulation System," issued on September 5, 1995, based on Application Serial No. 270,234. This application was a continuation of abandoned Application Serial No. 175,981, filed on December 30, 1993, which was a continuation of abandoned Application Serial No. 698,734, filed on May 10, 1991, which was a continuation-in-part of Application Serial No. 417,196,

filed on October 4, 1989 and which issued as U.S. Patent No. 5,036,473, which was a continuation-in-part of abandoned Application Serial No. 254,463, filed on October 5, 1988. The named inventors are Michael R. Butts and Jon A. Batcheller (CX-6). The term subsequent to the July 30, 2008 expiration of the '473 patent was disclaimed because of claim 8 of the '473 patent (CX-61, QM48252-48255).

413. Claims 1, 2, 3, and 15 of the '496 patent are at issue in this temporary relief proceeding. Claims 1 and 15 are independent claims, while claims 2 and 3 depend from claim 1. (CX-1, CX-6 Notice of Investigation, 61 *Fed. Reg.* 9486).

414. In the prosecution of the '496 patent, the following patents and publication were cited to the Patent Office via an Amended Information Disclosure Statement of September 14, 1994 (CX-61 at QM48260-48318): Sample et al U.S. Patent No. 5,109,353 (CX-3), the Xilinx 1986 Databook (RX-4), the XACTOR description in the Xilinx 1986 Databook (RX-4 at pages 4-27 and 28), the Wynn article "Designing With Logic Cell Arrays", (RX-54), the Schmitz article "Emulation of VLSI Designs Using LCAs" (RX-13), the Clos article "A Study of Non-Blocking Switching Networks," (RX-16) and the Wynn article (RX-12). Each of these references is listed on the first four pages of the '496 Patent (CX-6), except the Wynn article entitled "In-Circuit Emulation for ASIC-Based Designs"(RX-12), though the Wynn article (RX-12) was expressly cited in the amended Information Disclosure Statement at page 9 (CX-61 at QM48286).

415. Claim 1 of the '496 patent reads:

> An electrically reconfigurable logic assembly for use in an electrically reconfigurable hardware emulation system which can be configured with a circuit design in response to the input of circuit information, said electrically reconfigurable logic assembly comprising:
>
> a plurality of reprogrammable logic devices, each of said reprogrammable logic devices having internal circuitry which can be

reprogrammably configured to provide functional elements selected from the group of at least combinatorial logic elements and storage elements, each of said reprogrammable logic devices also having programmable I/O terminals which can be reprogrammably connected to selected ones of said functional elements configured into said reprogrammable logic devices;

a plurality of reprogrammable interconnect devices, each of said reprogrammable interconnect devices having I/O terminals and internal circuitry which can be reprogrammably configured to provide interconnections between selected ones of said I/O terminals; and

a set of fixed electrical conductors connecting said programmable I/O terminals on said reprogrammable logic devices to said I/O terminals on said reprogrammable interconnect devices such that each of said reprogrammable interconnect devices is connected to at least one but not all of said programmable I/O terminals on each of said reprogrammable logic devices.

(CX-6, '496 patent at col. 87, lns. 35-65).

416. Claim 2 of the '496 patent reads:

An electrically reconfigurable logic assembly as recited in claim 1, wherein said reprogrammable logic devices comprise programmable gate arrays.

(CX-6, '496 patent at 87:66-68)

417. Claim 3 of the '496 patent reads:

An electrically reconfigurable logic assembly as recited in claim 1, wherein said reprogrammable logic devices comprise FPGAs.

(CX-6, '496 patent at 1-3)

418. Claim 15 of the '496 patent reads:

An electrically reconfigurable logic assembly for use in an electrically reconfigurable hardware emulation system which can be configured with a circuit design in response to the input of circuit information, said electrically reconfigurable logic assembly comprising:

a plurality of reprogrammable logic devices, each of said reprogrammable logic devices having internal circuitry which can be reprogrammably configured to provide functional elements selected from the group of at least combinatorial logic elements and storage

elements, each of said reprogrammable logic devices also having programmable I/O terminals which can be reprogrammably connected to selected ones of said functional elements configured into said reprogrammable logic devices;

a plurality of reprogrammable interconnect devices, each of said reprogrammable interconnect devices having I/O terminals and internal circuitry which can be reprogrammably configured to provide interconnections between selected ones of said I/O terminals;

a set of fixed electrical conductors connecting said programmable I/O terminals on said reprogrammable logic devices to said I/O terminals on said reprogrammable interconnect devices such that each of said reprogrammable interconnect devices is connected to at least one but not all of said programmable I/O terminals on each of said reprogrammable logic devices; and

an interface structure arranged to provide signal paths for signals carrying information to or from designated ones of said functional elements in said reprogrammable logic devices.

(CX-6, '496 patent at col. 88, ln. 63 - col. 89, ln. 28).

419. Claim 18 of the '496 patent read:

18. An electrically reconfigurable logic board for use in an electrically reconfigurable hardware emulation system which can be configured with a circuit design in response to the input of circuit information, said electrically reconfigurable logic assembly comprising:

a logic board structure;

a plurality of logic FPGAs mounted on said logic board structure, each of said logic FPGAs having internal circuitry which can be reprogrammably configured to provide functional elements selected from the group of at least combinational logic elements and storage elements, each of said logic FPGAs also having programmable I/O terminals which can be reprogrammably connected to selected ones of said functional elements configured into said logic FPGAs;

a plurality of interconnect FPGAs mounted on said logic board structure, each of said interconnect FPGAs having I/O terminals and internal circuitry which can be reprogrammably configured to provide interconnections between selected ones of said I/O terminals; and

a set of fixed electrical conductors connecting said programmable I/O terminals on said logic FPGAs to said I/O terminals on said

interconnect FPGAs such that each of said interconnect FPGAs is connected to at least one but not all of said programmable I/O terminals on each of said logic FPGAs.

420. Claim 20 of the '496 patent read:

> 20. An electrically reconfigurable hardware emulation system for emulating a digital logic network design, which digital logic network design can be represented by design data, said electrically reconfigurable hardware emulation system comprising:
>
> a computer adapted to receive design data input to said electrically reconfigurable hardware emulation system, said computer including a partitioning computer program which partitions the digital logic network design being emulated into portions, a routing computer program which assigns connections between said portions, and a configuration computer program which generates configuration information, said configuration information serving to program the partitioned and routed digital logic network design into said electrically reconfigurable hardware emulation system;
>
> a plurality of reprogrammable logic devices capable of receiving said configuration information, each of said reprogrammable logic devices having internal circuitry which can be reprogrammably configured to provide functional elements selected from the group of at least combinatorial logic elements and storage elements, each of said reprogrammable logic devices also having programmable I/O terminals which can be reprogrammably connected to selected ones of said functional elements configured into said reprogrammable logic devices;
>
> a plurality of reprogrammable interconnect devices capable of receiving said configuration information, each of said reprogrammable interconnect devices having I/O terminals and internal circuitry which can be reprogrammably configured to provide interconnections between selected ones of said I/O terminals; and
>
> a set of fixed electrical conductors connecting said programmable I/O terminals on said reprogrammable logic devices to said I/O terminals on said reprogrammable interconnect devices such that each of said reprogrammable interconnect devices is connected to at least one but not all of said programmable I/O terminals on each of said reprogrammable logic devices.

421. In a June 29, 1993 amendment submitted during prosecution of the '496 patent, which introduced patent claims 1, 2, 3 and 15 in issue, applicants argued that:

> The so-called 'partial crossbar' connectivity scheme for connecting FPGAs in Applicants' logic emulation system is set forth in each of the new claims.

(CX-61 at QM48078 - 48088).

The Claim Term "An Electrically Reconfigurable Logic Assembly"

422. The preamble of the claims at issue in the '496 patent describe the field of invention as "[a]n electrically reconfigurable logic assembly for use in an electrically reconfigurable hardware emulation system. . ." The definitions recited in the Background and Summary of the Invention section of the '496 patent do not include a definition for the specific term "logic assembly," nor is there an antecedent usage of that term in the specification. (CX-6, col. 87, lns. 35-40, col. 88, lns. 63-68; Wolfe, Tr. at 2869-2870).

423. The claim term "logic assembly" was first employed in the language of Claim 1 when Claim 1 was presented to the Patent Office by way of a Preliminary Amendment, dated June 29, 1993, during the prosecution of the Butts '496 patent (CX-61, at QM48078). The Preliminary Amendment placed no restrictions on the term "logic assembly," nor were any such restrictions or limitations attributed to the term during subsequent prosecution of the Butts '496 patent (CX-61).

424. The term "assembly" is defined in mechanical terms as "[a] unit containing the component parts of a mechanism, machine, or similar device." *McGraw-Hill Dictionary of Scientific and Technical Terms* 133 (4th ed. 1989). The term "assembly" is also defined as:

> (2) (electric and electronics parts and equipments). A number of basic parts or subassemblies, or any combination thereof, joined together to perform a specific function. The application, size, and construction of an item may be factors in determining whether an item is regarded as a unit, an assembly, a subassembly, or a basic part. A small electric motor might be considered as a part if it is not normally subject to disassembly. The distinction between an assembly and a subassembly is not always exact: an assembly in one instance may be a subassembly in another where it forms a portion of an assembly.

IEEE Standard Dictionary of Electrical and Electronics Terms, 57 (3rd ed. 1984) (CRDX-

11).

425. Butts' technical interpretation of the term "assembly" in the preamble of the claims at issue in the '496 patent is as follows:

> Q. In Claim 1 of the '496, what does the word "assembly" mean?
>
> A. Well, an assembly is a collection of things. It is the noun which as the claim defines contains the following three primary elements: The plurality of reprogrammable logic devices, the plurality of reprogrammable interconnect devices and the set of fixed electrical conductors. And there are many, many, possible ways that that can find physical form. There are many possible assemblages, assembly is intentionally a general word. I mean if I meant chip or board, I would have said chip or board. In fact, Claim 18 does say "board."

(Butts, CX-210 at Q 53).

426. The preamble to claim 18 of the '496 patent is directed to "an electrically reconfigurable logic board" (CX-6, at col. 89, lns. 57-63). Claim 20 of the '496 patent is directed to an electrically reconfigurable hardware emulation "system" containing reprogrammable logical devices and reprogrammable interconnect devices (CX-6, col. 90, lns. 22-64). During prosecution of the '496 patent, applicants submitted a September 14, 1994 Amended Information Disclosure Statement, which argued:

> An electrically reconfigurable logic assembly incorporating Applicants' unique partial crossbar architecture is defined most broadly in independent claim 19 [patent claim 1]. The elements of [claim 1] include reprogrammable logic devices with functional logic elements, reprogrammable interconnect devices and fixed electrical conductors arranged in a partial crossbar configuration for electrically connecting the reprogrammable logic devices to one another through the reprogrammable interconnect devices. Applicants' independent [claim 15] adds an interface structure to the reconfigurable logic assembly of [claim 1], while Applicants' independent [claim 17] defines the reprogrammable logic devices as "logic FPGAs" and the reprogrammable interconnect devices as "interconnect FPGAs". Independent [claim 18] calls for a logic board which includes the elements of [claim 17]. Independent [claim 20] and [claim 23] are system-level claims which respectively utilize the broadly defined and more narrowly defined reconfigurable logic assemblies of [claim 1] and [claim 17] in conjunction with a computer programmed for partitioning and routing.

(CX-61 at QM48262-263).

427. [

]

The Claim Term "Plurality of Reprogrammable Logic Device"

428. The claims at issue in the '496 patent require a plurality of "reprogrammable logic devices" (CX-6, col. 87, ln 41). Those "reprogrammable logic devices" must "hav[e] internal circuitry which can be reprogrammably configured to provide functional elements selected fro the group of at least combinatorial logic elements and storage elements," as well

as "programmable I/O terminals which can be reprogrammably connected to selected ones of said functional elements configured into said reprogrammable logic devices." (CX-6, col. 87, lns. 42-51). There is no antecedent usage or definition of the term "reprogrammable logic device" in the specification of the '496 patent.

429. The specification of the '496 patent defines "logic chip" as:

> an ERCGA used to realize the combinational logic, storage and interconnectins of an input design in the Realizer system.

(CX-6, col. 2, lns. 19-21).

430. A reconfigurable "logic chip device" is described as follows:

> For a device to be useful as a Realizer logic chip, it should be an electronically reconfigurable gate array (ERCGA):
>
> 1) It should have the ability to be configured according to any digital logic network consisting of combinational logic (and optionally storage), subject to the capacity limitations.
>
> 2) It should be electronically reconfigurable, in that its function and internal interconnect may be configured electronically any number of times to seek many different logic networks.
>
> 3) It should have the ability to freely connect I/O pins with the digital network, regardless of the particular network or which I/O pins are specified, to allow the Realizer System partial crossbar or direct interconnect to successfully interconnect logic chips.

(CX-5, col. 7, lns. 32-47).

431. Whether or not a device is a logic device or an interconnect device is not simply a matter of the physical characteristics of the device. Thus, the specification of the '496 patent teaches with respect to the preferred embodiment, that the same Xilinx Logic Cell Array (LCA) is used for both logic chips and interconnect chips (CX-6, col. 8, lns. 26-28, col. 9, lns. 26-27). The segregation of logic versus interconnect devices is accomplished

by identifying or setting aside certain devices as logic resources which can be used by the emulation system to perform the logic functionalities associated with the user's circuit design. This segregation and identification process is carried out in the software structure which operates the emulation system. Respondents' expert Wolfe testified that:

> Q. What does the phrase reprogrammable logic devices mean in the context of claim 1 of the Butts '496 patent?
>
> A. Well, this is a problem throughout the patent, both patents, is that it's not made clear -- both the terms reprogrammable logic device and reprogrammable interconnect device are used. They're used separately. And, therefore, it's clear to me that they are intended to refer to separate things.
>
> But there's no definition that enables one to determine whether or not a particular device is a reprogrammable logic device or a reprogrammable interconnect device.
>
> And, in fact, in most of the discussions and in the preferred embodiment, the same physical devices are used. You can't look at the physical device and say that is a reconfigurable logic device, a reprogrammable logic device or that is a reprogrammable interconnect device.
>
> So given that, I believe there are only two possible methods to distinguish what is a reprogrammable logic device and what is a reprogrammable interconnect device. One is to simply accept the designer's labeling of the device as a logic device and an interconnect device. That doesn't necessarily make a lot of sense, but at least it allows you to have a name for each device.
>
> Or what seems to make the most sense to me is that if a device is used to implement logic, then it is a logic device. And if a device is used to implement interconnect, it is an interconnect device.

(JX-16, Wolfe Tr. at 93-94).

432. "Reprogrammable logic devices" as used in Claim 1 of the Butts '496 patent also include collections of discrete chips. With respect to "system-level interconnects" the specification of the '496 patent teaches that:

> One means of interconnecting logic boards is to reapply the partial crossbar interconnect hierarchically, treating each board as if it were a logic chip, and interconnecting board I/O pins using an additional set of crossbar chips.

(CX-6, col. 23, lns. 15-19). The specification further teaches:

> To distinguish among crossbar chips in a Realizer system, the partial crossbar interconnect which interconnects logic chips is called the X-level interconnect, and its crossbar chips are called Xchips. The interconnect which interconnects logic boards is called the Y-level interconnect, and its crossbar chips are called Ychips. In the X-level interconnect, the I/O pins of each logic board are divided into proper subsets, using the same division on each logic board. The pins of each Ychip are connected to the same subset of pins from each of every logic board. As many Ychips are used as there are subsets, and each Ychip has as many pins as the number of pins in the subset times the number of logic boards.
>
> * * *
>
> A specific example is the preferred embodiment:
>
> The partial crossbar interconnect is used hierarchically at three levels across the entire hardware system.
>
> A logic board consists of up to 14 logic chips, with 128 interconnected I/O pins each, and an X-level partial crossbar composed of 32 Xchips. Each Xchip has four paths to each of the 14 Lchips (56 total), and eight paths to each of two Ychips, totaling 512 logic board I/O pins per board.
>
> A box contains one to eight boards, with 512 interconnected I/O pins each, and a Y-level partial crossbar composed of 64 Ychips. Each Ychip has eight paths to an Xchip on each board via logic board I/O pins, and eight paths to one Zchip, totaling 512 box I/O pins per box.
>
> A rack contains one to eight boxes, with 512 interconnected I/O pins each, and a Z-level partial crossbar composed of 64 Zchips. Each Zchip has eight paths to a Ychip in each box via box I/O pins.

(CX-6, col. 23, lns. 25-38, col. 23, ln. 65 - col. 24, ln. 16).

433. The Butts '496 patent teaches that correspondence between the actual elements of the user's circuit design and the functional elements of the logic devices is not required (CX-6, col. 48, lns. 56-65, col. 49, lns. 4-15, and col. 49, lns. 24-27). A correspondence between the behavior or functionality of the user's logic circuit design and functionality of

the functional elements is required Id.

434. Claim 1 of the '496 patent requires reprogrammable logic devices having "programmable I/O terminals" that "can be reprogrammably connected to selected ones of said functional elements configured into said reprogrammable logic devices." (CX-6 at col. 87, lns. 47-51). There is no antecedent usage of the claim term "programmable I/O terminals" in the '496 specification. However, the specification teaches that logic chip devices :

> should have the ability to freely connect I/O pins with the digital network, regardless of the particular network or which I/O pins are specified. . . .

(CX-6, col. 7, lns. 56-61). The specification further teaches, with respect to the partial crossbar interconnect:

> The logic chip itself can offer an additional degree of freedom which crossbars do not exploit, because it has the ability to be configured to use any of its I/O pins for a given input or output of the logic network it is being configure for, regardless of the particular network. That freedom allows the possibility of the partial crossbar interconnect, which is the reason it is specified in the definition of the logic chip.
>
> * * * *
>
> . . . . Since the logic chip can be configured to use any I/O pin [that] may be assigned to the logic configured in a logic chip which is connected to a net, one I/O pin is as good as another.

(CX-6, col. 16, lns. 6-13, 34-37).

435. Respondents' Wolfe testified, regarding the claim term "programmable I/O terminals" as follows:

> Q. . . . Going on to the phrase "firm [sic] programmable I/O terminals," what does that mean to you in the context of claim 1 of the Butts 496 patent?
>
> A. Again, it's not perfectly clear. The technology that -- the term is not well defined, but the technology that is constantly referred to in the patent describes I/O terminals that can be programmed as to their

functionality. For example, their polarity, whether or not they are what we call push-pull or totem pole outputs or tristate outputs, whether or not they contain storage elements in and of themselves. Those are the characteristics in these devices that are constantly discussed throughout the patent, and that is one interpretation of programmable I/O terminals.

Q. What does the term programmable I/O terminals mean you to in the context of claim 1 of the Butts 496 patent?

A. I don't know if those words alone mean anything because of the way that they are typically used. Clearly intent is to describe a system, and the language in the patent is where the logic device, the reprogrammable logic device should have the ability to freely connect I/O pins with the digital network, regardless of the particular network or which I/O pins are specified, and I don't know whether or not he intended modifier programmable to refer to that capability or to the other capability of the I/O terminals. All the devices that he discussed have both capabilities.

Q. Now, after the phrase programmable I/O terminals in the claim, there's a continuation of the language, to wit, "which can be reprogrammably connected to selected ones of said functional elements connected into reprogrammable logic devices." Do you see that terminology?

A. Yes, I see that.

Q. Do you see programmable I/O terminals in the claim?

A. As I said, I haven't attempted to define what individual words mean in the claim. I think that that tells me something about the device that's being described in that complete phrase.

(Wolfe, Tr. at 2896-7). Wolfe later testified :

Q. . . . What is your definition of programmable I/O terminals in the context of claim 1 of the Butts '496 patent?

A. Based on my understanding of the devices that were described in the early part of the patent specification, I believe the programmable I/O terminals were referring to I/O terminals which have capability of performing different I/O functions such as inverting polarity, tristate functions, and incorporation of latches.

(Wolfe, Tr. at 3020).

436. Complainant's McCluskey testified that the claim limitation "programmable

I/O terminals" does not mean that any I/O pin on the reprogrammable logic device must be connectable to any functional element within the reprogrammable logic device (McCluskey, CRX-52A at Q R124, R131). Thus he testified:

> A. [DR. McCLUSKEY] ... Claim 1 says that programmable I/O terminals are I/O terminals which can be "reprogrammably connected to selected ones of said functional elements configured into said reprogrammable logic devices." I think the dispute here is whether this has to allow a perfect mapping from any arbitrary I/O pin into any arbitrary point in the digital network. I think that's far too strong an interpretation. There's nothing in the claim language that requires such a limitation, and there's nothing in the discussion of the patent that would lead an engineer to believe that such a strong reprogrammable I/O facility is required in order for the emulation systems described in the patent to be useful.

(McCluskey, CRX-52A, at Q R131).

437. The specification of the '496 patent teaches that the "freedom of connection" requirement identified in Col. 7 of the '496 specification need not be fully satisfied in a reprogrammable logic chip in order for that reprogrammable logic chip to serve as a "reprogrammable logic device" within the context of claim 1. Specifically, the '496 patent teaches that:

> Still another type of reconfigurable logic chip which could be used as a logic chip is the EEPLD, or electrically erasable programmable logic device . . . A commercial example is the Lattice Generic Array Logic (GAL). . . . It offers freedom of connection of I/O pins to logic only among all input pins and among all output pins, so it partially satisfies that requirement. . . . It can, however, be used as a Realizer logic chip.

(CX-6, at col. 8, lns. 50-63) (emphasis added).

The Claim Term "Reprogrammable Interconnect Devices"

438. The claims at issue in the '496 patent require a plurality of reprogrammable interconnect devices. (CX-6, '496 patent at 51-57).

439. The interconnect devices recited in the claim of the '496 patent must have

"I/O terminals and internal circuitry which can be reprogrammably configured to provide interconnections between selected ones of said I/O terminals." (CX-6, col. 87, lns. 53-57).

440. The claim term "reprogrammable interconnect device" is not expressly defined in the specification of the '496 patent. However, the specification defines "interconnect chip devices" as follows:

> Interconnect chips include crossbar chips, used in full and partial crossbar interconnects, and routing chips, used in direct and channel-routed interconnects. For a device ot be useful as a Realizer interconnect chip:
>
> 1) It should have the ability to establish many logical interconnections between arbitrarily chosen groups of I/O pins at once, each interconnection receiving logic signals from its input I/O pin and driving those signals to its output I/O pin(s).
>
> 2) It should be electronically reconfigurable, in that its interconnect is defined electronically, and may be redefined to suit many different designs.
>
> 3) If a crossbar summing technique is used ot interconnect tri-state nets in the partial crossbar interconnect, it should be able to implement summing gates. (If not, other tri-state techniques are used, as discussed in the tri-state section.)
>
> The ERCGA devices discussed above, namely the LCA, the ERA and the EEPLD, satisfy these requirements, so they may be used as interconnect chips. Even though little or no logic is used in the interconnect chip, the ability to be configured into nearly any digital network includes the ability to pass data directly from input to output pins.

(CX-6, col. 9, lns. 3-26).

441. The specification teaches with respect to the "Crossbar Summing Configuration" that:

> The crossbar chip must have one or more logic elements for the summing gate. Crossbar summing deviates from the practice of putting all logic in the logic chips and none in the crossbar chips, but an important distinction is that the logic placed in the crossbar chip is not part of the realized design's logic. it is only logic which serves to accomplish the interconnection functionality of a tri-state net.

(CX-6 at col. 20, lns. 4-11).

The Claim Term "A Set Of Fixed Electrical Conductors"

442. Claim 1 of the '496 patent requires a set of "fixed electrical conductors." "Fixed electrical conductors" are physical traces or conductors (Wolfe Tr. at 100:5-9, JX-16) which connect the programmable I/O terminals on the reprogrammable logic devices to the I/O terminals of the reprogrammable interconnect devices in claim 1. These connections are made such that each of the reprogrammable interconnect devices is connected "to at least one but not all" of the reprogrammable I/O terminals on each of the reprogrammable logic devices. (CX-6, col. 87, lns. 58-65).

443. The claims at issue in the '496 patent require "a set of fixed electrical conductors" connecting I/O terminals of the logic devices to I/O terminals of the interconnect devices such that each of the interconnection devices is connected to at least one but not all of the I/O terminals of each logic device. Complainant's McCluskey referred to this type of interconnection as what the specification defines as the "partial crossbar" interconnection. Thus, he testified:

> A. . . . . Then these two types of devices, these logic and interconnect devices, must be connected together by means of fixed electrical conductors. Claim 1 then requires, what I was calling earlier, the partial crossbar structure, in which each interconnect device has to be connected to at least one terminal on each of the logic devices but not to all of the terminals on any of the logic devices. So, this is my understanding of claim 1 of the '496 Butts patent.

(CX-214, McCluskey at Q 59).

444. The partial crossbar interconnect architecture is a blocking architecture, which means that there is no guarantee that every net can always be successfully interconnected. (Butts, CX-210 at 32). The '496 patent state that:

> Partial crossbar interconnects cannot handle as many nets as full crossbars can. The partial crossbar interconnect will fail to interconnect a net when the only I/O pins not already used for other nets on the source logic chip go to crossbar

chips whose paths to the destination logic chip are likewise full. The destination may have pins available, but in such a case they go to other crossbars with full source pins, and there is no way to get from any of those crossbars to the first.

* * *

Analysis and computer modeling has been conducted on the number of input design nets which can be interconnected by different partial crossbar interconnect architectures. Results indicate that a narrow partial crossbar is nearly as effective as a wide one or even a full crossbar. For example, the interconnect used on the logic board in the preferred implementation (14 128-pin logic chips, 32 56-pin crossbar chips) showed 98% of the interconnect capacity that a full crossbar would have.

It is extremely rare for real input designs to demand the maximum available number of multi-logic-chip nets and logic chip pins, as was assumed in the modeling.

(CX-6, col. 17, lns. 24-32, col. 18, lns. 3-15).

445. During prosecution of the '496 patent, in a September 14, 1994 "Amended Information Disclosure Statement," applicants argued:

Applicants have invented a new and highly useful connectivity scheme for a hardware logic emulation system, wherein reprogrammable logic devices capable of implementing the functional logic components of a digital logic circuit design undergoing emulation are interconnected to one another via a novel partial crossbar" architecture. Applicants' partial crossbar architecture employs a combination of reprogrammable interconnect devices and fixed electrical conductors arranged such that each interconnect device is connected to at least one but not all of the I/O terminals of the logic devices. The connection paths established through the logic device I/Os, fixed electrical conductors and reprogrammable interconnect devices for a given digital logic circuit design undergoing emulation are circuit-switched paths as opposed to message-switched paths. Hence, the connection paths are dedicated to one source I/O and its destination I/O(s) in static fashion, meaning the same paths are used between the source and destination I/Os for the entire connection lifetime.

* * *

An electrically reconfigurable logic assembly incorporating Applicants' unique partial crossbar architecture is defined most broadly in independent claim 19. The elements of claim 19 include reprogrammable logic devices with functional logic elements, reprogrammable interconnect devices and fixed

> electrical conductor arranged in a partial crossbar configuration for electrically connecting the reprogrammable logic devices to one another through the reprogrammable interconnect devices.

(CX-61 at QM48262).

446. The February 16, 1995 "Examiner's Statement of Reasons for Allowance" in the '496 prosecution history stated:

> During the 10 August 1994 interview, applicants' representative repeatively [sic] stated that the claimed invention is directed to an electrically reconfigurable logic assembly incorporating the unique **partial crossbar architecture** in a hardward [sic] logic **emulation system**. The examiner agrees that the prior arts of record fail to specifically disclose such a unique claimed **partial crossbar architecture** for use in a hardward [sic] logic emulation system

(CX-61 at QM48321) (emphasis in original).

447. In a September 14, 1994 Amended Information Disclosure Statement, submitted during prosecution of the '496 patent, applicants argued that:

> Significantly, Applicants' partial crossbar architecture is a blocking architecture. The completion of each succeeding connection path between logic device I/Os for a given digital logic circuit design undergoing emulation is not guaranteed. This is in distinct contrast to non-blocking connection schemes, where a connection path between any two remaining unconnected points in the system is always guaranteed regardless of the previous connection paths which have been established. Indeed, part of Applicants' inventive contribution to the field of logic emulation is the non-obvious recognition that a partial crossbar interconnection architecture, despite its blocking nature, will provide sufficient routing resources to realize a practical number of circuit-switched connection paths -- and a corresponding practical number of arbitrary logic circuit designs -- in a reconfigurable environment.

(CX-61 at QM48262).

448. To distinguish over the Spandorfer reference "Synthesis of Logic Functions on an Array of Integrated Circuits," applicants in the prosecution of the '496 patent argued as follows:

> The Spandorfer report in particular, entitled "Synthesis of Logic

Functions on an Array of Integrated Circuits", Contract Report AFCRI-66-298 (October 31, 1965), discloses a scheme for connecting macrocellular arrays of logic gates (i.e., NAND gates) to one another through a Clos-type switching network (see Spandorfer, pages 3-13 to 3-14).

* * *

The Spandorfer reference does raise the question of whether logic cell connections can be made using a structure "which realistically permit(s) a certain level of blocking", and then goes on to imply that the Clos-type network which interconnects Spandorfer's macrocellular array is a blocking network (see Spandorfer, page 3-13). Spandorfer's implication is incorrect. Putting aside the observation that Spandorfer fails to discuss any of the considerations and constraints associated with logic emulation -- and thus does not answer any questions about whether blocking connectivity schemes would work in a logic emulation environment -- the three-stage Clos network which Spandorfer discusses in his reference is in fact a non-blocking network (see, i.e., Clos, "A Study of Non-Blocking Switching Networks," *The Bell System Technical Journal*, March 1953, pp. 406-424; the Clos reference is further discussed below).

Spandorfer suggests a "second approach" to connecting logic cells, using an arguable blocking network in the form of a (d,k) graph structure (see Spandorfer, pages 3-13 to 3-19). . . .

Again, Spandorfer does not address the issues raised when a blocking interconnection configuration is applied in the context of a logic emulation system, where circuit-switched connection paths subject to arbitrary reconfiguration are required. Spandorfer properly understood thus teaches away from Applicants' claimed partial crossbar interconnection architecture, which, as noted above, is a blocking architecture intuitively unsuited for logic emulation systems.

(CX-61 at QM48265-266).

Language of Claim 2

449. Claim 2 of the '496 patent depends from Claim 1. The claim language defines the reprogrammable logic devices of Claim 1 as "programmable gate arrays." Claim 2 of the '496 patent does not expressly define the term "programmable gate array," nor does there appear to be an antecedent usage of that term in the specification. However, the specification of the '496 patent does define an "electronically reconfigurable gate array."

(CX-6, col. 2, lns. 13-18).

450. In the most general sense, "programmable gate arrays" are integrated circuit devices which contain both programmable logic elements and the means to reprogrammably interconnect those logic elements both internally and to external components (Sapiro Tr. at 762 and 851-852; Sapiro, CX-215, Q&A 78).

451. The specification of the '496 patent defines an "ERCGA" as:

> an electronically reconfigurable gate array, that is a collection of combinational logic, and input/output connections (and optionally storage) whose functions and interconnections can be configured and reconfigured many times over, purely by applying electronic signals.

(CX-6, col. 2, lns. 13-18).

Language of Claim 3

452. The specification of the '496 patent cites the Xilinx Logic Cell™ Array ("LCA") as a suitable logic device for the claimed invention. During prosecution of the '496 patent, applicants argued in an August 10, 1994 Transmittal Letter that:

* * *

> Examiner advised Applicants' undersigned attorney that a question had arisen as to whether the disclosure of the above-identified application supported claims specifically drawn to the use of FPGA devices. Although the precise term "FPGA" does not expressly appear in the specification or drawings of the above-identified application, FPGAs are inherently disclosed in the application.

* * *

> In a preferred embodiment of Applicants' invention, the ERCGAs are Xilinx XC3090 LCA chips. At the time Applicants' priority application was filed (on October 5, 1988), Xilinx LCA were also known to those of ordinary skill in the art as FPGAs. See, e.g., Graf, "A Field Programmable gate Array," Proceedings of the 6th International Conference on Custom and Semicustom Ics, November 4-6, 1986, attached hereto as Exhibit A. - See also the article entitled "Filed programmable logic sequencer," Electronic Engineering, p. 97, December 1977, attached as Exhibit B. Thus, Applicants' disclosure literally encompasses the use of FPGAs as reprogrammable logic chips.

(CX-61 at QM48110-111).

453. The Xilinx LCA is a FPGA, described in the specification as:

> An example of a reconfigurable logic chip which is suitable for logic chips is the Logic Cell Array (LCA) ("The Programmable Gate Array Handbook", Xilinx, Inc., San Jose, Calif., 1989). It is manufactured by Xilinx, Inc., and others. This chip consists of a regular 2-dimensional array of Configurable Logic Blocks (CLBs), surrounded by reconfigurable I/O Blocks (IOBs), and interconnected by wiring segments arranged in rows and columns among the CLBs and IOBs. Each CLB has a small number of inputs, a multi-input combinational logic network, whose logic function can be reconfigured, one or more flip-flops, and one or more outputs, which can be linked together by reconfigurable interconnections inside the CLB. Each IOB can be reconfigured to be an input or output buffer for the chip, and is connected to an external I/O pin. The wiring segments can be connected to CLBs, IOBs, and each other; to form interconnections among them, through reconfigurable pass transistors and interconnect matrices. All reconfigurable features are controlled by bits in a serial shift register on the chip. Thus the LCA is entirely configured by shifting in the "configuration bit pattern", which takes between 10 and 100 milliseconds. Xilinx 2000 and 3000-series LCA's "FPGAs" have between 64 and 320 CLBs, with between 56 and 144 IOBs available for use.

(CX-6, col. 7, ln. 62 - col. 8, ln. 20).

454. "Field programmable gate arrays" are "programmable gate arrays" which can be programmed after they leave the manufacturer (McCluskey CX-214, Q&A 76).

Language of Claim 15

455. Claim 15 of the '496 patent is an independent claim that includes virtually the same language as claim 1, but has the additional limitation of "an interface structure arranged to provide signal paths for signals carrying information to or from designated ones of said functional elements in said reprogrammable logic devices." (CX-6, '496 patent at col. 88, lns. 63, col. 89, lns. 28).

456. The '496 patent describes an interface for user-supplied devices ("user-supplied device module"). Specifically, the '496 patent states:

> Since the input design is realized in actual working hardware in the form of

configured logic and interconnection chips, it is practical and desirable to connect other actual hardware devices to the Realizer system. These may be any devices with digital inputs and outputs, such as microprocessor or other VLSI IC chips, digital/analog converters, display devices, input keyboards and switches, storage devices, computer input/output busses, etc. These may also be parts of digital systems, such as circuit boards or larger scale components, of which the realized design is a part.

* * *

There is such a variety of possible USDs that it is useful to provide a Realizer system with a standard means for a user to connect such devices to the Realizer system hardware. This means is the user-supplied device module (USDM)

The user-supplied device module:

1) Provides a means of physically connecting user supplied hardware devices.

2) Provides connections between the USDs and Realizer system logic and/or interconnection chips. Since the USDs fulfill roles in the design similar to logic chips, it is expedient to interconnect USDMs inthe same way as logic chips.

3) Provides the ability to freely assign USD pins to interconnect pins, as the logic chips normally installed in the L Chip location do.

Since it should provide capabilities similar to what a memory module provides for its RAM chips, the architecture of the USDM is similar to that of a memory module. FIG. 38 shows the USDM architecture.

* * *

A terminal block provides a means for making electrical connections between device input and output pins and the USDM logic chips, through a connector terminal strip, set of printed circuit board pads, or other such means.

(CX-6, col. 39, lns. 11-22, 41-62, 68, col. 40, lns. 1-4).

457. During prosecution of the '496 patent, applicants argued with respect to claim 1 that:

Claim 19 [issued claim 1] . . . defines the electrically reconfigurable logic assembly which forms the basic hardware component in the preferred embodiment of the novel reconfigurable hardware emulation system which is the subject of the '734 application. The claim elements include

> 'reprogrammable logic devices' with functional elements, 'reprogrammable interconnect devices' and a 'partial crossbar' connectivity scheme with 'fixed electrical conductors' or electrically connecting the reprogrammable logic devices to one another via the reprogrammable interconnect devices.

(CX-61 at QM48091). Applicants further argued with respect to claim 17 and claim 18:

> Claim 35 [issued claim 17] is a more detailed version of Claim 19.[issued claim 1]. The reprogrammable logic devices of Claim [1] are specifically defined as 'logic FPGAs' and the reprogrammable interconnect devices of Claim [1] are specifically defined as 'interconnect FPGAs'.
>
> * * *
>
> Claim 36 [issued claim 18] defines an electrically reconfigurable logic board which includes all of the detailed elements recited in Claim [17] mounted on a 'logic board structure.'

(CX-61 at QM48092).

K. Validity

Prior Art

458. Conception and reduction to practice of the Realizer, the preferred embodiment of the '473 and '496 patent, is set forth in Butts' December 21, 1993 affidavit to the U.S. Patent and Trademark Office. (Butts, CX-210, Attachment N).

459. Butts' earliest conceptions relating to the reprogrammable interconnect architecture disclosed in the specification maturing as the '496 and '473 patents occurred between[ ]and were recorded in a paper that he wrote for Mentor entitled *Reconfigurable Hardware for Logic Simulation: Description of Concept*[ ](Butts, CX-210, Attachment N at QM54323, QM54337).

460. Butts'[ ]paper described a network of reconfigurable logic chips interconnected by their I/O pins. Butts stated under oath in his affidavit to the Patent Office that he "specifically had in mind using the reprogrammable electrical conductors in at least

465. Butts stated under oath in his affidavit to the Patent Office that the subject matter of the specification that matured as the '473 and '496 patents was first reduced to practice in[ ](Butts, CX-210, Attachment N at QM54325).

The Sample '353 Patent

466. United States Patent Number 5,109,353, ('353 patent) entitled "Apparatus for Emulation of Electronic Hardware System" issued on April 28, 1992 from Application Number 279,447 filed on December 2, 1988 (CX-3). The named inventors are Stephen P. Sample, Michael R. D'Amour, and Thomas S. Payne (CX-3).

467. The '353 patent contains additional disclosure beyond what constituted Quickturn's actual work as of[ ] Specifically, the 3x3 array disclosed in Figure 1 of the '353 patent was never constructed by Quickturn. Thus, Sample testified:

> Q. I would like to ask you now a series of questions regarding the existence of devices at Quickturn prior to December 2nd, 1988, which is the filing date leading to your '353 patent. The first question is, did Quickturn have any emulation system that had a 3 by 3 array?
>
> A. No. [

] The test results for the prototype are shown on Exhibit Q (QM54661) of CX-64. (CX-64, Exh. Q, QM54661).

469. The Sample et al. prototype logic emulation board contained a[ ]of FPGAs interconnected using "nearest-neighbor" architecture. [

](CX-64, at QM54378, QM54445; Sample Tr. at 1219, 1224).

470. The Sample et al.[ ]which was manufactured and tested at Quickturn did not have specific FPGAs which were designated for interconnect, and other FPGAs which were designated for logic. The FPGAs in the Quickturn[ ]arrangement were designed to accomplish both interconnect and logic functions. (Sample, Tr. at 1089, 1091, 1134, 1135, 1136, 1141, 1142, 1145, 1156, 1160; Payne, JX-1, at 60, 64). The only evidence presented as to the actual utilization of the FPGAs in the[ ]demonstrates that each FPGA used at least some of its logic function. (Sample, Tr. at 1136; CX-64, Exhibit Q).

471. RX-49 is a declaration of Sample dated September 26, 1991, which was submitted, pursuant to 37 CFR §1.131, in connection with the prosecution of the '353 patent. (RX-49, Sample Tr. at 1053)

472. CX-64 is an April 13, 1994 affidavit of Sample, Mike D'Amour and Thomas Payne, the three named inventors of the '353 patent, submitted under 37 CFR §1.131 in the prosecution of Application Serial No. 08/171,348, which resulted in the issuance of patent no. 5,329,470. This document details the conception and reduction practice of the subject matter of the '353 patent. (CX-64).

473. In the affidavit submitted in the prosecution of Application Serial No. 08/171,348 (CX-64), Sample and D'Amour stated that they were employed by Quickturn at the time of the execution of the affidavit. (CX-64, at QM54373).

474. The '353 specification stated the following:

> "The heart of the system of the present invention is emulation array 16. Emulation array 16 includes a plurality of programmable gate array devices 18. The programmable gate array devices 18 are arranged in a matrix. For illustrative purposes only, emulation array 16 of figure 1 is shown as a 3 x 3 matrix containing nine total gate arrays, denoted by reference numerals 18a to 18i. Those of ordinary skill in the art will readily recognize that the 3 x 3 array depicted in figure 1 is for illustration only in that, in an actual

embodiment, the size of emulation array 16 is limited only by simple design choice." (CX-3, Col.3, lines 25-35).

475. The FPGAs used in the prototype of the '353 patent served a mixed logic/interconnect function, and were not segregated into logic chips and interconnect chips. Thus, Sample testified:

> Q. Can you characterize these FPGAs as both interconnect chips and logic chips?
>
> A. I think it's misleading to call them either interconnect or logic chips. They served a mixed function. There was no attempt made to divide them between those two functions.
>
> Q. Should we then call them interconnect and logic chips?
>
> A. That would probably be a better thing to call them.
>
> Q. And your design would not work unless some of these chips had interconnect, isn't that correct?
>
> A. Interconnect meaning the function of connecting between traces on the PC board, yes, I would say that's correct.
>
> Q. And your design would not work unless some of these chips contained logic?
>
> A. Well, obviously you can't have a design unless some of the chips contain logic.

(Sample, Tr. at 1091; see also Sample Tr. at 1089, 1134-1135, 1141-1142, 1150; Payne, JX-1 at 60).

476. The programmable gate array devices used in the prototype of the '353, and described in the '353 patent, are XC3090 integrated circuits manufactured by Xilinx Corporation. (CX-3 at col. 3, lns. 46-52; Sample, Tr. 1067-1068).

477. Figure 2 of the '353 patent shows a portion of an emulation array which includes four programmable gate array devices interconnected as they would be in the matrix. However, the text relating to this figure does not teach separating interconnect and

logic functions. Thus the specification of the '353 patent teaches as follows:

> Referring now to FIG. 2, a portion of the emulation array 16 of the system 10 of the present invention is shown to include programmable gate array devices 18a, 18b, 18d and 18e, interconnected as they would be in the matrix. In the example shown in FIG. 2, an AND-gate 30 is shown in programmable gate array 18e, having its first input connected through conductor 32 in programmable gate array 18a, conductor 34 in between gate arrays 18a and 18b conductor 34 in between gate arrays 18a and 18b conductor 33 in gate array 18b, and conductor 36 in between gate arrays 18b and 18e.
>
> * * * *
>
> Those of ordinary skill in the art will readily recognize that the example shown in FIG. 2 is a simplified example for illustrative purposes only and that in an actual circuit emulation, programmable gate arrays 18a, 18b, 18d and 18e shown in FIG. 2 will contain more logic functions and will be much more richly connected. In fact, once configured, the emulation array will contain the entire circuit to be emulated, with the exception of any VLSI components, which may be externally connected to the emulation array as shown with respect to FIG. 3.

(CX-3, fig.2, col. 5, lns. 50-59, col. 6, lns. 3-13) (emphasis added).

478. In an actual implementation of a[ ]array disclosed in the prosecution of the Sample '353 patent as part of a Declaration submitted by Sample (CX-64 p. QM-54661) (RPX-13), one half of the 16 FPGAs used two percent (2%) or less of the logic facility on the FPGA. The remaining half had greater than two percent (2%) of the logic facility used. That example was used as evidence of the actual construction and operation of the Sample emulator prior to the date of the Butts patent. (CX-64 p. QM-54661, RPX-13, RDX-10AC).

479. Sample testified regarding the actual implementation reflected in CX-64 Attachment Q as follows:

> Q. So half of the FPGAs in this prototype had only two percent of the logic clbs utilized, is that correct?
>
> A. Yes. This was a quite small design, therefore, not many of the chips had a large percentage of the logic used.

(Sample, Tr. at 1087; see also Sample Tr. at 1090, 1136).

Xilinx FPGA

480. Prior to the date of the Butts invention, there were two types of Xilinx FPGAs which existed, namely, the Xilinx 2000 and 3000 series FPGAs. These FPGAs had three main functional components -- the reconfigurable input/output, the configurable logic blocks and the interconnect resources. Figure 2.3.1 of the Trimberger book entitled "Field - Programmable Gate Array Technology" (Butts, CRX-48, Attachment A at 19) shows the general arrangement of these three components. Generally, the input/output (I/O) resides at the periphery of the chip. The logic blocks are generally arranged in an array of rows and columns. The programmable interconnect is placed in the regions between the logic blocks and provides the interconnect functions. (Butts, CRX-48, Q 2; Butts, CRX-48, Attachment A at 19; RX-54, at 1; Wynn, Tr. at 2319).

481. The interconnect resources for the Xilinx 3000 series consisted of three different types of interconnect resources -- the long lines, the direct interconnect and the general purpose interconnect. The long lines were horizontally and vertically placed metal segments which spanned the entire width or height of the array. The long lines bypassed the switch matrices of the general purpose interconnect. The direct interconnections connected horizontally and vertically adjacent blocks. The general purpose interconnects consisted of short metal segments connected by switch matrices. They permitted the various logic blocks to be connected. (Butts, CRX-48 at Q 3-6; RX-54, at 4-5; Wynn, Tr. at 2319 - 2330; RX-4, at 1-14 to 1-16).

482. An FPGA is a general purpose integrated circuit which can be user programmed to cause it to configure itself to become a user specified logic circuit. FPGAs are particularly suitable for in-circuit emulation and debugging since, once programmed with the initial circuit design, they can be reprogrammed as many times as desired to implement

design changes, and even entirely new circuits. (Wynn, RX-706 at Q 4). Prior to the date of the Butts invention, there were two types of Xilinx FPGAs which existed, namely, the Xilinx 2000 and 3000 series FPGAs. (Butts, CRX-48 at Q 2; see also, CRX-48, Attachment A at 19).

483. An FPGA has three basic components: (1) Logic blocks (called configurable logic blocks or CLBs), (2) Programmable input/output (I/O) interfaces, and (3) A programmable interconnect network between the logic blocks themselves and between logic blocks and the I/O interfaces. (Wynn, RX-706 at Q 5).

484. The logic blocks were programmable to accomplish to a wide variety of basic logic functions including the well known standards such as AND, OR, NOR, NAND, etc. and to accomplish various higher order logic functions. These functions are called combinational logic. (Wynn, RX-706 at Q 6).

485. Field Programmable Gate Arrays existed prior to the Butts invention. Sample et al. discovered the use of FPGA's in emulators independently of Butts. Thus, Sample testified:

> Q. Is it fair to say that the advent of field programmable gate arrays in the marketplace was part of your inspiration in deciding to design an emulator such as that shown in your patent, sir?
>
> A. Field programmable gate arrays are one of the enabling factors that made this type of system practical. It could have been built earlier but it probably would not have been economically practical.
>
> * * *
>
> Q. . . . Field programmable gate arrays were invented and after their invention, a number of investors [sic] used those field programmable gate arrays to build emulators, including yourself, Mr. butts, the PiE people?
>
> A. That's true.

(Sample Tr. at 1161-62).

486. Butts was not the inventor of the idea of using a single FPGA to emulate a design. He did invent techniques for using multiple logic devices, which could be FPGA's. Butts taught the use of programmable interconnect to generally accomplish any interconnection among the FPGA's. (Butts Tr. at 407-408; CX-5; CX-6).

Wynn Article - "Designing With Logic Cell Arrays"

487. The Wynn article entitled "Designing With Logic Cell Arrays" (RX-54) describes the structure and function of the Xilinx 2000 series FPGAs, also known as LCAs. (RX-54)

488. The Wynn article RX-54 compares custom chips versus off-the-shelf programmable chips. Custom chips have certain recognized disadvantages relative to commodity FPGAs. One of the disadvantages of custom chips is nonrecurring engineering expense, which is the amount of money that must pay to have an initial prototype device manufactured. Another disadvantage is that a custom chip once built results in a product inventory that is specific to the function of the custom chip, and if changes are made later, those inventories waste money. (RX-54, p. 1, Wynn, Tr. at 2317 and 2318).

489. Pardner Wynn obtained a bachelor of science degree in electrical engineering from Stanford in 1981. He also received a master of science degree in electrical engineering from Sanford in 1982 and then undertook postgraduate course work and research at Stanford from 1982 to 1984. (Wynn, RX-706 at Q 1).

490. In 1986, Pardner Wynn became one of the early employees of Xilinx, a pioneer in field-programmable gate arrays (FPGAs). During that employment period, he worked with customers to implement their logic designs on FPGAs. (Wynn, RX-706 at Q 2)

491. The Wynn article "Designing with Logic Cell Arrays" (RX-54) specifically

taught an XACTOR emulator, described as a PC based in-circuit emulator permitting real time in-circuit emulation of up to four LCAs simultaneously. The XACTOR allowed emulation for debugging purposes by providing an interface which allowed alteration of the design and permitted the internal states to be read back during operation. (RX-54, Wynn, RX-706 at Q 13).

492. Each of the FPGA's in the XACTOR was contained in a "pod," and no pod was dedicated to any particular function (Wynn, Tr. at 2336). The XACTOR did not provide an interconnection between or among the FPGA's in the different pods (other than ground or power) (Wynn, Tr. at 2337-2338). Thus, there was no electronically reconfigurable interconnect between the FPGA's in the circuit under development, rather, those connections were made by the system under development itself, such as through a printed circuit board or wire-wrapped connection. (Wynn Tr. at 2338).

493. Butts was familiar with the XACTOR prior to the invention of the subject matter of the '473 and '496 patents. (Butts, Tr. 391:24-392:2).

Wynn Article - "In Circuit Emulation"

494. The Wynn article is entitled "In-Circuit Emulation for ASIC-Based Designs" and was published in VLSI Systems Design, October, 1986. The Wynn article (RX-12) teaches the use of a Xilinx FPGA (LCA) as an emulation technology to emulate the design of an ASIC (application specific integrated circuit) to test out the design before using it and before casting it into permanent form in the ASIC. (RX-12; Butts, CRX-48 at Q 11; Wynn, Tr. at 2334).

495. The Wynn article (RX-12) discloses a system using "pods" having only a single FPGA, and teaches up to four "pods" could be controlled simultaneously. There is no disclosure of an interconnect structure or architecture for connecting the multiple FPGA

devices, and there is no discussion regarding the partitioning of logic functions among various devices. (Butts, CRX-48 at Q 11; Wynn, Tr. at 2334).

Schmitz Article

496. The Schmitz article (RX-13) is entitled "Emulation of VLSI Designs Using LCAs" and was published in VLSI Systems Design on May 20, 1987.

497. The Schmitz article teaches the use of FPGAs as a prototyping technology in a hardwired prototype. The Schmitz article at page 58 provides that: "For most systems, the emulator would probably be created using wrapped-wire technology to allow easy changes and modifications." Regarding design changes, respondents' Wynn testified:

> Q. And if you look at page 58 of RX-13, left-hand column, last paragraph, where it starts for most systems the emulator would probably be created using wrapped wire technology to allow easy changes in modifications, that's at least one portion that indicates that he's suggesting wrapped wire technology?
>
> A. That's correct. This is one place where he's suggesting that -- I'm not sure why he put the word "most" in there, makes no sense, but that is what he's suggesting here, yes.
>
> Q. And if you did use wrapped wire technology, how would you make changes and modifications to the circuit?
>
> * * *
>
> THE WITNESS: . . . there's really two types of changes that could be made. Now . . . every device on this board is a programmable or a custom configurable logic device, so if the designer were reasonably good, then the vast majority of design changes that needed to be done within this class of design, in other words, something contains two LCAs and a couple of PAL devices would take place inside the chip, so the vast majority of design changes ought to be things where they would recompile the design. In fact I think Schmitz refers to that in here, saying it only takes a minute or so to make design changes because you would make the change on your little computer terminal, recompile it and download it into the device and then continue your emulation.
>
> But it's also possible that he might decide at some point, gosh, I really

need a third LCA or, gosh, I really only need one PAL instead of two PALs, this is wasting space, so I'm going to take that off and then make appropriate changes in the actual wire wrap.

So possibly the change could take place inside the chips. That would be the most typical. But there would be possibly other enhancements he would make that would require adding new chips to the board.

BY MR. MURPHY:

Q. And in this passage that I referred you to at page 58, left-hand column RX-13, what he's talking about there with changes or modifications in wire wrap would be to physically unwrap the wire on he board and to either make another connection or just to disconnect the previously existing connection?

A. Yes. What he's suggesting here is in this portion, the latter case that I talked about where you may decide, wow, I can't fit this all into two LCAs, I need a third one, for example, and the wire wrap technology gives you a very easy way to add additional chips.

Q. Or to delete a connection?

A. Yes.

(Wynn, Tr. at 2346-2348).

498. RX-13 shows the emulation of a design by partitioning that design between four devices, two FPGAs and two PALs. This is illustrated in figure 3 of RX-13. A PAL is a programmable logic array. (Wynn, RX-706 at Q 29). In figure 3 of RX-13, PALs 1 and 2 are shown as being used for instruction decoding logic and the two FPGAs are used for the remaining logic. (RX-13; Wynn, RX-706 at Q 31, 32).

499. Page 54 of RX-13 states "The XACT development software for the LCA allows an engineer to make simple logic changes using an interactive graphics editor on the single routing, compile the logic into a device configuration bitstream, and download the design data into the target device in under a minute." (RX-13).

500. The Schmitz article does not teach automatic partitioning. Thus, Wynn

testified:

> Q. And as you read article RX-13, you understand that he was talking about doing this partitioning by hand as opposed to automatically partitioning?
>
> A. It appears that's probably what he was talking about, yes.

(Wynn, Tr. at 2345).

501. The Schmitz article teaches using two FPGA's as a hardware prototype of a particular design and if there is interconnect which happens to fall completely within one of the FPGA's, that interconnect can be changed just by changing the FPGA. The Schmitz article does not indicate that all interconnections can be changed electronically. (Butts Tr. at 614-615).

502. Butts received a copy of the article by Nick Schmitz marked as RX-13 before he made the inventions of the '473 and '496 patents. (RPX-13; Butts Tr. at 304-305).

503. [There is no Finding 503].

504. Butts testified that he had been thinking about hardware logic emulation systems prior to learning of the Schmitz article, and that he did not derive his idea about hardware logic emulation systems from the Schmitz article. (Butts CX-210 at 31-32).

Clos Article

505. The Clos article (RX-16) is entitled "A Study of Non-Blocking Switching Networks" and was published in the March, 1953 Bell System Technical Journal, Vol. 32, No. 2. The Clos article is describes:

> a method of designing arrays of crosspoints for use in telephone switching systems in which it will always be possible to establish a connection from an idle inlet to an idle outlet regardless of the number of calls served by the system.

(RX-16 at 406).

506. The October 31, 1965 Spandorfer report entitled "Synthesis Of Logic Functions On an Array Of Integrated Circuits," contract report AFCRI-66-298 (October 31, 1965), discloses a scheme for connecting macrocellular arrays of logic gates (i.e. NAND gates) to one another through a Clos-type switching network. (RX-752 at 3-13 to 3-14; CX-61, p.QM48194).

507. A "Clos network" is not simply a three-stage crossbar network. Rather, as disclosed in the Clos article (RX-16) and the Spandorfer report (RX-742), a three-stage crossbar interconnection structure is non-blocking only where certain mathmatical relationships between the number of input and output terminals on the network and the number of crosspoints in each level of crossbar are satisfied. (RX-16 at 421-423; RX-742 at 3-8 to 3-14).

508. [

]

509. [

]

510. [

]

511. Butts noted that Clos networks only make connections from one output to one input, whereas logic designs have multi-point nets, one output driving many inputs. (Butts CX-210 at 32).

512. McCluskey explained that the operation of one-to-many connections through a device (known as "fanout"), rather than a simple point-to-point connection, makes routing becomes much more difficult in any interconnect architecture. (McCluskey, Tr. at 3982).

513. The file wrapper of the '496 patent contains a December 10, 1993 "Admission of Validity and Infringement and Stipulated Dismissal With Prejudice," in which PiE admitted that the '473 and '353 patents were valid and infringed (CX-61 at QM48303-48304). A "Declaration of Glen M. Antle, executed on December 10, 1993, and part of the file wrapper of the '496 patent, indicates that PiE was acquired by Quickturn in a "reverse triangular merger" arrangement which closed on June 30, 1993. (CX-61 at QM48295-48295).

514. Butts testified regarding his discovery of the "partial crossbar" interconnect, that he started with a nearest neighbor architecture but:

> I found that personally unsatisfactory and I attempted to interconnect logic chips. I did a complete break and totally put the nearest-neighbor architecture aside and attempted to start from first principles to say "okay, I have logic chips, the logic chips have pins, they contains portions of the design and I wish to find a way to interconnect those logic chip pins. I went along a path of finding a way to maintain most of the connectibility of a full crossbar, at least for actual logic circuits, while not incurring the extreme costs of a full crossbar. I succeeded in the partial crossbar interconnect architecture.

(Butts, CRX-48-at Q8).

515. With respect to the Sample et al. RPM prototype, applicants argued during prosecution of the '496 patent that:

> [t]here is nothing in the Sample et al '353 patent which would suggest substituting Applicants' partial crossbar architecture for Sample at [sic] al's 'nearest-neighbor' architecture. Accordingly, Applicants' claims, all directed as they are to partial crossbar configurations, can be distinguished over the Sample et [al] '353 patent.

(CX-61 at QM48265).

Person of Ordinary Skill

516. A person of ordinary skill in the art would have either (1) a bachelor's degree in electrical engineering or computer engineering, and possibly a graduate degree, or (2) equivalent level of experience to a bachelors degree if in fact that person did not have a degree, and several years of industrial experience in the design and development of digital systems. (Butts, Tr. at 393; Wolfe, Tr. at 2752-54; Sapiro, Tr. at 864).

L. Infringement

[

]

518. [

]

IX. Conclusions of Law

1. The Commission has in rem jurisdiction, subject matter jurisdiction and in personam jurisdiction.

2. There has been an importation of Meta systems which are the subject of the unfair trade allegation.

3. Complainant is likely to succeed on the merits with respect to establishing that there is a domestic industry defined by the claims in issue.

4. Complainant is likely to succeed on the merits in establishing that the doctrine of assignor estoppel is applicable to the facts of the investigation, and respondents Mentor and Meta are estopped from challenging the validity of the '473 and '493 patents.

5. Independently of the doctrine of assignor estoppel complainant is likely to succeed on the merits in establishing that the claims of the '473 patent and of the '496 patent in issue are valid and enforceable.

6. Complainant is likely to succeed on the merits in establishing that each of the respondents infringe the claims in issue.

7. Complainant has established that it will suffer irreparable harm in the absence of temporary relief.

8. The balance of harms favors the granting of temporary relief.

9. The public interest does not preclude the granting of temporary relief.

10. Motion No. 383-1 is granted.

11. On the granting of Motion No. 383-1, a temporary limited exclusion order should issue. Also temporary cease and desist orders, against each of the respondents, prohibiting the sale (except under bond) of Meta emulators present in the United States at the date of entry of the order but not prohibiting respondents' marketing and sales activities

related to Meta emulators that might be imported or sold under bond and not relating to replacement parts.

12. On the granting of Motion No. 383-1, complainant should not be required to post a bond. Mentor/Meta should be required to post a bond of 25 percent of the entered value of each Meta emulator imported during the temporary relief period.

X. Initial Determination And Order

Based on the foregoing findings of fact, conclusions of law, the opinion and the record as a whole, and having considered all of the pleadings and arguments presented orally and in briefs, as well as proposed findings of fact, Motion No. 383-1 is granted.

The administrative law judge hereby **CERTIFIES** to the Commission this initial determination, which is not a final initial determination, together with the record consisting of the following:

1. The transcripts of the prehearing conference, the hearing and the closing arguments;

2. The exhibits, admitted into evidence and the exhibits as to which objections have been sustained; and

3. ALJ Exhibit 1 (Mentor's May 28, 1996 letter to the administrative law judge) and ALJ Exhibit 2 (Bull's comments concerning the issues of remedy, the public interest and bonding).

The pleadings of the parties filed with the Secretary are not certified, since they are already in the Commission's possession in accordance with the Commission's final rules.

Further, it is ordered that counsel for the parties shall have in the hands of the administrative law judge a copy of this initial determination with those portions containing confidential business information designated in brackets no later than Tuesday, July 27, 1996. Any such bracketed version shall not be served by telecopy on the administrative law judge. If no such version is received from a party, it will mean that the party has no objection in removing the confidential status, in its entirety, from this initial determination.

Pursuant to the Commission final rule 210.24(17(ii), this initial determination shall become the determination of the Commission thirty (30) calendar days after issuance of this "more complicated" investigation, unless the Commission modifies or vacates the initial

determination within that period.

Paul J. Luckern
Administrative Law Judge

Issued: July 8, 1996