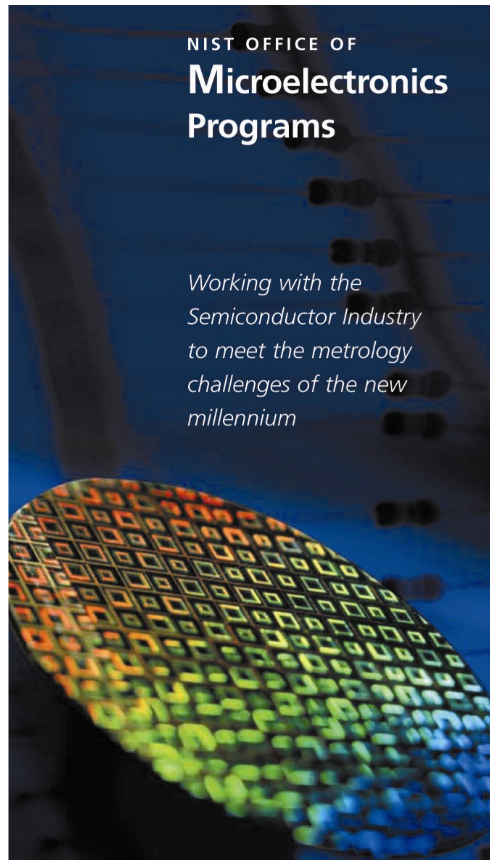
Electronics and Electrical Engineering Laboratory
Office of Microelectronics Programs

NIST
National Institute of Standards and Technology




# Strategic Forecast

*"Ad eundum quo nemo ante iit."*

*"The future isn't what it use to be"*

***Presentation at SEMICON West from Jean-Christophe Eloy, GM of Yole Developpement, a market research and consulting group based in Lyon, France.***

## September 2006

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# EXECUTIVE SUMMARY

The semiconductor industry and its supporting infrastructure, once completely vertically integrated, are global and highly fragmented. The invention of the integrated circuit has enabled enormous productivity gains in information processing and communications. These productivity gains are expected to continue through dimensional shrinking but also through incorporation of additional functions.

Steeply rising research and development costs have driven the participants to form consortia and clusters of collaboration. First these were regional but are now global. In order to focus research and development activities on critical barriers to progress the industry maintains the **International Technology Roadmap for Semiconductors**, (ITRS) a consensus document of over 600 pages of barriers to progress and potential solutions.

The enormous investments necessary in order to manufacture leading edge semiconductor products have forced nominal competitors to create joint ventures. This trend is relatively recent, but can be expected to continue.

The National Bureau of Standards, now the National Institute of Standards and Technology (NIST), has played a key role in developing measurement methods and standards in support of the semiconductor industry. In Fiscal Year 2006 the National Semiconductor Metrology Program (NSMP) is funding $12M in metrology development at NIST. These funds are roughly matched with other funds, including Laboratory STRS, and Other Agency, for a total effort of about $25M.

Since its creation in 1992 the NSMP has focused most of its funding on near term problems. With traditional scaling becoming increasingly problematic the focus on longer term issues associated with “Ultimate CMOS” and “Beyond CMOS” will need to be funded with a larger portion of the available funding. These projects will be closely coordinated with the Center for Nanoscale Science and Technology. The existence of the Nanofabrication Facility and the recent acquisition of state-of-the-art metrology tools such as the custom environmental scanning electron microscope and the dual beam focused ion beam scanning electron microscope will greatly enhance the NIST capability to develop novel metrology for nanoelectronics.

The OMP staff will continue to monitor the ITRS activities closely to maintain up to date knowledge of the metrology needs of the semiconductor manufacturing industry, and adjust the portfolio appropriately.

# CUSTOMERS

**Industry**

In its infancy, the semiconductor electronics industry was highly vertically integrated. The early manufacturers were well known electronics companies. These companies included Western Electric, IBM, General Electric, RCA, NEC and SONY. They had to design and build much of their own manufacturing equipment and prepare their own materials. Although Bell Laboratories had to license its intellectual property, many aspects of the technologies were highly proprietary. After the invention(s) of the integrated circuit[1] the industry expanded rapidly, especially in "Silicon Valley," the San Francisco Peninsula. Gradually the manufacturing processes converged, especially in Silicon Valley, largely the result of job-hopping.[2]

The semiconductor manufacturing industry grew rapidly, displacing the electron tube and relay logic technologies. Competition drove manufacturers to put more and more function into single chips by shrinking dimensions. This led Gordon Moore in 1965 to formulate his famous "Moore's Law."

Over time, manufacturers began divesting their equipment and material supply functions, and companies such as Applied Materials grew rapidly.[3] This phenomenon is a natural consequence of economies of scale. Curiously, many Japanese companies still maintain some internal equipment development and manufacture.

The industry now has aligned itself into designers, suppliers, and semiconductor manufacturers. Some manufacturers, Independent Device Manufacturers (IDMs) retain design and manufacturing functions. These include Intel, AMD, IBM, NEC, Fujitsu, Philips and Infineon. Others serve as "foundries" which provide manufacturing services to other companies. These include TSMC, UMC, Chartered Semiconductor and SMIC. "Fabless" companies design only. These include LSI Logic, Agere (the remains of the Western Electric Microelectronics Division) and many small companies. Economy of scale has forced the latter group out of the manufacturing arena. Competitors form joint ventures to manufacture large volume products, especially memory. For instance, Intel and Micron formed IM Flash Technologies to manufacture NAND Flash memory. Hitachi and Mitsubishi Electric formed Renesas to manufacture a variety of products, including microcontrollers and microprocessors.

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[1] Jack Kilby (Texas Instruments Incorporated); US Patent Number 4,042,948, originally filed 6 May 1959, and Robert Noyce (Fairchild Semiconductor Corporation); US Patent Number 2,981,877, filed 30 July, 1959.
[2] This was less prevalent in the old line Eastern electronics manufacturers, largely because they enjoyed low employee turnover. For instance in the 1970s when the Silicon Valley companies were using aluminum metallization, Western Electric was using Ti-Pt-Au under the misguided assumption that it was more reliable.
[3] For instance, Bell Laboratories transferred its plasma reactor technology to Applied Materials and its e-beam mask writer to ETEC; Motorola divested its plasma reactor technology to Tegal.

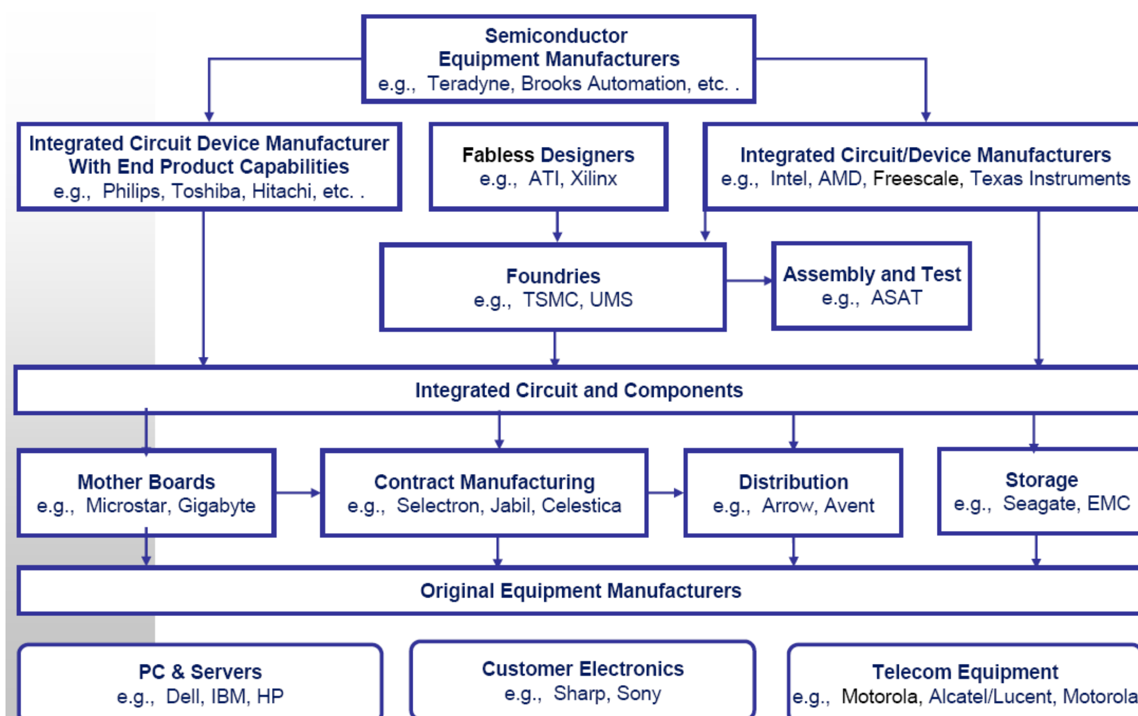


**Figure 1; Current Industry Structure**

NIST researchers interact extensively with collaborators from IDMs and equipment and materials suppliers. It is imperative that these interactions be maintained and strengthened for maximum effectiveness of the projects. One especially noteworthy example is the presence of Dr. Kwang Woo Choi, a visiting scientist from Intel, working on resist characterization in the Polymers Division. Kwang Woo acts as a liaison to all semiconductor device research at Intel, and through him a signicant collaboration between John Suehle in the Semiconductor Electronics Division and the Intel team working on advanced channel designs has begun. Also, Intel is funding a NIST employee, Dr. John Woodward, working on resist metrology in the Optical Technology Division using scanning chemical force microscopy.

## Consortia and Collaborative Clusters

Once dominated by US manufacturers, Japan began making serious inroads in the late 1970s. The MITI-led VLSI Project (1976)[4] and the US Defense Research & Engineering-led VHSIC Project (1978) were two government initiatives meant to spur innovation and gain or retain prominence in this growing industry. As the competition between Japan and the US heated up, American companies formed the first true consortium, the Semiconductor Research Corporation

[4] The VLSI Project had reversed engineered the Perkin Elmer lithography tool resulting in Nikon and Canon entering the market with improved tools, and driving Perkin Elmer out of the market. Today there are no US manufacturers producing leading edge lithography tools.

in 1982. Its mission was to help academia produce trained advanced degree scientists capable of contributing immediately to the US semiconductor industry. Consortia became the new model for dealing with the ever mounting investments necessary to maintain the rapid productivity improvements demanded by the customers.

- **Semiconductor Research Organization** (1982), **Larry Sumney** President. The charter is to fund training of advanced degree scientists and engineers in silicon technology, unfettered by ITAR considerations. http://www.src.org

- **IMEC** (1984) was founded as a non-profit organization led by **Prof. R. V an Overstraeten** and under the supervision of a Board of Directors, with delegates from industry, Flemish universities and the Flemish Government. **Prof. Gilbert Declerck** was appointed President and CEO upon Van Overstraaten's death in 1999. http://www.imec.be

- **SEMATECH** (1987); **Larry Sumney** as Managing Director, then **Robert Noyce** as CEO. **SEMATECH** was formed to help US equipment manufacturers and materials suppliers improve their products.[5] It is staffed by assignees from the member companies. The member companies represent over half the total worldwide semiconductor production. http://www.sematech.org

- **SELETE** (1996); Selete was founded in 1996 as a consortium for development of 300mm-wafer based production technologies with an equal capital investment from 10 semiconductor manufacturers. Selete joins the private funded project, Asuka II, and the government funded AIST. It worked closely with **ICCI**, a former subsidiary of **SEMATECH** on 300 mm wafer and equipment standards. http://www.selete.co.jp/?lang=EN

- **Albany NanoTech** (1997?); founded and directed by **Alain Kayoleros**, is an adjunct to the University at Albany. Strictly speaking it is not a consortium, but with over 150 industrial affiliates it looks remarkably like one. In many respects it resembles **IMEC.** The facility is truly impressive; they have a 200 mm CMOS line running with significant military and MEMs work, and two 300 mm facilities for process development. TEL, one of the largest equipment supplier companies, has moved a major equipment development facility there from Austin, TX. IBM has a significant presence, as does Hitachi High Technology, Infineon, and even Intel has a presence. SEMATECH has a presence, doing Extreme Ultraviolet Lithography (EUVL) development at this facility. http://www.albanynanotech.org/

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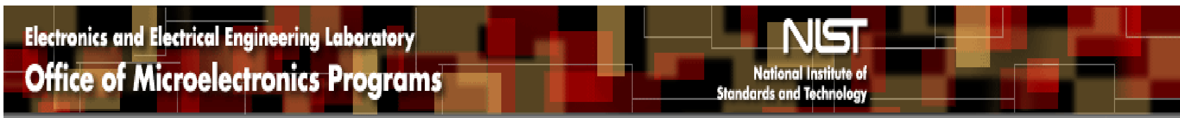
[5] SEMATECH is a subsidiary of the Semiconductor Industry Association. The International Semiconductor Manufacturing Initiative (ISMI) and the Advanced Technology Development Facility (ATDF) are subsidiaries of SEMATECH.



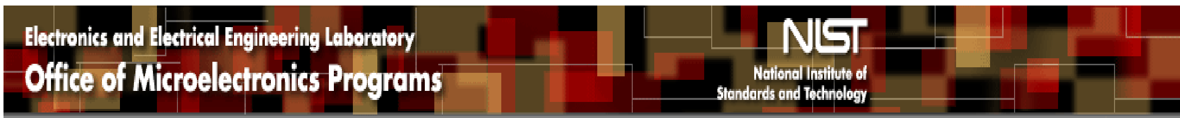

In this arena, NIST researchers interact extensively with collaborators from SEMATECH and SRC. It is essential for the health of the NIST effort that these interactions be maintained and strengthened. Additional collaborations with other consortia and collaborative clusters should be explored.

An excellent example of a close collaboration is the presence of a NIST assignee at SEMATECH in the critical dimension and overlay metrology area.[6] The presence of the assignee on site at SEMATECH helps disseminate the discipline of metrology while being able to have intimate contact with the metrology issues facing the industry.

Finally, while academic institutions are not strictly speaking direct customers, extensive interactions with academia and NIST researchers are a significant and useful part of the success of the National Semiconductor Metrology Program. The **SRC** funds graduate students in over 50 universities worldwide. The Focus Center Research Program additionally funds post-doctoral research in numerous universities.

The Nanoelectronics Research Initiative is administered by SRC but is largely funded by states, NSF, and DARPA.

[6] Dr. Ron Dixson spent over two years on this assignment; Dr. George Orgi is in his second year there. Both are members of the Precision Engineering Division.




# LITHOGRAPHY METROLOGY PROGRAM

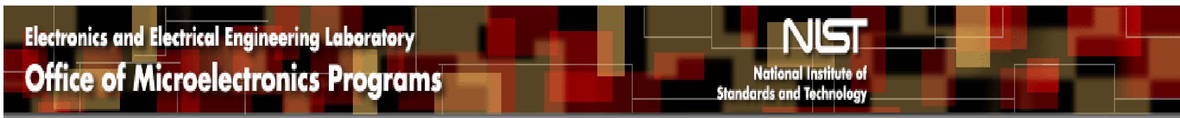
The overall goal of this task is to support developments in DUV and EUV. The areas of emphasis are characterization of lens materials, and immersion fluids, laser calorimetry, radiation detector sensitivity and damage.

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The industry at this point has moved into the deep ultraviolet (DUV) spectrum. Currently, exposure tools operating at 193 nm are in leading edge manufacturing facilities. The first 193 nm immersion lithography tools have been shipped to leading edge manufacturers and are being used for final development of next generation semiconductor product. High index fluids and lens materials for 193 nm tools are under intense exploration to develop higher numerical aperture systems.

Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13.6 nm is being investigated, and demonstration tools are being designed and assembled. Two alpha tools have been shipped to development consortia in 2006. EUV lens metrology, and metrology for the development of advanced photoresist materials for EUV are critical projects that need additional support. Development of interferometric EUV exposure for resist metrology is a critical gap in the portfolio.

Nano Imprint Lithography is the “dark horse” in the next generation lithography race, but shows enormous promise. NIST now has a tool, and researchers are beginning the task of defining metrology issues.

## FY 06 OMP FUNDING: $923K

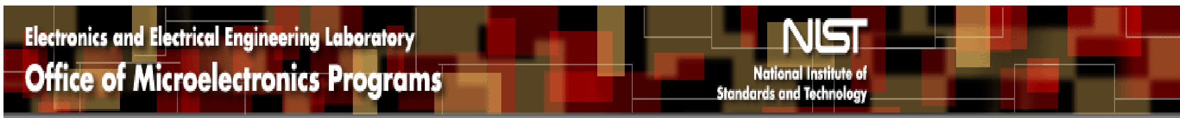



# Critical Dimension and Overlay Metrology Program

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes ≈35 % of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, development of advanced critical dimension and overlay techniques, and comparisons of different critical dimension and overlay measurement techniques.

Currently, critical dimension and overlay measurements improvements have barely kept up with lithography capabilities. To maintain cost effectiveness continued advances need to be made. Recent acquisition of state-of-the-art equipment installed in the Advanced Measurement Laboratory has put NIST in an excellent position to continue serving the industry at a high and most visible level with this program. NIST needs to continue to monitor progress on alternative microscope technologies that show great promise, such as the helium ion microscope. Partnerships with SEMATECH and other similar entities need to be encouraged in order to supply meaningful artifacts the industry needs.

## FY 06 OMP Funding: $2,089K




# Front-End Processing Metrology Program

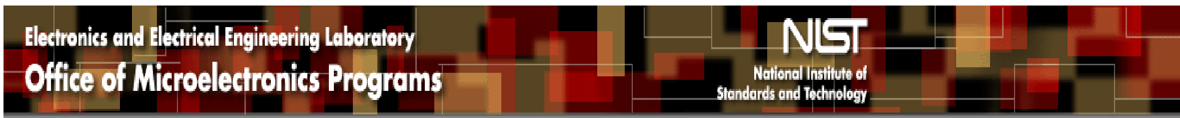
The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and wafer flatness and roughness metrology as well as electrical and reliability characteristics. The gate dielectrics, traditionally $SiO_2$ and SiON, will soon no longer be viable. The overall task is to provide starting wafer dimensional and defect metrology, suitable metrology and reference materials for their dielectrics and junctions, including electrical characterization, gradient, thickness and roughness metrology and overall reliability metrology.

Greater emphasis on reliability needs to be implemented.

The potential for increasing wafer diameter from 300 mm to 450 mm needs to be followed carefully, so that needed equipment for the relevant metrology can be acquired in time to be effective.

## FY 06 OMP Funding: $1,720K




# Interconnect and Packaging Metrology Program

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. Environmental pressures are leading to the reduction and eventual elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as a circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.

The potential for using multi-wall carbon nanotubes for interconnect conductors needs to be watched, and the relevant metrology developed if further progress is made.  Optical interconnect is another area of opportunity demanding attention.

## FY 06 OMP Funding: $1,460K

# PROCESS METROLOGY PROGRAM

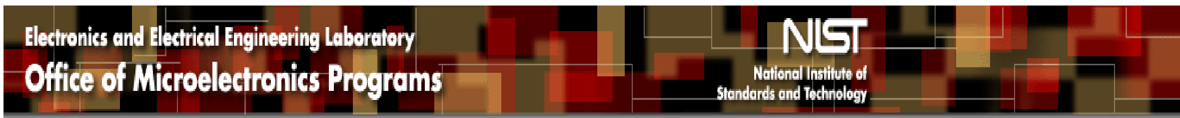
Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth — silicon, oxygen, and aluminum.

Recently, however, copper has been introduced for interconnect conductivity, replacing aluminum alloys. A variety of low-dielectric constant materials are being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling current has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material is sufficient, but in the near future more exotic materials such as transition metal oxides, silicates, and aluminates will be required. As dimensions are reduced, gate depletion effects and dopant diffusion through the gate dielectric are limiting transistor performance. With the replacement of the traditional silicon dioxide/polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products. Critical physical parameters need to be measured on a wide variety of reactive and non-reactive process gases, allowing the accurate calibration of flow meters and residual gas analyzers. Water contamination at extremely low levels in process gases presents serious manufacturing difficulties. Accurate calibration of water vapor at extremely low vapor pressures is required.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products and a wide variety of metrology issues emerge in plasma, chemical vapor, and rapid thermal processing steps used in semiconductor manufacture.

# FY 06 OMP FUNDING: $1,115K

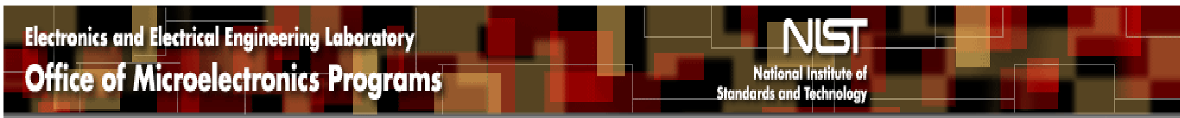



# ANALYSIS TOOLS AND TECHNIQUES PROGRAM

The continuing shrinking of device dimensions and the rapid inclusion of new materials into device fabrication demands the development of new analytical tools and techniques. The need for new analytical techniques and tools has increased as the components in the transistors approach the low nanometer level and the number of transistors per chip approaches 1 billion. The development of tools capable of characterizing the structures produced in the laboratories as well as those needed to confirm the manufacturing process require significant improvements; although those used for production also require significant speeds not to slow down the commercial manufacturing. This latter condition may require some sacrifices in the resolution and accuracy of those tools. In addition, more significant modeling capability is critically needed to fill in the knowledge gap in domains where measurements can not be performed. Significant improvements in tools capable of analyzing properties of defect particles in the sub-30 nm size are urgently needed.

The High Resolution Microcalorimeter X-ray Spectrometer for Chemical Analysis project must be funded for success in the face of probable rapidly declining Other Agency funding.

## FY 06 OMP FUNDING: $370K



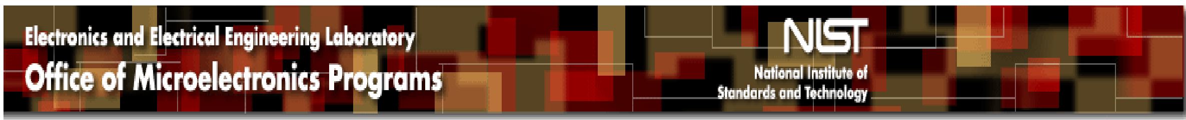

# Device Design and Characterization Program

As microelectronics pushes into the nanoelectronics regime, traditional CMOS is reaching its fundamental limits. New device structures need to be characterized, such as Multi-Gate FETs (MUGFETs), fully depleted and partially depleted silicon-on-insulator, various alloys such as silicon-germanium and silicon-germanium-carbon, strained layers and other exotica such as carbon nanotube and molectronic device structures. Another addition to the portfolio is the emerging field of organic materials electronics. To this end we have initiated a new program, "Device Design and Characterization."

The challenges characterizing Ultimate CMOS and Beyond CMOS structures are daunting, and this program needs to be expanded significantly. An especially important metrology development needed now is to be able to measure local strain at the device level.

One project that has to be highlighted because it will impact all the projects in the portfolio over time is the Advanced Measurements Nanofabrication Facility Support project. With the completion of the Advanced Measurement Laboratory on the Gaithersburg, Maryland campus, we have populated a cleanroom facility with advanced processing and metrology equipment suitable for advancing into the nanotechnology era. Over time additional equipment will need to be purchased.

## FY 06 OMP Funding: $2,560K

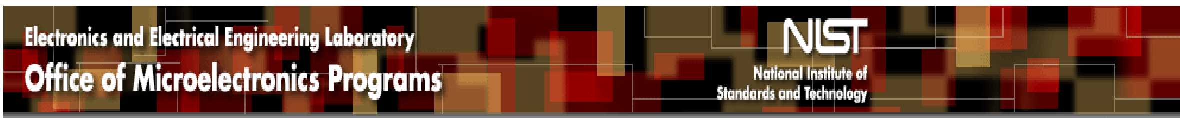



# SYSTEM DESIGN AND TEST METROLOGY PROGRAM

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The addition of new functions to provide system on-chip solution pose additional testing challenges. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing IC contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is essential to develop accurate testing strategies.

## FY 06 OMP FUNDING: $780K




# MANUFACTURING SUPPORT PROGRAM

Cross-cutting all manufacturing disciplines is the need for supporting information technology and processing capabilities. The transition to 300mm fabs, single-wafer lots, and the extensive use of foundries has made efficient information handling and automation indispensable to the production process. Information technology touches nearly every aspect of semiconductor production and distribution, including process control, tool to tool interconnect, automated material handling and tracking, reticle management, and information interchange across the supply chain. NIST is working with the International Semiconductor Industry Initiative (ISMI, a subsidiary of SEMATECH) to provide and maintain an on-line engineering statistical handbook to support process control, and is working with industry on standards required to support information flow across the "engineering chain," and to provide standards for secure electronic diagnostic data.

The rapid introduction of advanced equipment control, advanced process control, automation and e-manufacturing, driven by the need to improve reproducibility by reducing the human element, by the ergonomic considerations forced by the use of larger and larger wafers, and by the need to achieve full equipment utilization, makes this program ripe for significant expansion.

## FY 06 OMP FUNDING: $270K